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Pin Electronic (PE) with Levels Specification Using ATE Tester

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Abstract

The increasing complexity of electronic components and their stringent performance requirements necessitate precise and reliable testing methodologies. This study explores the development and implementation of a pin electronic system with level specification using Automated Test Equipment (ATE) testers. The purpose of ATE implementation is to drastically reduce human error, increase test throughput, and provide precise, real time data analysis. By utilizing advanced ATE platforms, the study evaluates the accuracy, repeatability, and scalability of the testing process. The proposed approach for the creation of the DTI board is to study the behavior of components that contribute to the levels of VIH, VIHH, and VIL values, thus, influencing the measurement of the PE electronic pins. The results demonstrate significant improvements in measurement precision and test cycle efficiency, offering a robust solution for quality assurance in semiconductor manufacturing. These findings provide valuable insights into optimizing test protocols for high-performance electronic components and pave the way for future advancements in ATE-driven testing methodologies.

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I. INTRODUCTION

Systems for Automatic Test Equipment (ATE), which include BJT and CMOS devices, are crucial in the production of semiconductor devices. The equipment, which is more generally referred to as “testers”, enable manufacturers to test each device for engineering characterization and/or production validations. Unfortunately, testing can be expensive when ensuring correct functionality with acceptable performance. In general, the complexity of the device-under-test (DUT) makes 100 percent incoming inspection using ATE no longer practical or cost-effective for most quality control organizations. One of the most crucial elements in selecting the right kind of tester is the cost of the test, as developing ATE systems that are affordable is one of the reasons [1].

In prior ATE systems, the DCL (Drive Comparator and Active Load) was integrated into the same integrated circuit (IC) and the PMU was a separate unit. The DCL and PMU were then connected to the PE board; therefore, more PE channels could be integrated into the PE board. Additionally, the integration of the PMU into the PE board enhances the system reliability by eliminating the need for mechanical relays [2].

An integrated circuit is subject to a variety of tests from initial design specifications to full-scale manufacturing production, and the importance of testing at the specified time points reflects the need to acquire information about the device for various reasons [3]. ATE stands for Automatic Test Equipment system. These systems play a critical role in semiconductor device verification and production testing. However, the conventional ATE architecture often faces several limitations, and constraints in measuring accuracy, particularly in measurement accuracy when dealing with high-speed or low-power devices. In addition, parasitic effects, signal integrity issues, and hardware complexity can further affect the reliability of the test results. These challenges highlight the need for improved testing methodologies and system architecture. Thus, this research aims to address these limitations by proposing an enhanced approach that improves measurement accuracy and test efficiency while maintaining compatibility with existing ATE infrastructures.

The drivers are typically connected to the logic input, which outputs one of two analog voltages. These drivers are commonly referred to as pin drivers, they are usually connected to a contact pin that is mechanically connected to a board or component lead [4]. In the semiconductor production process, wafers are cut into individual ICs, which still undergo testing before pre-assembly. ATE system are constructed to conduct wafer-testing based on identifying failures of the ICs at an early stage before further manufacturing processes. This helps reduce the cost of production by preventing defective components from progressing further in the assembly line.

ATE systems are instrumental in yield improvement in semiconductor manufacturing. These systems provide insight

into production performance, identifying areas where defects are most likely to occur. The system helps manufacturers fine-tune processes, increasing yields and reducing waste.

Figure 1 shows the illustration of the connection from the Digital-to-Analog Converter (DAC) and Analog-Digital Converter (ADC) to PMU measurement, as well as the Event Generator and Timing connection to the Pin Electronic. Each connection is connected to the DUT channel by a relay. Thus, the PMU is commonly used for FVMI (Force Voltage Measure Current) in Functional measurement mode applications, such as input bias current measurement. During the measurement, the PMU applies a voltage on the DUT pins, and the corresponding current is measured. Continuity testing is also a common testing method for the PMU, in which a current is forced into the DUT pins, and the resulting voltage is measured to verify the functionality or presence of the ESD diode. PMU with a wide dynamic range can be used for measuring very low leakage current (<1nA) and very low impedance (<5). ATE-based solutions provide attractive economics for production since the measurement instrumentation is not duplicated for each device or load board but is applied only once within the test system [5].

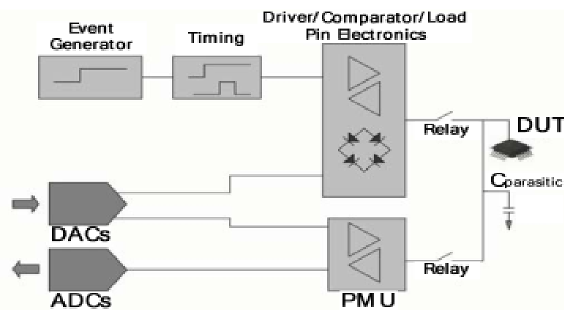


Figure 1. Tester Block Diagram Connection

II. RELATED WORKS

System-type VLSI circuit have recently been developed and pose new difficulties for Automatic Test Equipment (ATE), as well as in fixing and connecting circuits to testers. BGA packages with high ball counts, often approaching near 1000, require more tester channels than what most Automated Test Equipment (ATE) systems can provide [6].

The DC PMU provides four main functions: forcing voltage, forcing current, measuring voltage, and measuring current. Op-Amp A1 supports forcing voltage or current by using one of two feedback loops. A1 can be configured as a Unity Gain Buffer for voltage forcing or as a Voltage Controlled Current Sources (VCCS) for current forcing. These configurations depend on whether the feedback loop includes a Unity-Gain buffer A5 or another feedback loop involving A1, which consists of three op-amps [7].

The conventional structure faces challenges with offset, mismatch, and stability due to the complexity of multiple op-amps, resistors, and feedback loops [8]. The previous parametric measurement unit using DDA technology is limited in the operating range of the FVMI mode due to structural constraints inherent to the DDA-based instrumentation. A significant approach has been defined by introducing the integration of Parametric Measurement Unit (PMU) directly into the Driver, Comparator, Active load (DCL) circuitry. This integration eliminates the need for mechanical relays, increases the PE channel density, and improves system reliability [21]. Others describe that the use of solid-state power systems can improve power system performance as the components act to manage overload voltage or current, safeguarding devices from parameter variations [20]. Using extra parameters of MOSFET can also be another option, functioning similarly to a relay, as the component enables turn-on and turn-off transitions and ensures that the switching voltage of the MEMs switch is virtually zero [19].

The objective of this research is to improve the performance and reliability of HEX inverter testing devices, aiming to reduce errors and operational issues encountered during testing on Automatic Test Equipment (ATE) systems and dedicated load boards. The study is intended to support enhanced functionality and consistent reliability in ATE applications. This includes the development of voltage level circuit specifications specifically designed for ATE integration, with modifications involving the use of relay switches to optimize performance. Additionally, the research involves analyzing data obtained from circuit simulations and comparing the results with theoretical values derived from mathematical calculations to validate the design's accuracy and effectiveness.

III. METHODOLOGY

This section presents a comprehensive overview of the methodology employed for the development of the relay switching circuitry, beginning with the conceptual phase and continuing through simulation, circuit protection strategy, and comparative performance evaluation. The aim is to establish a reliable, simulation-validated circuit design that aligns with the functional requirements of Automatic Test Equipment (ATE) environments.

The methodology process, illustrated in Figure 2, starts with the circuit design phase using PSPICE, a powerful circuit simulation software widely utilized in academic and industrial applications. PSPICE offers an extensive library of passive and active electronic components—including resistors, capacitors, inductors, diodes, transistors, and integrated circuits—each modeled using accurate electrical parameters. This enables realistic simulation of circuit behavior under various operating conditions.

The design focused on creating a reliable relay-based switching system capable of handling voltage and current levels typical in HEX inverter testing scenarios. The COTO 9202 electromechanical relay was selected due to its fast-switching capabilities, stable mechanical structure, and compatibility with standard ATE hardware interfaces. The relay was particularly suited for signal routing and control in test systems where precision and reliability are critical.

To enhance the performance and durability of the relay circuit, passive protection elements were integrated into the design. Specifically, flyback diodes were placed across relay coils to suppress inductive voltage spikes generated when the relay was de-energized. These diodes were essential in preventing EMF from damaging other components in the circuit. Furthermore, capacitors were strategically positioned at high-current paths to act as local energy reservoirs. Their purpose was twofold: to smooth out voltage fluctuations and to mitigate transient currents that could lead to relay contact degradation or false triggering.

The power supply to the circuit was selected based on the

electrical requirements specified in the relay's datasheet, ensuring proper actuation voltage and current without exceeding the safe operating limits of the components. Accurate supply matching was critical to ensure reliable switching and to prevent mechanical wear or misoperation of the relay.

Following the implementation of the circuit design, simulation analysis was carried out using PSPICE. This phase allowed for detailed observation of circuit behavior during switching operations, including transient response, voltage regulation, and timing accuracy. The simulation outputs such as switching delay, voltage across contacts, and current flow were recorded for further evaluation.

To validate the simulation results, mathematical models of the circuit were developed based on fundamental electrical engineering principles. Kirchhoff's Voltage Law (KVL), Kirchhoff's Current Law (KCL), and differential equations governing RLC circuits were used to calculate theoretical expectations for each stage of operation. The simulated data was then systematically compared to these theoretical values to identify any discrepancies and ensure consistency between design intent and simulated behavior.

This comparison not only confirmed the accuracy of the circuit model but also provided insights into potential deviations that might occur during physical implementation. Any notable inconsistencies were analyzed to determine whether they stemmed from component tolerances, model limitations, or other external factors.

The methodology concludes with an evaluation of the relay circuit's readiness for physical prototyping. Only after the design achieved satisfactory performance in both simulation and theoretical analysis was it considered viable for integration into the ATE test system for HEX inverter evaluation.

The use of PSpice facilitates the creation of circuit components and improves understanding of the component list used in the design. Therefore, Figure 3 illustrates a portion of the circuit developed to achieve the required VIH voltage level, with the expected voltage range between –1 V and 7 V.

The circuit was designed and simulated using PSPICE to achieve the required VIH voltage level. An LM324 operational amplifier was configured with a feedback network consisting of Rin at value 10 kΩ and Rf at 10 kΩ to control the gain and stabilize the output voltage. The amplifier operated with ±20 V supply rails to allow sufficient output voltage swing. Additionally, a voltage divider composed of R1 at value 10 kΩ and R2 at approximately 23.3 kΩ was used to scale the output voltage to the required VIH level. Through simulation, the circuit demonstrated the capability to generate voltage levels within the target range of –1 V to 7 V, ensuring compatibility with the intended testing requirements. A similar approach was applied to the VIHH level design, where the components used were primarily standard elements such as resistors, operational amplifiers, and voltage divider to control and compare different voltage level inputs across interconnected circuits.

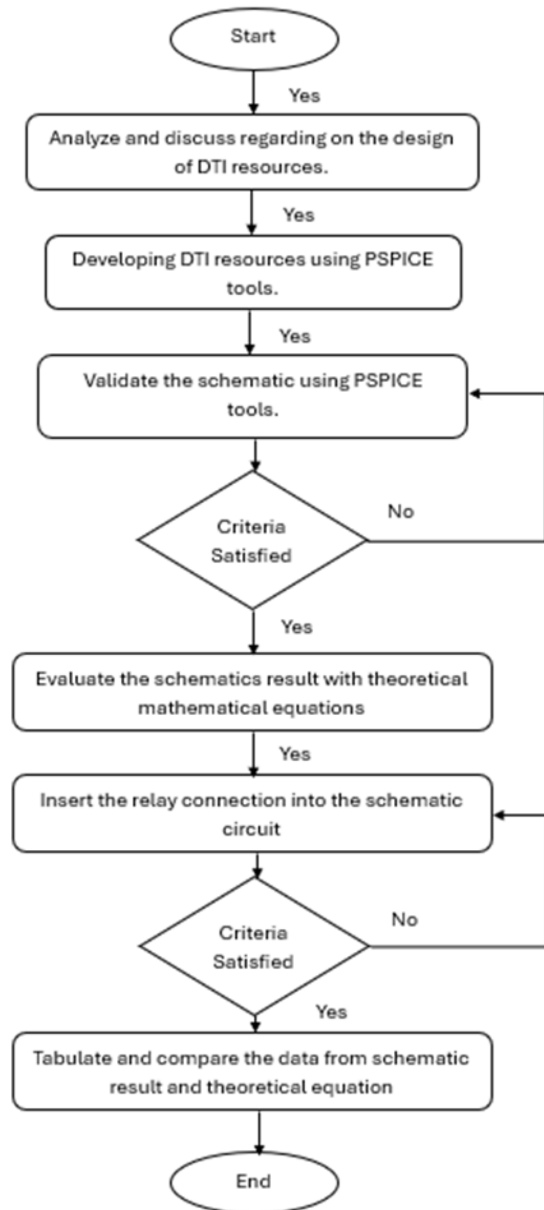


Figure 2. Methodology Process

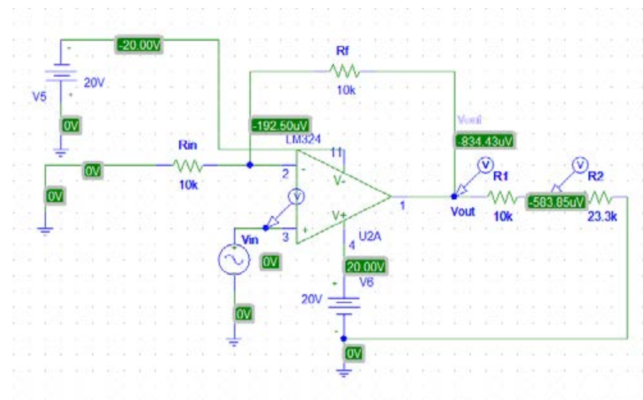


Figure 3. Non-inverting operational amplifier VIH voltage level

IV. AUTOMATIC TEST EQUIPMENT (ATE)

Automatic Test Equipment (ATE) systems are widely used in the electronics industry to perform high-precision testing of components and assemblies through computer-controlled instruments. These systems automate the process of applying test signals and measuring responses, making them vital for

ensuring product quality, especially in high-volume production. A well-designed ATE system requires a deep understanding of test technologies, proper calibration scheduling, and careful integration of digital and analog test instruments such as Digital Test Instrument (DTI) and Analog Performance Instrument (API) boards. For example, a DTI board can handle up to 128 channels per unit and supports operations such as waveform generation, error processing, and DC parametric testing, making it a core component in digital circuit evaluation.

Despite their automation, ATE systems still involve manual steps such as configuring parameters and reviewing results, which may introduce human error. Additionally, the cost and complexity of ATE, especially during early-stage chip evaluation, have led to a demand for simpler, in-house testing alternatives. One such method is the supply current test, commonly referred to as ISS or IDDQ testing.

The ISS test is a defect-oriented technique that measures the device's supply current under steady-state conditions. In CMOS circuits, normal quiescent current levels are typically low, so any significant increase often indicates defects such as bridging faults or leakage paths. By monitoring supply current, this method can detect faults that may go unnoticed in traditional logic testing. It is especially effective when used in conjunction with functional and structural testing techniques, contributing to improved fault coverage, early defect detection, and overall product quality.

Together, ATE-based testing and supply current analysis provide a comprehensive framework for validating circuit integrity and functionality, balancing automation with defect-specific diagnostics across both digital and analog domains.

A. *ATE Tester*

An Automatic Test Equipment (ATE) system uses computer-controlled test devices to administer stimuli and measure responses accurately. To create a new ATE system, it is important to understand current test technologies, identify needs, and use a straightforward design methodology [7]. Instruments used in the ATE can naturally shift in accuracy over time. The determination of calibration intervals (the time between two consecutive calibrations) is a critical issue. A long calibration period increases the chance of exceeding tolerance, while a short interval wastes resources and disrupts the routine instrument operation [8].

To assemble the test equipment, testers are evaluated based on circuit card assemblies that comprise the switching devices. The building of the tester equipment that satisfies the performance test and applies the completed test equipment to the actual production process to examine if it is effective in improving the performance test time and functionality [9]. However, ATE does not eliminate the possibility of operator error as the testing procedure is not entirely automated. Operators manually install measurement parameters, launch measurement, record findings, and ensure conformity with specifications [10].

Test set programming can be difficult and repetitive. Test engineers may ignore problems when examining their own work due to programming bias. To avoid this, software should be treated as published work, with an impartial reviewer checking for design, quality, and faults [11]. While BIT and ATE are useful in testing, they do not offer a comprehensive diagnostic solution for on-platform maintenance. This can leave a gap in a system`s maintenance philosophy if users want to reduce No Evidence of Failure (NEOF) rates without using ATE in operational environments [12]. Although ATE systems offer high automation, they are costly and require precise setup and specialized personnel. As a result, ASIC makers demand alternative testing solutions that can be carried out in-house during the early chip evaluation phase [13].

ATE tester can be divided into two types for data analysis and production testing, such as DTI board and API board. DTI board stands for Digital Test Instrument and API board refers to Analog Performance Instrument. One of the boards used for testing and development purposes is the DTI board. The board has 128 channels per board, each with PMU and high-voltage support. On the MX system, up to 12 boards can be configured for a total of 1536 digital channels. Each DTI board performs vector waveform generations, error processing, and DC parametric testing for each PE channel. Furthermore, each DTI has a DUT capture processor that is accessible to all channels on the DTI board. Figure 4 shows the block diagram of the DTI board.

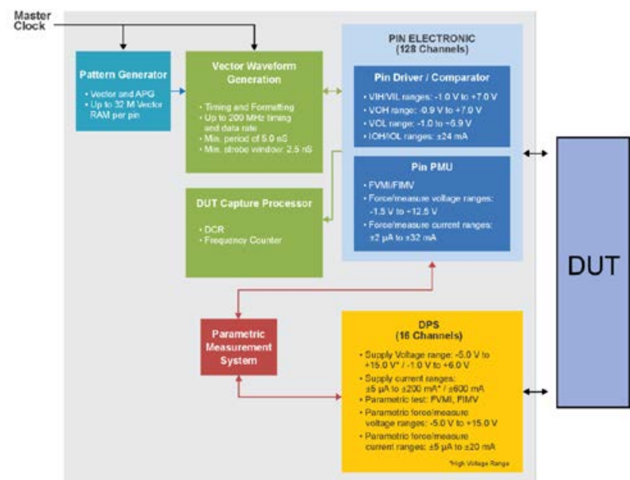


Figure 4. Block Diagram of DTI Board

B. *Supply Current Test (ISS)*

The leakage current (ISS) test is a defect-based test that analyzes device supply current during steady-state conditions [14]. In static CMOS circuits, the ICC/IDDQ is typically low due to natural circuit leakages and the absence of a direct connection between power and ground during the quiescent state. High ICC levels indicate significant leak into the power supply bus. The power supply current is directly observable and can uncover problems that would otherwise go undetected during logic testing. This technique has gained popularity because of its simplicity [15].

Square signals are commonly employed as inputs in digital circuitry. IDDT current only appears at rising or falling edges of digital circuit inputs. In analog circuits, IDDT current can occur during operation. This is caused by the circuit`s input signals [16]. The IDDQ approach is commonly used for end-of-production testing of electronic boards and integrated circuits. Several research demonstrate that the IDDQ test is a useful test technique. ICC testing can enhance quality and reduce production costs for CMOS ICs. Combined with traditional methods such as functional or stuck-at-fault testing, it effectively detects faults and failure mechanisms early in the production process [17].

ICC testing, which measures quiescent current, is a crucial aspect of CMOS circuit testing. It detects physical faults that cause a significant amount of current to flow in the presence

of a fault, but do not affect the output function [18]. A flaw may alter the properties of this waveform. These parameters include the current waveform width, peak value, average value, and peak time [19]. Several studies have examined transistor-level flaws in CMOS integrated circuits, including open circuit testing [20].

Figure 5 shows the open testing purpose. The defects consist of open and short circuits. Bridging errors can arise at either the logic gate`s output or its internal transistor terminals. Bridges can occur at the inter-gate level or between logic gate outputs. A bridge fault can occur between the sources and gate, drain and source, drain and gate, bulk and gate nodes, and drain and gate.

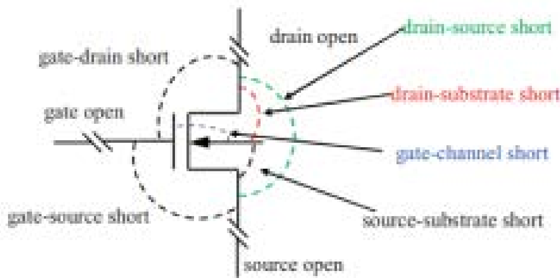


Figure 5. Open-Short Circuit Testing

V. RESULTS AND DISCUSSION

Table 1 depicts the datasheet specification for hexa-inverter IC devices that were used as experiment devices on the ATE tester. The supply current (ICC/IDD) test was performed across a voltage range of 5 V to 15 V. This was limited by tester accuracy and the inability to test IC devices that exceed the input high voltage (VIH) and higher-level input high voltage (VIHH) ranges, including the ground (GND) level. Supply voltage (VCC) level readings ranged from 5 µA to 20 µA at all temperatures, such as 25̊C.

Table 1
ICC test data specifications

Symbol	Parameter	V_{DD}(V)	T_{amb} (̊C)				Unit
			-40̊C	25̊C	85̊C	125̊C	
$I_{s(OFF)}$	OFF – state leakage current, Z & Y port	15V	-	1000	-	-	nA
		15V	-	200	-	-	nA
I_{DD}	Supply current, I_o = 0A	5V	5	5	150	150	uA
		10V	10	10	300	300	uA
		15V	20	20	600	600	uA
C_I	Input capacitance, S_n	-	-	7.5	-	-	pF

According to the ATE tester, the VIH level could only be verified between -2 V and 7 V, while the VIHH level included verification from -5 V to 15 V. The GND level could only be forced between -2 V, and 1 V. Figure 5 depicts the differences in forcing conditions at 10 V and 15 V. The average value showed that 10 V was more stable than 15 V due to VCC level forcing at 13.5 V and GND level forcing at -2.5 V. However, the VIL level could not be driven to the GND level.

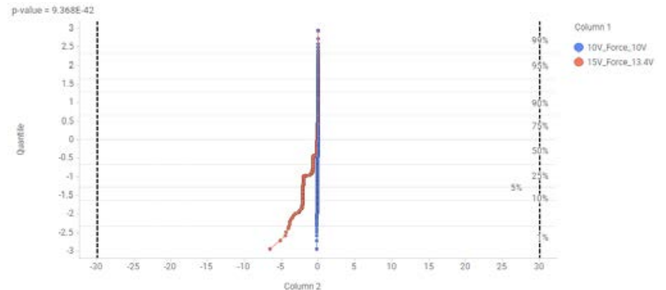
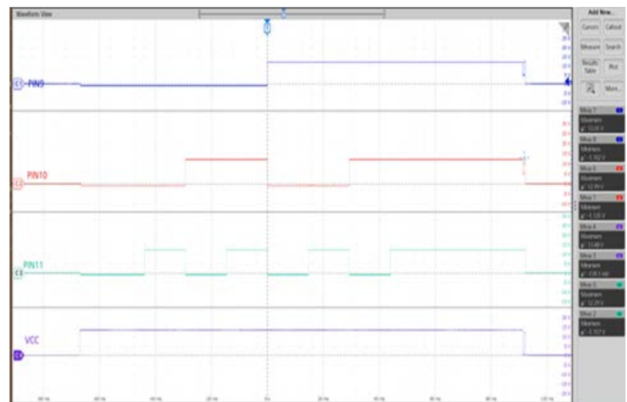
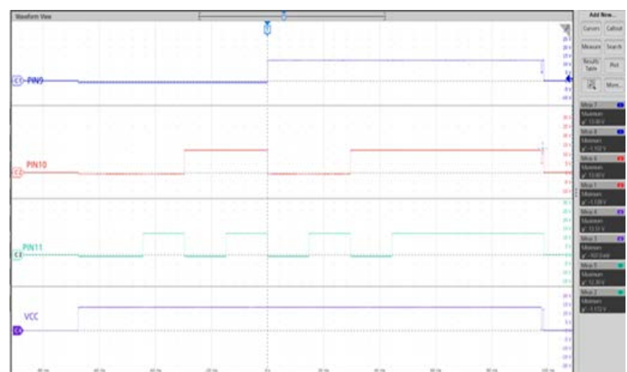


Figure 6. ICC test comparison between 10V vs 15V forcing data specification

Figure 7(b) depicts the compensation of the ICC/IDD test when forced at 15 V, as well as the conventional test program when the VCC level was forced at 13 V and the GND level was at -2.5 V. The voltage amplifier was designed using a non-inverting operational amplifier based on the IC application devices. Figure 7(a) waveform also summarizes the behavior of the input pins when the hex-inverter IC was forced according to datasheet specifications, whereby the high state was at 7 V to 12.5 V and the low state was at -1.5 V.



(a) Code “vpar_force_set” compensate the value of ISS test (A).



(b) Conventional test program forcing VCC level at 13V and GND level at -2.5V

Figure 7. ICC/IDD test

VI. CONCLUSION

Pin Electronic (PE) with level specification is a critical component of Automated Test Equipment (ATE), ensuring accurate testing of semiconductor devices. By precisely controlling and measuring voltage, current, and signal timing, PE verifies that a Device Under Test (DUT) meets functional and parametric requirements. Proper configuration of PE levels (VOH, VOL, VIH, VIL, IOH, IOL) is essential for reliable and efficient testing. With advancements in ATE

technology, PE continues to evolve, enabling higher accuracy, faster testing, and support for complex semiconductor devices in modern electronics. Understanding and optimizing PE settings enhances test efficiency, reduces yield loss, and ensures high-quality semiconductor production. Thus, this research demonstrated that some ATE testers are still under development to improve the basic testing of complex semiconductor devices while reducing production-related costs. The tester capabilities were enhanced and tested at 10V with respect to the VCC level and GND level as well as PE levels (VIH, VIHH, VIL).

In conclusion, the proposed project demonstrated the testing approach using the Automatic Test Equipment (ATE) environment while improving measurement reliability and test efficiency. The method provided enhanced accuracy while maintaining compatibility with existing hardware. For future work, further focus should be placed on improving signal integrity, reducing parasitic effects, and optimizing measurement precision for high-speed and low-power semiconductor devices.

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CONFLICT OF INTEREST

We confirm that this paper is original and was not published or does not have similarity with other papers. In the case when this paper was earlier submitted to other journal authors are obliged to inform about this.

AUTHOR CONTRIBUTION

Khairuddin Osman, T. Yasuno (Conceptualization; Formal analysis; Visualisation; Supervision)

Nur Khairunisha Kamel, Norzahirah Zainuddin (Methodology; Data curation; Writing - original draft; Resources).

REFERENCES

[1] K. Deng, H. Wang, Z. Shu, T. Gu, Y. Xiao, E. Liu, and Z. Zhao, “System-on-Chip Test and Characterization: A Review,” IEEE Transactions on Instrumentation and Measurement. 2025.

[2] S. D’Souza, M. Getz, P. Sullivan, J. Peraza, G. Veltink, and P. Van Ulsen, “Pin Electronics for Instrumentation and Automated Test Equipment: Challenges and Solutions,” IEEE European Test Symposium (ETS), pp. 1-4, 2025.

[3] I.A. Grout, “Introduction to Integrated Circuit Test Engineering,” Integrated Circuit Test Engineering: Modern Techniques, pp.1-16, 2006.

[4] B. Harvey, “A high-voltage ATE pin driver,” In Proceedings of the 1992 Bipolar/BiCMOS Circuits and Technology Meeting IEEE, pp. 234-237, 1992.

[5] P. Bhoumik, C. Bailey, and K. Chakrabarty, “Defect Analysis and Built-In-Self-Test for Chiplet Interconnects in Fan-out Wafer-Level Packaging,” IEEE 43rd VLSI Test Symposium (VTS), pp. 1-7, 2025.

[6] N. Z. P. Gifa, M. B. Rizke, S. R. Sari, N. D. Rahmawati, F. F. Yofianka, F. A. Tsaniyah, S. A. Ayu, and M. Ikaningtyas, “Human Resource Strategy Development in Facing Challenges Digital Transformation: Case Study of PT Telkom Indonesia,” Jurnal Bisnis dan Komunikasi Digital, vol. 2, no. 4, pp.12-12, 2025.

[7] R. Ruliyanta, and I. Kusuma, “Long Range Communication Radio Channel Propagation: A Review,” Journal of Telecommunication, Electronic and Computer Engineering (JTEC), vo. 17, no. 2, pp.37-42, 2025.

[8] J. Moreira, A. Papanikolaou, and J. Hesselbarth, “High-Volume OTA Production Testing of Millimeter-Wave Antenna-in-Package Modules,” IEEE Open Journal of Instrumentation and Measurement, 2025.

[9] S. Holdobin, N. Brynza, O. Tiutiunyk, O. Serhiienko, I. Sosnov and P. Samus, “Multi-Parameter Analysis of Biosignals in Long-Term Control Medical Devices Management,” 7th International Congress on Human-Computer Interaction, Optimization and Robotic Applications (ICHORA), pp. 1-7, 2025.

[10] H.V. Pandhare, “Future of Software Test Automation Using AI/ML,” International Journal of Engineering And Computer Science, vol. 13, no. 5 , 2025.

[11] S. Feng, J. Liu, R. Lai, C. Ruan, Y. Yu, L. Zhang, and T. Chen, “Productively Deploying Emerging Models on Emerging Platforms: A Top-Down Approach for Testing and Debugging,” Proceedings of the ACM on Software Engineering, 2(ISSTA), pp.1818-1840, 2025.

[12] J. C. Liu, C. H. Chen, and C. E. Wu, “A High Timing Resolution and Data Rate Pulse Generator for Automatic Test Equipment Applications,” IEEE Transactions on Instrumentation and Measurement, 2025.

[13] S. Stiltner, R. Whitehurst and E. Avers, “Sternocleidomastoid Syndrome in a Collegiate Basketball Athlete: A Case Study,” Journal of Sports Medicine and Allied Health Sciences: Official Journal of the Ohio Athletic Trainers Association, vol. 11, no. 1, pp. 9, 2025.

[14] J. Geng, R. Mandrioli, C. Q. Jiang, and M. Ricco, “Vertically Stacked Dual-Bus DC-DC Converter for Data Center High-Current Power Delivery,” IEEE Transactions on Power Electronics, 2025.

[15] I. Yasri, , A. Al-Alif, and F. Pirwanhadi, “A Security Home System Feature as a Part of Home Assistant through IoT Platform,” Journal of Telecommunication, Electronic and Computer Engineering (JTEC), vol. 17, no. 2, pp.15-21, 2025.

[16] J. Gai, H. Chen, Z. Wang, H. Zhou, W. Zhao, N. Lane, and H. Fan, “Exploring code language models for automated hls-based hardware generation: Benchmark, infrastructure and analysis,” Proceedings of the 30th Asia and South Pacific Design Automation Conference, pp. 988-994, 2025.

[17] V. Sarasa Laborda, L. Hernández-Álvarez, Hernández L. Encinas, J. I. Sánchez García, and A. Queiruga-Dios, “Study About the Performance of Ascon in Arduino Devices” Applied Sciences, vol. 15, no. 7, pp. 407 2025.

[18] S. P. Mohanty, and E. Kougianos, “iVAMS 3.0: Hierarchical-Machine-Learning-Metamodel-Integrated Intelligent Verilog-AMS for Ultra-Fast, Accurate Mixed-Signal Design Optimization’” arXiv preprint arXiv:2506.01045, 2025.

[19] Zhang, Y., Liu, W., Kou, L., Liu, Y. F., & Keimel, C. (2018). Design of a high-power MEMS relay with zero voltage switching and isolated power and signal transfer. Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC, 2018-March(c), 1974–1980.

[20] Verma, N., Gupta, K., & Mahapatra, S. (2015). Implementation Of Solid-State Relays for Power System Protection. International Journal of Scientific & Technology Research, 4(6), 65–70.

[21] Collins, E., In-Seok, J., Yong-Bin, K., & Kyung-Ki, K. (2011). A Design Approach of a Parametric Measurement Unit on to a 600MHz DCL. ISCOCC 2011, 446-449.