The Impact of Gate-Induced Drain Leakage (GIDL) on Scaled MOSFETs for Low Power Device

A.S. Mohd Zain, T.B. Ngelayang, F. Salehuddin, H. Hazura, S.K. Idris, A.R. Hanim, AM AH
Micro Nano Electronics (MiNE), Centre for Telecommunication Research and Innovation, Faculty of Electronics and Computer Engineering, Universiti Teknikal Malaysia Melaka, Hang Tuah Jaya, 76100 Durian Tunggal, Melaka, Malaysia.
anissuhaila@utem.edu.my

***Abstract*— In this research, we investigated the impact of Gate-Induced Drain Leakage (GIDL) on scaled Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) for low power application. The output of this research determined the implications of GIDL on the performance of MOSFET with various sizes that are supplied via low voltage power. The MOSFET design parameters were proposed by referring to the International Technology Roadmap for Semiconductors (ITRS), 2011 edition. SILVACO's DEVEDIT and ATLAS software was used for this research to design a device structure and obtain output characteristics. Three MOSFETs with different physical gate length and several other parameters were designed and simulated. From the extracted data, it shows that as the size of MOSFET physical gate length become smaller, the leakage current tends to be higher. Apart from GIDL current (I_{GIDL}) value, the "ON" current (I_{ON}) value and threshold voltage (V_{TH}) value also been extracted for all MOSFET designs.**

***Index Terms* - Gate-Induced Drain Leakage (GIDL); Low Power Application; Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET).**

I. INTRODUCTION

The Journal of Over four decades, semiconductor industry has undergone a various transformation in the improvement of its product. Moores' Law stated that processor speed or overall processing power for computers would double for every two years [1, 2]. It specifically states that the number of transistors of an affordable Central Processing Unit (CPU) would double for every two years [3]. The early basic concept of the integrated circuit was to pack in multiple transistors, the devices that regulate current in a circuit, into a single, tiny chip, which would almost eliminate the distance between the circuits and therefore increase the speed with which electronic instructions flow through a computer.

As the improvement of Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) develops through times, the innovation of microchips had been evolved in many forms. [4] The size of the microchips is getting smaller. As it goes smaller, it would save more production cost which will benefit the producer [5, 6].

However, one of the problems that always occur when scaling of MOSFET being conducted is the Gate-Induced Drain Leakage (GIDL) current. GIDL is a crucial issue for scaling of the MOSFET [7]. It is induced by the Band-to-Band Tunnelling (BTBT) effect in strong accumulation mode and generated in the gate-to-drain overlap region [8, 9]. The surface BTBT or GIDL increases exponentially due to the reduced gate oxide thickness [10, 11]. Thus, this project investigates the impact of GIDL on scaled MOSFETs for low power application. The result indicates that GIDL is significantly higher when the size of MOSFET physical gate length is reduced.

II. DEVICE SIMULATION PROCESS

The development of this project is divided into two phases. The first phase is on the information gathering, analysing and research on scaled MOSFET for low power application. The most important part this research phase being conducted is to familiarise the characteristics and impact of Gate-Induced Drain Leakage (GIDL) on MOSFET itself. All data and information collected are used in the analysis for the impact of GIDL on all proposed design parameters conducted.

Meanwhile, the second phase is designing process of the MOSFET. These designs were constructed by using Silvaco TCAD software. The criteria of all three designs is based on the proposed suitable parameters.

The first stage in this process is designing the MOSFET by using the DEVEDIT application. All the dimension sizes were set according to the parameters that will be tested and some fixed parameters. Then, the base region and desired impurities were being doped into the structure.

After MOSFET being designed by using the DEVEDIT application, it will then have been tested and executed in the Atlas application. In here, the desired graphs will be plotted by the Tonyplot application. From the graphs obtained, the input voltage (V_{IN}), gate-induced drain leakage current (I_{GIDL}), and threshold voltage (V_{TH}) were extracted. Finally, the analysis of the impact of GIDL on every design was carried out. The GIDL impact on all three designs is also being compared.

III. RESULT AND ANALYSIS

A. Parameter design

Table 1 shows the design parameter for three different gate lengths. The DEVEDIT application from SILVACO TCAD is used to design the MOSFET structure. The structure of designed MOSFET is shown in Figure 1-6.

B. Transfer characteristic curves

Figures 7-9 depict an overlay of drive current versus gate voltage for three different device technology. From these I-V characteristics, the value of GIDL can be obtained. The value of drain voltage is biased at 0.7 V, 0.61 V and 0.51 V for 24nm, 16 nm and 9.8 nm gate length respectively as prescribed in ITRS.

Table 1
Overall design parameters for MOSFET structure with gate length 24 nm, 16 nm and 9.8 nm.

Parameters \ Physical Gate Length (nm)	24.0	16.0	9.8
Power Supply Voltage (V)	0.70	0.61	0.51
Channel Doping (Boron) (10^{18} / cm^3)	3.7	0.1	0.1
Silicon Dioxide (SiO_2) Thickness (nm)	0.9	0.8	0.7
Junction Depth (Xj) (nm)	9.0	6.0	3.7
Source/Drain Impurities (Arsenic) (10^{19} / cm^3)	1.0	1.0	1.0
MOSFET Body Dimension (nm)	80 x 20	80 x 20	80 x 20
Source/Drain Electrode Dimension (nm)	15 x 2	15 x 2	15 x 2

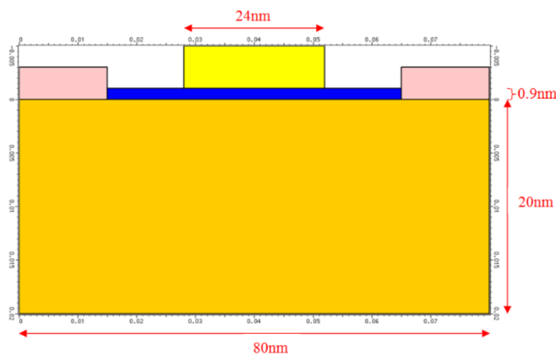

Figure 1: MOSFET structure of 24 nm gate length

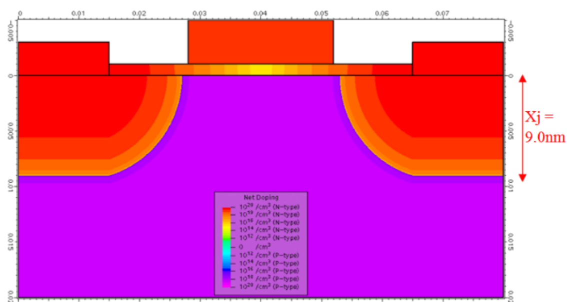

Figure 2: Contour structure with junction depth for 24 nm gate length MOSFET

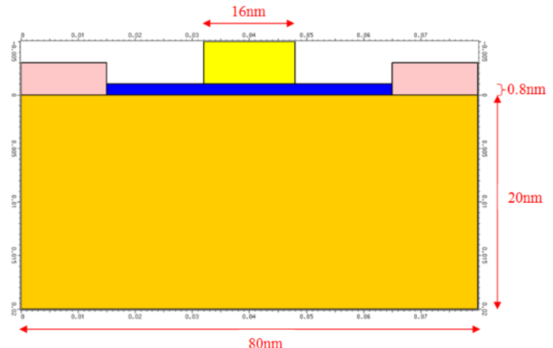

Figure 3: MOSFET structure of 16 nm gate length

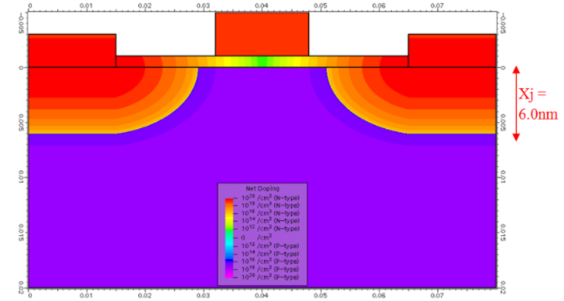

Figure 4: Contour structure with junction depth for 16 nm gate length MOSFET

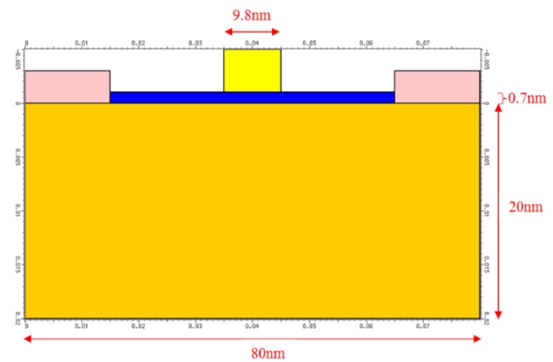

Figure 5: MOSFET structure of 9.8 nm gate length

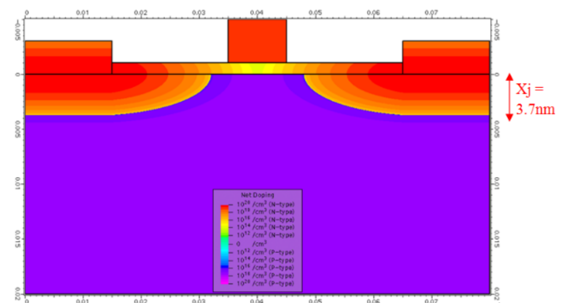

Figure 6: Contour structure with junction depth for 9.8 nm gate length MOSFET

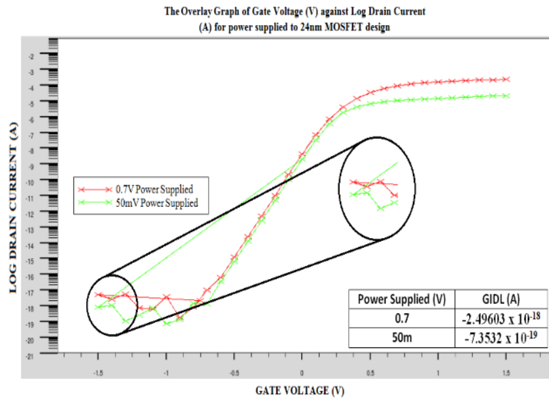

Figure 7 : Overlay of output characteristic for 24 nm gate length MOSFET with an extracted GIDL.

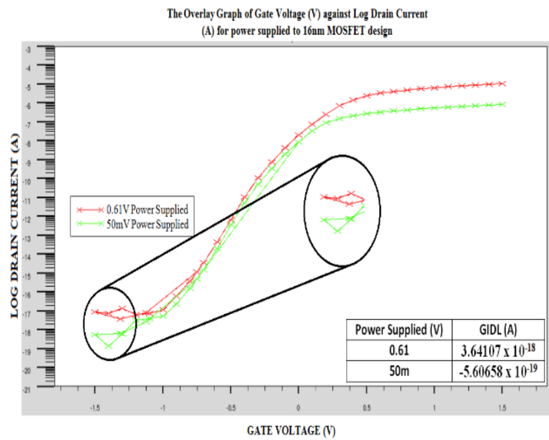

Figure 8 : Overlay of output characteristic for 16nm gate length MOSFET with an extracted GIDL.

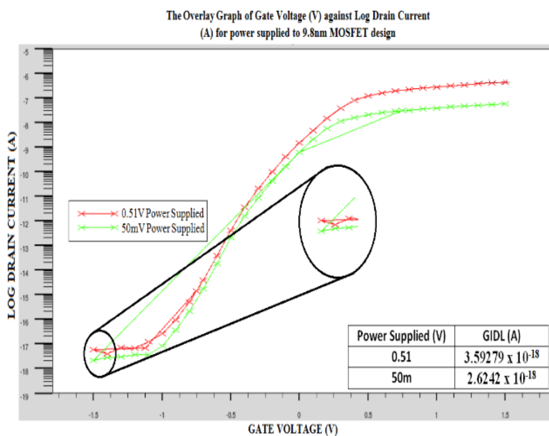

Figure 9 : Overlay of output characteristic for 9.8nm gate length MOSFET with an extracted GIDL.

Based on Figure 7-9, all gate lengths were biased at a different value of drain voltage: 0.7V, 0.61V and 0.51V accordingly. The complete results are presented in Table 2. It was observed that when the value for physical gate length is getting smaller, the "ON" current (I_{ON}) will decrease. The same situation also implies the threshold voltage (V_{TH}). However, the gate-induced drain leakage current (I_{GIDL}) will increase.

For MOSFET designs of 24 nm gate length, when it biased at 0.7 V power, the "ON" current (I_{ON}) is 2.38×10^{-4} A, GIDL current (I_{GIDL}) is 9.0×10^{-18} A, threshold voltage (V_{TH}) is 0.315 V. Meanwhile, the extracted values when supplied with 50 mV power shows the "ON" current (I_{ON}) is 2.17×10^{-5} A, GIDL current (I_{GIDL}) is 8.7×10^{-19} A, threshold voltage (V_{TH}) is 0.2 V. Comparing both the results, we can say that the "ON" current (I_{ON}) decreases when much lower power is supplied. GIDL current (I_{GIDL}) also results in decreasing value from 9.0×10^{-18} A to -8.7×10^{-19} A. Only threshold voltage (V_{TH}) showed increased value when the power supplied decreases.

Table 2
Overall output data for 24 nm, 16 nm and 9.8 nm MOSFET technology

Gate Length (nm)	24		16		9.8	
Power Supply (V)	0.7	50m	0.61	50m	0.51	50m
I_{ON} (A)	2.38×10^{-4}	2.17×10^{-5}	1.02×10^{-5}	8.07×10^{-7}	4.30×10^{-7}	5.80×10^{-8}
GIDL (A)	9.0×10^{-18}	8.7×10^{-19}	8.5×10^{-18}	6.3×10^{-19}	6.0×10^{-18}	5.0×10^{-18}
V_{TH} (V)	0.315	0.2	0.2	0.1	0.125	0.05

As for MOSFET design with 16 nm gate length, the proposed supplied power is 0.61 V. Result shows the "ON" current (I_{ON}) is 1.02×10^{-5} A, GIDL current (I_{GIDL}) is 8.5×10^{-18} A, threshold voltage (V_{TH}) is 0.2 V. When the power supplied was change to 50 mV, the "ON" current (I_{ON}) shows decrement to 8.07×10^{-7} A. GIDL current (I_{GIDL}) reading also showing decrement from 8.5×10^{-18} A to 6.3×10^{-19}. While threshold voltage (V_{TH}) decreases to 0.1 V.

On the other hand, MOSFET design with 9.8nm gate length was supplied with 0.51V power. The "ON" current (I_{ON}) is 4.30×10^{-7} A, eventually dropped to 5.80×10^{-8} A when power supplies are decreased to 50mV. Extracted GIDL current (I_{GIDL}) is 6.0×10^{-18} A increases to 5.0×10^{-18} A, when supplied with 50 mV power. Decrement from 0.125 V to 0.05 V of threshold voltage (V_{TH}) also happens.

Analysing through the increment and decrement pattern of "ON" current (I_{ON}), GIDL current (I_{GIDL}) and threshold voltage (V_{TH}) on each MOSFET design when supplied power is changed, it can be said that the "ON" current (I_{ON}) and GIDL current (I_{GIDL}) decreases when lower power is exerted on it. On the other hand, the threshold voltage (V_{TH}) increases.

However, by referring to the extracted result for the proposed power supplied to the MOSFET designs, the readings show that for MOSFET with 24 nm, 16 nm and 9.8 nm gate length, "ON" current (I_{ON}) and threshold voltage (V_{TH}) decreasing as the length of physical gate decreases, but the GIDL current (I_{GIDL}) increases as the length of MOSFET gate reduced.

Threshold voltage (V_{TH}) shifting is caused by an electrostatic field that no longer resembles the planar capacitor as the effect of device scaling. Shifting of the threshold voltage value will cause a lack in a pinch off and definitely will increase the leakage current and output conductance. Gate capacitance will change upon device scaling.

Analysis for the leakage current shows that when the MOSFET physical gate length was reduced, the GIDL current increases. It was found that the GIDL current increases by 5.56% when the physical gate length was reduced from 24 nm to 16 nm. Larger leakage value was obtained when physical

gate length was reduced from 16 nm to 9.8 nm where the GIDL current increases by 29.41%.

The huge difference on GIDL current increment in percentage especially on MOSFET physical gate length is reduced from 16 nm to 9.8 nm is due to the limiting constraints of the SILVACO TCAD software that had been used during the conduction of this project. Previous research stated that SILVACO TCAD software is not suitable to be used in simulating MOSFET with physical gate length which is lower than 15 to 12 nm.[6] Other softwares such as Synopsys' Sentaurus TSUPREM4 or Ab Initio Quantum is said to be the one that is compatible to simulate MOSFET design with extremely short physical gate length.

IV. Conclusion

Through this research, the impact of the gate induced barrier lowering (GIDL) in scaled devices have been identified. The smaller gate length experienced a major impact of GIDL. The GIDL was found not only affected by the scaled gate length, but it also contributed by the gate-drain overlapped region.

Acknowledgment

The authors would like to thank the Ministry of Higher Education (MOHE), MiNE and CeTRI, Universiti Teknikal Malaysia Melaka (UTeM) for sponsoring this research study under the research grant RACE/F3/TK3/FKEKK/F00299.

References

[1] S. T. M, "Scaling of MOSFETs," in *Indo German Winter Academy*, Digha, 2006.

[2] Ren-Ji.C, Sah C.T, IEEE Transaction on Electron Devices, 1983.

[3] J.R. Brews. (1979). IEEE Trans. Electron Dev. ED-26(11),p1696

[4] C. Fiegna et al. (June 1994). Scaling The MOS Transistor below 0.1um, IEEE Transactions on Electron Devices, Vol 41, No. 6

[5] T. Hiramoto, "Low Power and Low Voltage MOSFET," *Special issue on low power, high speed CMOS technology,* vol. 38, no. 2, p. 9, 2000.

[6] S. A. Parkle, "Design for suppression of GIDL," *IEEE Transaction on Electron Devices,* vol. 39, no. 7, p. 3, 1992.

[7] J. L. a. Y. Y.K. Fang, "Investigation of Bulk Traps Enhanced Gate Induced Leakage Current in Hf-based MOSFETs," *IEEE Electron Device Letter,* vol. 29, no. 5, pp. 509 - 511, 2008.

[8] B. C. a. L. Harrison, "Zero-power MOSFETs reduces power consumption," in *Advanced Linear Devices*, Sydney, 2007.

[9] J.-H.Y. Bum-Joon Kim, "Characteristics of Low-powered Dual MOSFET," University of Seoul, Seoul, 2011.

[10] K. Jeon, "Band-to-Band Tunnel Transistor Design and Modeling For Low Power Applications," University of California, Berkeley, 2012.