A Novel Ultra Low-Power 10T CNFET-Based Full Adder Cell Design in 32nm Technology

Mohammad Hossein Shafiabadi, Yavar Safaei Mehrabani
Sama Technical and Vocational Training College, Islamic Azad University, Islamshahr Branch, Islamshahr, Iran.
shafiabadi@iiau.ac.ir

***Abstract*—Nowadays, energy consumption is the main concern in portable electronic systems such as laptops, smart mobile phones, personal digital assistances (PDAs) and so forth. Considering that the 1-bit Full adder cell has been the determinant circuit due to its wide usage in these systems, it affects the entire performance of the electronic system. In this paper, a novel low-power and low-energy 10 transistor (10T) Full Adder cell using NAND/NOR functions based on carbon nanotube field effect transistors (CNFETs) is presented. The proposed cell showed superiority in terms of power-delay product (PDP) compared to the other cells under different simulation condition, such as power supply, temperature, load and operating frequency variations. Moreover, a Monte Carlo (MC) simulation was conducted to study the reliability of the proposed cell against manufacturing process variations (i.e. the variations of diameters of carbon nanotubes). Simulations confirmed the robustness of the proposed cell.**

***Index Terms*—Full Adder Cell; Carbon Nanotube (CNT); Low-Power; 10 Transistor; Process Variation.**

I. INTRODUCTION

Nowadays, energy consumption has become a major concern in portable electronics such as laptops, mobile phones, personal digital assistances (PDAs) and so forth. In this respect, many attempts have been made to design low-power circuits. Among the different types of circuits, the 1-bit Full Adder cell has a wide range of usage and has been used as a building block for larger circuits such as subtractor, multiplier, and divider. It has also been applied in digital filters that address the calculation unit of cash memory within the microprocessor [1] and almost anywhere in digital electronic systems. Thus, the design of a low-power Full Adder cell affects the energy consumption of the entire digital system. In this study, a novel 10 transistor (10T) cell that consumes low-energy than the previous designs is introduced. It utilises a 3-input capacitor network to realise the NOR and the NAND functions. In this study, for the first time, we have obtained the output carry of the Full Adder cell (Cout) referred to the Majority function from the output of the NAND function. Therefore, we have saved one inverter, which is equivalent to two transistors.

The carbon nanotube field effect transistor (CNFET) technology is one of the most promising successors to the traditional silicon bulk transistors, i.e. metal oxide semiconductor field-effect transistors (MOSFETs) [2]. It has an excellent low off-current and high switching speed due to ballistic movement of electrons [2]. Therefore, it can enhance the performance of the circuits. The CNFET transistor has four terminals, namely the MOSFETs named gate, source, drain and body. There are a number of carbon nanotubes (CNTs) that function as the channel of CNFET under the gate terminal. The carbon nanotubes conduct electricity between the drain and the source terminals. The threshold voltage of each CNFET is obtained using Equation (1) [3].

$$V_{th} = \frac{0.43}{D_{CNT}(nm)} \quad (1)$$

The symbol D_{CNT} denotes the diameter of each carbon nanotube existing under the gate terminal of CNFET. The diameter of CNT is obtained using the Equation (2) [3].

$$D_{CNT} \approx 0.0783 \times \sqrt{n_1^2 + n_2^2 + n_1 n_2} \quad (2)$$

Where n_1 and n_2 denote the integer pair (n_1, n_2), they referred to the chirality vector, which determines whether the CNT is a metallic or semiconductor. If n1-n2=3K (Kϵ $\mathbb{Z}$), then the CNFET is a metallic; otherwise it is a semiconductor. The structure of CNFET device is shown in Figure 1 [4].

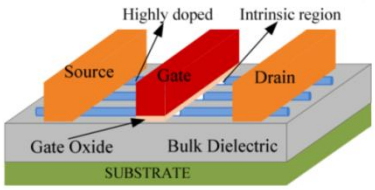

Figure 1: The CNFET device [4]

The organisation of this paper is as follows. In section II, we briefly review the previously published papers on the design of Full Adder cell. In section III, the novel 10T Full Adder cell is proposed. In section IV, the simulation results and discussion are provided. Finally, section V concludes the paper.

II. PREVIOUS WORK

In this section, we briefly review a number of Full Adder cells addressed in the literature. In fact, the pros and cons of

each design were studied. The various parameters, including the critical path of cell from inputs to the output signals and the number of transistors were considered.

The Design2 Full Adder cell is shown in Figure 2 [5]. The Design2 contains 8 transistors and 7 capacitors. The intermediate capacitor ($2C_2$) results in the Design2 is considered as noise sensitive. In other words, if a small noise occurs at this node, then the SUM signal will fail to function. The critical path of Design2 consists of only three transistors.

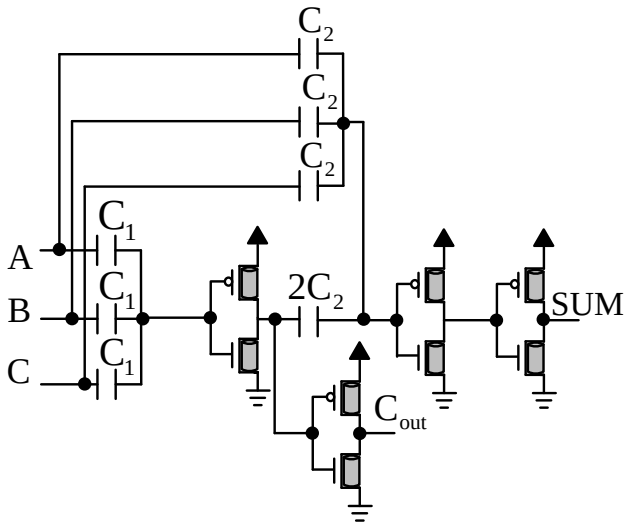

Figure 2: The schematic of Design2 cell [5]

The 3c2c Full Adder cell is shown in Figure 3 [6]. It is the enhanced version of the Design2 cell. It contains 5 capacitors and 8 transistors. In fact, the 3c2c cell has a lesser number of capacitors compared to the Design2 cell. Its critical path consists of three transistors. The 3c2c cell has noise sensitivity issue, similar to in Design2 cell.

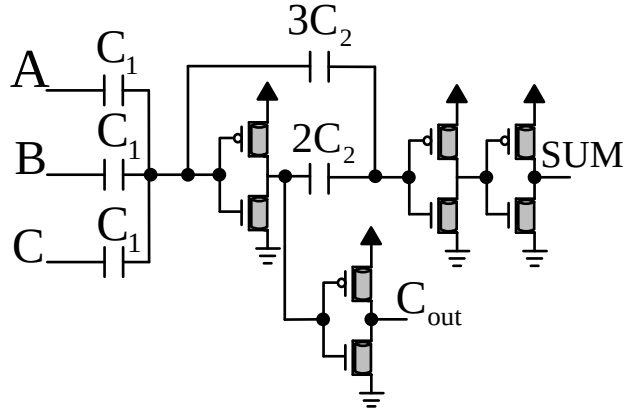

Figure 3: The schematic of 3c2c cell [6]

The schematic of 12T Full Adder cell is shown in Figure 4 [7]. It contains 12 transistors and a 3-input capacitor network. There is a multiplexer that applies either the NOR or the NAND functions to the $\overline{SUM}$ signal. The selected line of multiplexer is connected to the voltage of the capacitor network. It is worth to notice that the critical path of this cell consists of three transistors.

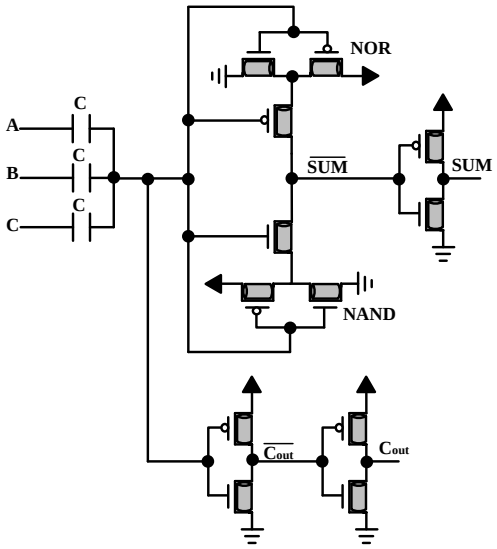

Figure 4: The schematic of 12T cell [7]

The schematic of FSFA2 Full Adder cell is shown in Figure 5 [8]. It contains 22 transistors and a 2-input capacitor network. The FSFA2 has lesser number of capacitors compared to the previous designs. The presence of inverter gates at the output nodes guarantees the rail-to-rail signals. Its critical path consists of four transistors, which causes a long propagation delay. The FSFA2 applies pass transistors at the internal nodes to decrease the power consumption.

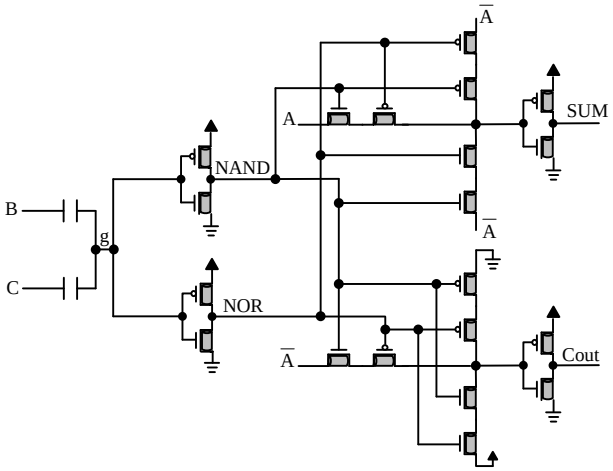

Figure 5: The schematic of FSFA2 cell [8]

The schematic of SyMuT Full Adder cell is shown in Figure 6 [9]. The SyMuT design has a fully symmetric structure with 14 transistors and a 3-input capacitor network. The output signals of SyMuT are rail-to-rail and their critical path consists of three transistors only.

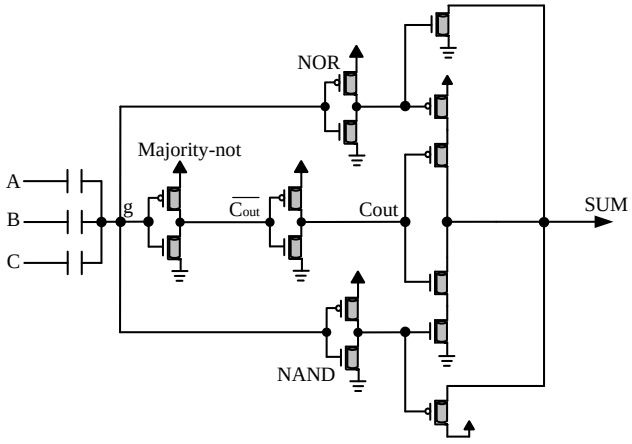

Figure 6: The schematic of SyMuT cell [9]

III. THE PROPOSED FULL ADDER

The block diagram and the transistor level implementation of the proposed 10T Full Adder cell are shown in Figure 7 (a) and (b), respectively. The proposed cell applies a capacitor network to realize NAND and NOR functions [10]. Then using these functions, the SUM and C_{out} signals are produced. The proposed cell contains a capacitor network, four inverter gates and two NCNFET pass transistors. The inverter gates at the output nodes guarantee full voltage swing outputs. It is one of the important characteristics of the cell in driving the following cells in cascaded manners, such as the ripple carry adders. The characteristics of transistors utilised in Figure 7 are tabulated in Table 1. This table reports the diameter of carbon nanotubes (CNTs), the threshold voltage, and the number of CNTs (tubes) for each individual transistor.

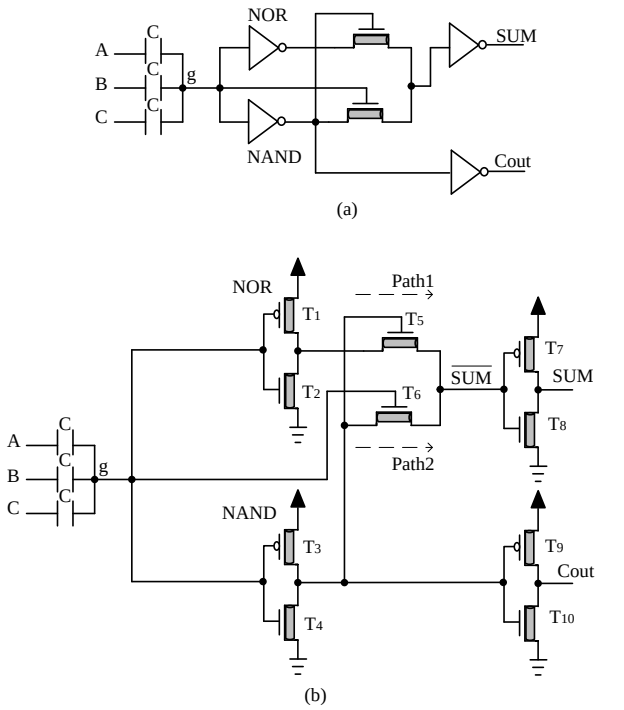

Figure 7: The proposed Full Adder cell (a) Block diagram (b) Transistor level implementation

Table 1
Characteristics of transistors of the proposed cell

Tr. No.	Tr. Type	Diameter (nm)	No. of Tubes	$\|V_{TH}(v)\|$
T1	PCNFET	0.783	5	0.54
T2	NCNFET	2.114	1	0.20
T3	PCNFET	2.114	1	0.20
T4	NCNFET	0.939	2	0.45
T5	NCNFET	1.409	7	0.30
T6	NCNFET	4.071	5	0.10
T7	PCNFET	1.174	8	0.36
T8	NCNFET	1.409	13	0.30
T9	PCNFET	1.957	3	0.21
T10	NCNFET	1.017	2	0.42

In the following, we discuss how the NAND and the NOR functions are realized using the inverter gates in the proposed cell. There are eight combinations of inputs for a 1-bit Full Adder cell. For simplicity, we use the logical summation of inputs ($\sum$in) to decrease the number of combinations of inputs to only four cases ($\sum$in=0, 1, 2, 3). For instance, if one of the input signals is logical '1', then we use symbol $\sum$in=1. This technique causes a decrease in the rows of the true table of the Full Adder cell. Table 2 shows how the inverter gates of the proposed cell produce the NAND and the NOR functions at VDD=0.45V. We provide a circuit analysis for one combination of inputs, i.e. $\sum$in=2. The other cases of inputs can be analysed in the same way. If $\sum$in=2, then the potential of node g=0.3V is based on superposition theorem. This potential results in turning the T_2 transistor on and the T_1 transistor off. The T_2 transistor pulls down the output of the NOR function to the ground level. Therefore, the output of the NOR function becomes a logical '0'. On the other hand, 0.3V has the potential to turn both T_3 and T_4 transistors on. In this case, the voltage drops between the gate and source terminals (V_{gs}) of T_3 and T_4 transistors are -0.15V and 0.3V, respectively. It is worth to note that -0.15V is more close to the threshold voltage of T_3 than 0.3V to the threshold voltage of T_4. In conclusion, T_3 is turned on more than the T_4, which consequently causes the output voltage of NAND function to be 0.27V, which is more than the half of the power supply voltage (VDD/2=0.22V).

Table 2
The operation of NOR and NAND functions at V_{DD}=0.45V

$\sum$in	g (v)	T1	T2	NOR (v)	T3	T4	NAND (v)
0	0	ON	OFF	0.45	ON	OFF	0.45
1	0.15	ON	ON	0.13	ON	OFF	0.45
2	0.3	OFF	ON	0	ON	ON	0.27
3	0.45	OFF	ON	0	OFF	ON	0

We provide a circuit analysis of the last stage inverters to show how the SUM and C_{out} signals are produced. Table 3 tabulates the amount of voltages for different nodes of the proposed cell. It also shows which path is active (√) and which is not (x) in the presence of different input combinations. Once again, we only consider the case $\sum$in=2. The same way can also be used to analyze other cases of inputs. As shown in Table 2, the potential of the node g, the NAND and the NOR functions are 0.3V, 0.27V and 0V, respectively, when $\sum$in=2. The voltage of node g results in turning T_6 on. In conclusion, path2 becomes active and passes the output of the NAND function to the $\overline{SUM}$ signal. In fact, the voltage of $\overline{SUM}$ signal

reaches to 0.24V. Moreover, the 0.27V potential of the output of the NAND function is not high enough to turn on the T_5 transistor. It results in path1 to become inactive. In conclusion, the following inverter produces logic '0' at the SUM node. On the other hand, C_{out} becomes logic '1', which is the proper value for this case of inputs. With this technique, we succeeded for the first time to obtain C_{out} signal (Majority function) from the output of NAND function, which was not possible prior to this study.

Table 3
The operation of the proposed cell at V_{DD}=0.45V

∑in	g (v)	T5	T6	Path1	Path2	$\overline{SUM}$ (v)	*SUM*	*Cout*
0	0	ON	OFF	√	x	0.35	0	0
1	0.15	ON	OFF	√	x	0.13	1	0
2	0.3	OFF	ON	x	√	0.24	0	1
3	0.45	OFF	ON	x	√	0	1	1

Figure 8 illustrates the output waveforms of the proposed Full Adder cell in the presence of variant input combinations. The output waveforms confirm that the outputs of the proposed cell are full swing. Figure 8 also shows how the Majority function (C_{out}) is realized from the output of NAND function.

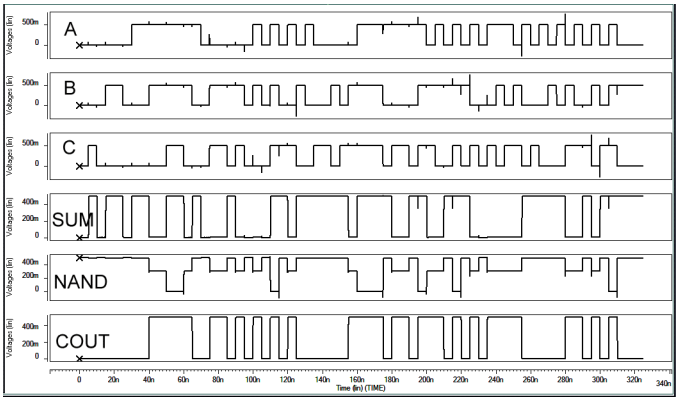

Figure 8: The input/output waveforms of the proposed cell

Table 4 summarizes the characteristics of different Full Adder cells, including the number of transistors (#Tran), the number of capacitors (#Cap), the total number of elements and the critical path of each cell. The total number of elements is the multiplication of the number of transistors and capacitors. The proposed cell has the least number of elements and its critical path contains only three transistors.

Table 4
The characteristics of different Full Adder cells

Design	Reference	#Tran.	#Cap	Total Elements	Critical Path
Design2	[5]	8	7	15	3
3c2c	[6]	8	5	13	3
12T	[7]	12	3	15	3
FSFA2	[8]	22	2	24	4
SyMuT	[9]	14	3	17	3
Proposed	[Present]	10	3	13	3

IV. Simulations and Discussions

In this section, we run different computer simulations using Synopsys HSPICE tool to study the merits of the different cells. The compact SPICE model for 32nm CNFET technology was used [11, 12]. This model considers SB effects, parasitics, including the CNT, source/drain, and gate resistances and capacitances, and CNT charge screening effects. Some important parameters of the CNFET model with their values are tabulated in Table 5. Moreover, we fed inputs using the output of buffers in order to have more realistic inputs. Further, the standard fan out of four inverters (FO4) was used at the output nodes as the load.

Table 5
Some parameters of CNFET model [11, 12]

Parameter	Value	Description
$\mathbf{L_{ch}}$	32nm	Physical channel length
$\mathbf{L_{geff}}$	100nm	The mean free path in the intrinsic CNT channel
$\mathbf{L_{ss}}$	32nm	The length of doped CNT source-side extension region
$\mathbf{L_{dd}}$	32nm	The length of doped CNT drain-side extension region
$\mathbf{K_{gate}}$	16	The dielectric constant of high-K top gate dielectric material
$\mathbf{T_{ox}}$	4nm	The thickness of high-K top gate dielectric material
$\mathbf{C_{sub}}$	40pF/m	The coupling capacitance between the channel region and the substrate
Efi	6ev	The Fermi level of the doped S/D tube

For the first simulation, we studied the operation of the circuits against various power supplies at 100MHz operating frequency, load of FO4 and room temperature (27°C). The range of the power supply varied from 0.5V to 0.4V. The results of the simulation are listed in Table 6. The bold-faced numbers indicate the best performance. Based on Table 6, proposed cell has the lowest power delay product (PDP). It compromises properly between the power consumption and the delay parameters. At a low power supply, such as 0.4V, the Design2, FSFA2 and SyMuT cells failed to function. However, the proposed cell performed well at all power supplies. The proposed cell overcomed other cells in terms of PDP. For instance, at 0.5V $V_{DD,}$ the proposed cell was about 53%, 61%, 55%, 17% and 55% more efficient in comparison to Design2, 3c2c, 12T, FSFA2 and SyMuT.

Temperature variation affects the threshold voltage, saturation velocity and carrier mobility of a CNFET transistor. Therefore, it is very useful that we study the efficiency of the designs in the presence of ambient temperature variations. Simulations were conducted in the vast range of temperatures, ranging from 0°C to 60°C at 100MHz operating frequency, 0.5V V_{DD} and load of FO4. The simulation results are shown in Figure 9. The results confirmed the superiority of the proposed cell at all temperatures. In fact, not only that the proposed cell has the lowest PDP, but also its PDP increased gradually with the increase of the temperature. The 3c2c cell was the worst cell due to the large energy consumption compared to the other designs.

Driving capability is another important metric for a design. It refers to how well a circuit can operate in the presence of large loads. The variant loads were applied to the output of

circuits under consideration, which ranged from 0.5fF to 0.8fF. The results are illustrated in Figure 10. Figure 10 clarifies that the proposed cell consumed the lowest PDP in comparison to the other cells at all loads. Based on Figure 10, the 3c2c and SyMuT cells have the highest PDP.

Table 6
Performance metrics against power supply variation

Design	Power (E-6 W)	Delay (E-12 S)	PDP (E-17 J)
Vdd=0.5V			
Design2	0.45306	203.72	9.2299
3c2c	0.52276	215.09	11.244
12T	0.32066	302.03	9.6848
FSFA2	0.07484	698.49	5.2278
SyMuT	0.10886	880.13	9.5814
Proposed	0.14195	303.54	**4.3089**
Vdd=0.45V			
Design2	0.32139	318.24	10.228
3c2c	0.34371	252.70	8.6854
12T	0.24876	401.63	9.9909
FSFA2	Failed	Failed	Failed
SyMuT	0.091196	4728.8	43.124
Proposed	0.088959	442.18	**3.9336**
Vdd=0.4V			
Design2	Failed	Failed	Failed
3c2c	0.24313	500.89	12.178
12T	0.18960	1330.6	25.229
FSFA2	Failed	Failed	Failed
SyMuT	Failed	Failed	Failed
Proposed	0.057119	1094.9	**6.2538**

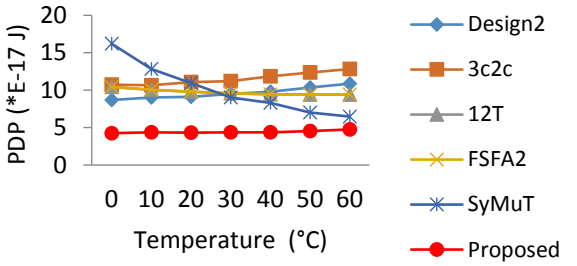

Figure 9: PDP versus temperature (supply voltage=0.5V, frequency= 100MHz, Cload= FO4)

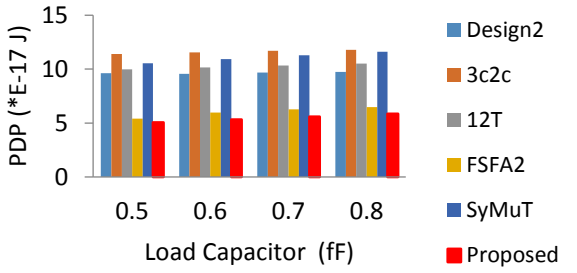

Figure 10: PDP versus output load capacitor (supply voltage= 0.5V, frequency= 100MHz)

In order to study the efficiency of the proposed cell against the frequency changes, another simulation was run at 0.5V power supply, 0.5fF load and room temperature. Both the low and high frequencies were applied to the circuit. 100MHz was applied for the low frequency and 500MHz was applied for the high frequency. The simulation results are shown in Figure 11. The results illustrate that the proposed 10T cell has the lowest PDP, while the SyMuT design has the highest frequency. Therefore, the proposed cell can be used effectively in the applications with low-energy and high-speed operation.

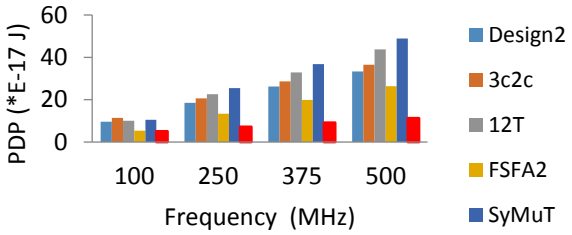

Figure: 11. PDP versus input operating frequency (supply voltage= 0.5V, Cload= 0.5fF)

The process variation of CNFETs negatively affects the performance of devices and circuits. Currently, the diameter of CNTs cannot be tuned exactly in the fabrication process of CNFETs [13]. The variant diameters result in the variant threshold voltage for CNFET device. Therefore, it is very important to study the performance of circuits in the presence of process variation. The Monte Carlo (MC) simulation with a reasonable number of 30 iterations has been used for this purpose. If a circuit functions well for all 30 iterations, there is a 99% possibility that over 80% of all of the probable component values act properly. The diameter distributing is assumed as Gaussian with 6-sigma distribution [14]. A standard deviation from the mean in the range of 0.04nm to 0.2nm was taken into account [15]. The simulation results are tabulated in Table 7. This table shows that the proposed cell is reliable against the process variations of CNTs.

Table 7
Parameter variations against the deviations of the diameters of CNTs

Diameter Deviations (*nm*)	0.04	0.08	0.12	0.16	0.2
Delay Variation (E-10)	0.659	1.06	2.932	9.764	22.504
Power Variation (E-7)	0.098	0.188	0.281	0.386	0.502
PDP Variation (E-17)	0.589	1.299	4.52	15.035	36.707

V. CONCLUSION

A novel low-energy and process variation tolerant NAND/NOR based 10T Full Adder cell was introduced using carbon nanotube field effect transistors (CNFETs) in this paper. In order to produce the output carry (C_{out}) or the Majority function, we used the output of NAND function. In fact, for the first time, the Majority function was realized from the NAND function. This technique has resulted in transistor count saving. Comprehensive simulations were performed to scrutinize the performance of cells. The power supply, temperature, load and frequency variations were considered. All simulations confirmed the superiority of the proposed 10T cell compared to other cells. Moreover, Monte Carlo simulation was conducted to study the robustness of the proposed cell against diameter variations of carbon nanotubes. Results indicated the robustness and reliability of the proposed Full Adder cell in the presence of process fluctuations.

ACKNOWLEDGMENT

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