Process Parameter Optimisation for Minimum Leakage Current in a 22nm p-type MOSFET using Taguchi Method

Afifah Maheran A.H.[2], Menon P.S.[1], I. Ahmad[3], F. Salehuddin[2], A.S. Mohd Zain[2]
[1]*Institute of Microengineering and Nanoelectronics (IMEN),*
Universiti Kebangsaan Malaysia (UKM), 43600 Bangi, Selangor, Malaysia.
[2]*Centre for Telecommunication Research & Innovation (CeTRI), Faculty of Electronic & Computer Engineering (FKEKK),*
Universiti Teknikal Malaysia Melaka (UTeM), Hang Tuah Jaya, 76100 Durian Tunggal, Melaka, Malaysia.
[3]*Centre for Micro and Nano Engineering(CeMNE), College of Engineering,*
Universiti Tenaga Nasional (UNITEN), 43009 Kajang, Selangor, Malaysia.
afifah @utem.edu.my

Abstract*—In this research paper, the effects of variation on the process parameters were optimised while designing a nano-scaled p-type MOSFET (metal-oxide-semiconductor field-effect transistor) planar device for 22 nm technology. The aim of this procedure is to meet the minimum leakage current (I_{OFF}) by optimising the process parameters as leakage current. It is one of the characteristics that must be taken into account for device functionality. The gate structure of the device consists of Titanium dioxide (TiO_2) that functions as the high permittivity material (high-k) dielectric and Tungsten silicide (WSi_x) metal gate, where it is deposited on top of the TiO_2 high-k layer. The fabrication process was designed using an industrial-based numerical simulator. This simulator was then aided in design with the L9 Taguchi's orthogonal array method to optimise the process parameters to achieve the best combination of the process parameters with the lowest leakage current. The objective is to obtain I_{OFF} values using Smaller-the-Better (STB) signal-to-noise ratio (SNR). The results of the factor effect on the SNR clearly shows that the Halo implantation tilting angle has the greatest influence with 52.47% in minimising the leakage current of the device where the implantation tilting angle is 35°. It is followed by the Halo implantation dose with 34.23% effect, gate oxide growth annealing temperature was ranked third at 12.29% effect and metal gate annealing temperature has the least influence with 1.01%. The final results in characterising and modelling the process parameters of the 22nm PMOS device technology with reference to the prediction by the International Technology Roadmap for Semiconductors (ITRS) succeeded, where the result of the I_{OFF} value was lower than the predicted value which is less than 100 nA/μm.

***Index Terms*—Taguchi Method; 22 nm p-Type MOSFET Technology; Leakage Current.**

I. INTRODUCTION

Designing a nanoscale device with the lowest leakage current is crucial since it is a major contributor to the total integrated circuit (IC) power. With the intention to achieve higher integration density and performance, complementary metal-oxide-semiconductor (CMOS) devices have been aggressively scaled down. However, continuous variation in the process parameters can lead to an increase in the transistor leakage current. This situation happens due to the reduction of the gate channel length, which results in a closer gap between the drain and the source of the scaled devices, leading to short channel effects [1]. This situation is worsened since scaling the gate length is proportional to the reduced thickness of gate oxide. With the silicon dioxide (SiO_2) gate dielectric layer thickness reaching its scaling limits, researchers have been exploring and discovering several alternatives, such as the introduction of high permittivity (high-k) gate dielectric as well as the usage of a metal gate as an alternative to the poly-silicon gate structure. This has also been one of the major challenges for further downscaling besides the management of process variation to keep the planar CMOS devices on track for the 20 nm node technology [2],[3].

Therefore, statistical process variations on the parameters of the fabrication process play a major role in future technology scaling and has been continuing throughout the semiconductor history [4],[5]. It has been reported that the process variation, such as variation associated with implants and anneals, pocket implants and tiling angle are one of the subjects that plays a significant role in the future technology scaling. Moreover, there has been a track record since 1961 where the first discussion of random variation in semiconductor device was made by Shockley and extended to MOS devices developed by Keyes in 1975 [5].

Hence, accurate estimation of variability in the process parameters of scaled devices is extremely important to design a perfect nanoscale transistor with minimum leakage current. Besides the dependence on the flat-band voltage (V_{fb}) and the supply voltage (V_{dd}), there is a number of leakage mechanisms contributing to the total leakage current in a device. They depend differently on the transistor geometry, such as the gate length (L_g), oxide thickness (T_{ox}), and doping profile. These leakage components contribute to the increase of the total leakage even though each parameter is considered to be independent of each other. In this case, the distribution is assumed to be Gaussian, and among these components, the I_{OFF} is reported to be the most sensitive to the parameter variation [6]. The prediction made by the International Technology Roadmap for Semiconductors (ITRS) gives a

good guidance in scaling down the size of the CMOS transistor by providing detailed characteristics of the robust nano-scaled CMOS device.

In this experiment, a model of 22 nm high-k/metal gate which utilises the TiO_2/WSi_x gate structure of planar PMOS device has been designed and simulated using an industrial-based simulation tool. Our previous work in optimising the fabrication process parameters on CMOS devices has been reported in various publications [7][8][9]. Therefore, we are motivated to continue our research by optimising the process parameter variations to achieve minimum leakage current (I_{OFF}) on PMOS devices. The process parameter variations have been verified with L9 orthogonal array of Taguchi method. The Taguchi method is a reliable method in optimising the device process parameters with less number of experiments as it is able to predict the optimum result of the process parameter combination as well as reduce the time consumption. It is also able to ensure the output is in the tolerable quality range, and finally achieve a robust design [10]. The aim of the experiment is to design the device with a minimum I_{OFF} as in the ITRS prediction for 22 nm gate length p-type MOSFET (PMOS) transistor, where the maximum value for I_{OFF} is limited to 100 nA/µm [11].

II. EXPERIMENTAL METHODOLOGY

A. Fabrication and Device Characterisation Process Using ATHENA and ATLAS tools

Figure 1 shows the process flow of the experiment in designing and optimising the process parameter of a 22nm PMOS planar structure model.

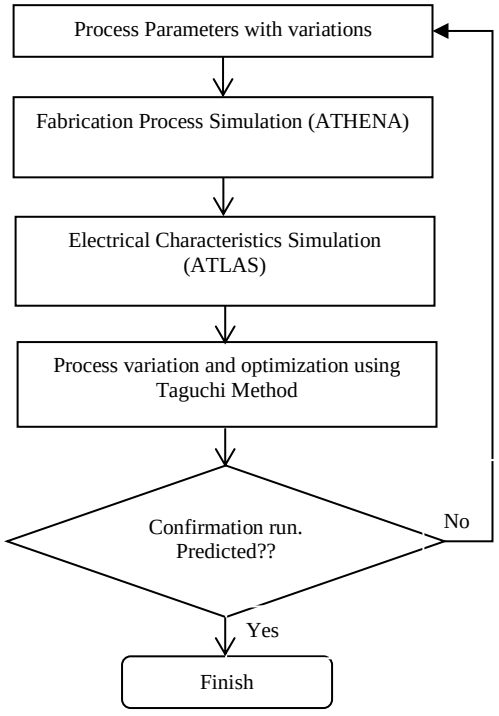

Figure 1: Flow chart of the variability process analysis

The details of virtual fabrication in designing the 22 nm PMOS planar structure device are summarised as follows. The sample used in this experiment is a <100> orientation of p-type silicon substrate. N-wells were firstly created by developing a 200Å oxide screen on wafers followed by phosphorus doping with a dosage of $4.5x10^{11}$ atom/cm^2 and it was annealed. The next step was to produce a Shallow Trench Isolator (STI) structure, by depositing an oxide layer with the thickness of 130Å and then a 1500Å nitride layer, followed by the growth of a sacrificial oxide layer (PSG) with the temperature of 900°C. This step was completed by an etching process. The next process was to develop a layer of gate oxide with dry oxygen diffusion and conduct the annealing process with the temperature of 900°C. The Boron Difluorite (BF_2) with dosage of $1.75x10^9$ atom/cm^2 was implanted for the threshold-adjustment implantation procedure. Then, high-k layer of TiO_2 (dielectric permittivity = 80) was deposited for a thickness of 2 nm and this was being etched to produce a 22 nm gate length. The deposition of WSi_x metal as the metal gate structure then took place with a thickness of 53 nm. The halo structure was implanted by phosphorus with a dose of $2.0x10^{10}$ atom/cm^2 and tilt angle of 40°. Then spacers were formed followed by source-drain implantations with boron implantation dose. The next process was the PMD development with 0.015 µm Borophosphosilicate Glass (BPSG) layer followed by the compensation implantation process with phosphorous dose. Lastly, the aluminium layer was deposited to form the metal contact for the source and drain, and at this point the device was completely fabricated. Then, the transistor underwent electrical characteristic measurement using ATLAS module in order to study the leakage current characteristics with reference to ITRS. The planar structure and doping profile of 22nm TiO_2/WSi_x PMOS device is shown in Figure 2 and Figure 3 respectively.

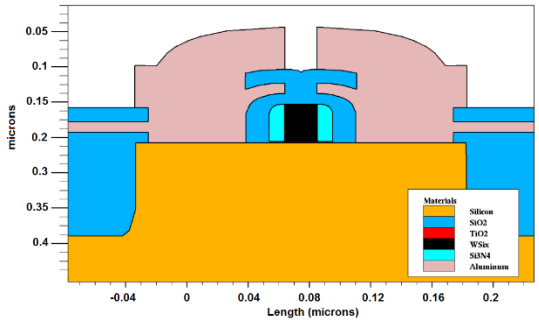

Figure 2: Completed PMOS transistor with 22 nm gate length

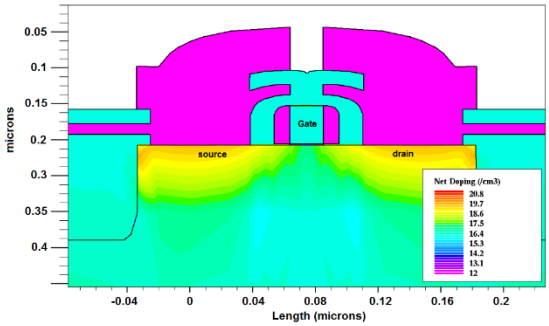

Figure 3: The doping profile of the 22 nm gate length PMOS transistor

B. Process Variation and Optimization using Taguchi Method

Variation in fabrication process parameters (factor) is now becoming one of the major roles in future technology scaling. Since this experiment is a continuation from our previous research that studied other characteristics, four process parameters were selected to study the variability effect. In this study, three levels of each factor and two noise factors containing two levels were added to complete the L9 orthogonal array analysis structure. In total, there were 36 combination simulation runs to complete the variability process recommended by Taguchi Method, and finally to discover the best combination level of process parameters in designing the 22 nm PMOS planar device.

In this experiment, the process parameters examined were the Halo implantation dose, Halo implantation tilting angle, gate oxide growth annealing temperature and the metal gate annealing temperature. While the noise factors were Sacrificial Oxide Layer (PSG) annealing temperature and the BPSG layer annealing temperature. The noise factors were included in order to get a more accurate design.

The Halo structure has a local dopant pocket in highly dopant dose placed next to the source and drain junctions, which is called the Halo Implant. The halo structure was implemented in order to reduce short channel effects, for example, the subsurface punch-through [12]. The gate oxide gives a better Short Channel Effect (SCE) [13]. Since the thickness of oxide is not easily scaled down by the scaling factor, there is a need to change the gate oxide thickness (T_{ox}). The variation of the gate oxide thickness was conducted by adjusting the annealing temperature. The use of metal gates is the suppression of polysilicon gate depletion and a good compatibility with high-k dielectric materials [14].

The range value of the selected process parameters is varying one by one so that it will be in range of ITRS prediction, which is ±12.7%. The minimum and maximum result is considered as level 1 and level 3 respectively, while level 2 as a middle value resulted from simulation result in Part A. Then, the Taguchi method was implemented with orthogonal array to get the optimum parameter. The details of the process parameters and noise factors are listed in Table 1 and Table 2 respectively. Table 3 shows the experimental layout of the L9 Taguchi orthogonal array method [15].

Table 1
Process Parameters

Factor	Process Parameter	Unit	Level 1	Level 2	Level 3
A	Halo Implantation dose	Atom/cm^2	1.5 x10^{10}	2.0 x10^{10}	2.5 x10^{10}
B	Halo Implantation tilting angle	Degree	35	40	45
C	Gate Oxide growth annealing temperature	°C	890	900	910
D	Metal gate annealing temperature	°C	840	850	860

Table 2
Noise Factors

Symbol	Noise Factor	Level 1	Level 2
		°C	
X	Sacrificial Oxide Layer	900 (X_1)	905 (X_2)
Y	BPSG	800 (Y_1)	805 (Y_2)

Table 3
L9 Taguchi Experimental Layout

Exp. No.	Process parameter			
	Halo Implantation	Halo Implantation tilting angle	Gate Oxide growth anneal	Metal gate anneal
1	A_1	B_1	C_1	D_1
2	A_1	B_2	C_2	D_2
3	A_1	B_3	C_3	D_3
4	A_2	B_1	C_2	D_3
5	A_2	B_2	C_3	D_1
6	A_2	B_3	C_1	D_2
7	A_3	B_1	C_3	D_2
8	A_3	B_2	C_1	D_3
9	A_3	B_3	C_2	D_1

III. RESULT ANALYSIS AND DISCUSSION

A. Process Variations Analysis

The proses parameter variation was conducted based on the experimental combinations in Table 3, and the simulation results of the device for I_{OFF} is listed in Table 4. On top of that, the goal of this experiment was to achieve the minimum I_{OFF} as possible with reference to the ITRS projection.

Table 4
I_{OFF} Simulaion Results for PMOS Device

Exp. No	I_{OFF} (nA/μm)			
	X1Y1	X1Y2	X2Y1	X2Y2
1	11.6579	12.3213	11.6526	12.3157
2	13.2732	14.0396	13.2672	14.0333
3	19.5786	20.7195	19.5704	20.7109
4	10.0462	10.6726	10.0417	10.6679
5	13.6378	14.3949	13.6317	14.3885
6	14.4003	15.2370	14.3939	15.2303
7	9.83749	10.4297	9.83282	10.4248
8	10.8553	11.5370	10.8506	11.5320
9	11.9361	12.6022	11.9304	12.5963

When optimising the process parameters and choosing the best combination of the parameter to achieve the minimum I_{OFF}, there are some conditions that must be taken into account. In this experiment, Signal-to-Noise Ratio (SNR) analysis is used to identify the optimum process parameters. Since the target in this experiment is to get a minimum I_{OFF}, therefore the goal is to optimise the process parameters device using signal-to-noise ratio (SNR) of Smaller-the-Better [15]. The SNR (Smaller-the-Better), η_{STB} can be expressed as;

$$\eta_{STB} = -10\log_{10}\left(\frac{1}{n}\sum_{i=1}^{n} y_i^2\right) \quad (1)$$

where n is the number of tests and y_i is the experimental value of the leakage current.

Once the type of analysis is identified, the first condition is to determine the highest Signal-to-Noise Ratio (SNR) value for each level of the process parameter based on the simulation results. From that, the highest SNR value for each process parameter level can be selected as the possible level to achieve the experiment's goal. Analysing the factor effect percentage on SNR is important as it indicates the priority of a process parameter to reduce variation. A larger SNR value indicates better characteristic quality and shows greater influence of the factor on the device performance.

The second condition is to determine the dominant factor of the design from the analysis of variance (ANOVA) result. In ANOVA analysis, the highest percentage of factor effect on variance indicates that the factor is a dominant factor and the factor will result in the most sensitive effect and greatest influence to the process variation. Thus, variability on the dominant factor must be taken seriously.

Finally, once the selecting of the process parameters have been made, the selected level from the analysis will be then simulated again with respect to the noise factor in order to achieve the optimal design. By applying the formula given in Eq. (1) the η_{STB} for the device is calculated and summarised as in Table 5. Since the experimental design is orthogonal, the effect of each process parameter on the SNR at different levels can be separated out. The factor effect percentage using ANOVA is listed in Table 5 as well.

Table 5
SNR Response for the I_{OFF}

Factor	SNR (STB), dB			Factor Effect on Variance (%)
	L1	L2	L3	
A	156.54	157.78	159.04	34.23
B	159.33	157.79	156.24	52.47
C	158.01	158.40	156.95	12.29
D	157.90	157.92	157.54	1.01

As mentioned before, the first condition in optimising the device process parameters' is to achieve the best process combination identified by the highest SNR value on each factor level. Based on the SNR (STB) data in Table 5, it shows that the highest SNR value for Factor A is at level 3 with SNR of 159.04 dB, Factor B at level 1 with SNR of 159.33 dB, while Factor C is at level 2 with 158.40 dB and lastly for Factor D, the SNR value is 157.92 dB at level 2.

The step continues with the second condition by identifying the largest percentage of the factor effect on variance as it is the most influential factor in determining the dominant factor in achieving minimum I_{OFF}. It is clearly shown that Factor B contributes the highest influence of factor effect on variance in minimising the leakage current of the device with percentage of 52.47%. Therefore, Factor B, which is Halo implantation tilting angle can be stated as the dominant factor. With reference to Table 5, the factor effect graph for the SNR (STB) can be plotted as shown in Figure 4.

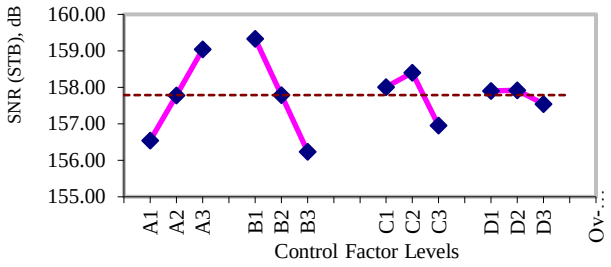

Figure 4: SNR (STB) graph

Referring to Fig. 4, from the left, the slopes correspond to the process parameters of Halo Implantation dose (Factor A: A_1, A_2, A_3), Halo Implantation tilting angle (Factor B: B_1, B_2, B_3), Gate Oxide growth annealing temperature (Factor C: C_1, C_2, C_3) and Metal gate annealing temperature (Factor D: D_1, D_2, D_3). The slope of each factor corresponds to the factor effect that influences each process parameter. As can be seen in Fig. 4, Factor B contributes the highest effect as the slope resulted in a large difference between each level of the factor and this is confirmed that the factor can be considered as a dominant factor of the experiment.

B. Confirmation of Optimum Factor

Based on all the information gathered, the best setting of the process parameters for a 22 nm PMOS device that affects the I_{OFF} which is suggested by Taguchi method is A_3, B_1, C_2, D_2 and this is summarised in Table 6.

Table 6
Optimum Setting of the Process Parameters

Factor	Process Parameter	Level	Best Value
A	Halo Implantation dose	3	2.50×10^{10} atom/cm^2
B	Halo Implantation tilting angle	1	35°
C	Gate Oxide growth annealing temperature	2	900 °C
D	Metal gate annealing temperature	2	850 °C

Table 7
Results of Optimum Setting Parameter with Added Noise

I_{OFF} (nA/μm)			
I_{OFF} 1 (X_1,Y_1)	I_{OFF} 2 (X_1,Y_2)	I_{OFF} 3 (X_2,Y_1)	I_{OFF} 4 (X_2,Y_2)
7.8969	8.38009	7.89307	8.37606

To finalise the optimum result of the design, these parameters were then simulated with the noise factors to get the final I_{OFF} results as shown in Table 7. After the optimisation approach, the device shows that the best I_{OFF} value is 7.89307 nA/μm with the noise factor combination (X_2, Y_1). However, all the noise factor combination resulted in the I_{OFF} is much lower that the predicted value of 100 nA/μm made by ITRS specification on 22 nm gate length CMOS device.

IV. CONCLUSION

As a conclusion, optimising the process parameters of a 22 nm TiO_2/WSi_x PMOS planar structure device with the lowest I_{OFF} recommended by the Taguchi method was successfully achieved. It has been shown that the variability of process parameters has a significant impact on the I_{OFF} [16]. In this experiment, it was proven that the Halo implantation tilting angle of 35° resulted in the dominant factor with an influence of 52.47% on the factor effect on variance. It is proved that studies from other researchers also showed that the variability of the Halo profile results in a better device behaviour, where the best parameter for the Halo tilt angle is between 25° to 35° [17],[18]

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REFERENCES

[1] K. Roy, J. P. Kulkarni, and S. K. Gupta, "Device/circuit interactions at 22nm technology node," in *IEEE Design Automation Conference (DAC '09)*, 2009, pp. 97–102.

[2] H.-J. Cho, K.-I. Seo, W. C. Jeong, Y.-H. Kim, Y. D. Lim, W. W. Jang, J. G. Hong, S. D. Suk, M. Li, C. Ryou, H. S. Rhee, J. G. Lee, H. S. Kang, Y. S. Son, C. L. Cheng, S. H. Hong, W. S. Yang, S. W. Nam, J. H. Ahm, D. H. Lee, S. Park, M. Sadaaki, D. H. Cha, D. W. Kim, S. P. Sim, S. Hyun, C. G. Koh, B. C. Lee, S. G. Lee, M. C. Kim, Y. K. Bae, B. Yoon, S. B. Kang, J. S. Hong, S. Choi, D. K. Sohn, J. S. Yoon, and C. Chung, "Bulk planar 20nm high-k/metal gate CMOS technology platform for low power and high performance applications," *Int. Electron Devices Meet.*, no. V, pp. 15.1.1–15.1.4, Dec. 2011.

[3] J. W. Sleight, I. Lauer, O. Dokumaci, D. M. Fried, D. Guo, B. Haran, S. Narasimha, C. Sheraw, D. Singh, M. Steigerwalt, X. Wang, P. Oldiges, D. Sadana, C. Y. Sung, W. Haensch, and M. Khare, "Challenges and opportunities for high performance 32 nm CMOS technology," *IEEE Int. Electron Devices Meet.*, pp. 1–4, 2006.

[4] K. J. Kuhn, "CMOS transistor scaling past 32nm and implications on variation," in *IEEE Advanced Semiconductor Manufacturing Conference*, 2010, pp. 241–246.

[5] K. Kuhn, C. Kenyon, A. Kornfeld, M. Liu, A. Maheshwari, W. Shih, S. Sivakumar, G. Taylor, P. VanDerVoorn, and K. Zawadzki, "Managing process variation in Intel's 45nm CMOS technology," *Intel Technol. J.*, vol. 12, no. 2, pp. 93–109, 2008.

[6] S. Mukhopadhyay and K. Roy, "Modeling and estimation of total leakage current in nano-scaled-CMOS devices considering the effect of parameter variation," *Int. Symp. Low Power Electron. Des.*, no. 1, pp. 172–175, 2003.

[7] A. H. Afifah Maheran, P. S. Menon, I. Ahmad, and S. Shaari, "Effect of Halo structure variations on the threshold voltage of a 22nm gate length NMOS transistor," *Mater. Sci. Semicond. Process.*, vol. 17, pp. 155–161, Jan. 2014.

[8] A. H. Afifah Maheran, P. S. Menon, I. Ahmad, and S. Shaari, "Optimisation of Process Parameters for Lower Leakage Current in 22 nm n-type MOSFET Device using Taguchi Method," *J. Teknol. (Sciences Eng.*, vol. 4, pp. 45–49, 2014.

[9] A. H. Afifah Maheran, P. S. Menon, I. Ahmad, S. Shaari, H. A. Elgomati, and F. Salehuddin, "Design and Optimization of 22 nm Gate Length High-k/Metal gate NMOS Transistor," *J. Phys. Conf. Ser.*, vol. 431, pp. 1–9, Apr. 2013.

[10] H. A. Elgomati, B. Y. Majlis, A. M. Abdul Hamid, P. S. Menon, and I. Ahmad, "Modelling of process parameters for 32nm PMOS transistor using Taguchi method," *Asia Model. Symp.*, pp. 40–45, May 2012.

[11] ITRS, "ITRS Report," *www.ITRS2012.net*, 2012. .

[12] S. I. Amin and M. S. Alam, "Virtual fabrication and analog performance of sub-40nm bulk MOSFET using TCAD Tool," *Int. J. Comput. Sci. Informatics*, vol. 1, no. 1, pp. 39–44, 2011.

[13] M. Salmani-Jelodar, H. Ilatikhameneh, S. Kim, K. Ng, and G. Klimeck, "Optimum High-k Oxide for the Best Performance of Ultra-scaled Double-Gate MOSFETs," vol. 13, no. February, pp. 1–5, 2015.

[14] J. Widiez, M. Vinet, B. Guillaumot, T. Poiroux, D. Lafond, P. Holliger, V. Barral, B. Previtali, F. Martin, M. Mouis, S. Deleonibus, C. E. A. Drt-leti, and M. Grenoble, "Fully depleted SOI MOSFETs with WSix , metal gate on HfO2 gate dielectric," *IEEE Int. SOI Conf. Proc.*, pp. 177–178, 2006.

[15] M. S. Phadke, *Quality engineering using robust design*. Pearson Education Inc. And Dorling Kindersley Publishing Inc. India., 2008.

[16] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proc. IEEE*, vol. 91, no. 2, pp. 305–327, 2003.

[17] A. Erlebach, T. Feudel, A. Schenk, and C. Zechner, "Influence of HALO and drain-extension doping gradients on transistor performance," *Mater. Sci. Eng. B*, vol. 114–115, pp. 15–19, Dec. 2004.

[18] Z. A. N. Faizah, I. Ahmad, P. J. Ker, P. S. A. Roslan, and A. H. A. Maheran, "Modeling of 14 nm gate length n-Type MOSFET," *RSM 2015 - 2015 IEEE Reg. Symp. Micro Nano Electron. Proc.*, pp. 2–5, 2015.