# Simulation Study on Different Logic Families of NOT Gate Transistor Level Circuits Implemented Using Nano-MOSFETs

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*Abstract*—**In this paper, a simulation study has been done on logic NOT transistor circuits with four different logic families, namely: (i) nano-CMOS NOT gate, (ii) nano-MOSFET loaded n-type nano-MOSFET NOT gate, (iii) resistive loaded nano-MOSFET NOT gate, and (iv) pseudo nano-MOSFET NOT gate. The simulation tool used is WinSpice. All the n-type and p-type nano-MOSFETs have channel length (L) 10 nm with width (W) 125 nm or 250 nm, depending on the type of logic families. Simulated timing diagrams for input and output waveforms showed correct logical NOT gate operations for all four logic families. Additionally, the voltage transfer characteristic (VTC) curves have been plotted for all four logic families. From the VTC plots, logic swing ($V_{LS}$), transition width ($V_{TW}$), high noise margin ($V_{NMH}$), low noise margin ($V_{NML}$), high noise sensitivity ($V_{NSH}$), low noise sensitivity ($V_{NSL}$), high noise immunity ($V_{NIH}$) and low noise immunity ($V_{NIL}$) have been obtained. Analysis on these values indicated that all the four logic NOT gate families which consist of nano-transistors meet the NOT gate operation conditions. Drain current, intrinsic delay and dynamic power are discussed as the effects of down scaling. In conclusion, NOT gates made of nano-MOSFETs with nanometer dimensions are able to perform correct logical operations in the same way as NOT gates made up of conventional bulk MOSFETs as proven by timing diagrams and VTC plots.**

*Index Terms*—**Logic Family; Nano-MOSFET; NOT Gate; Simulation.**

## I. INTRODUCTION

Downscaling of MOSFET structural dimensions from micrometer regime to nanometer regime has occurred over the last few decades [1, 2, 3]. The conventional bulk CMOS technology is rapidly continuously downscaling until it approaches the scaling limits. The MOSFET channel length L is approaching 10 nm. In order to enable gate to control charge in the channel, the requirement $T_{OX} \ll L$ must be met, where $T_{OX}$ is the oxide thickness [4]. In this study, the gate oxide thickness is approaching 1.5 nm, which is a few atomic layers. Meanwhile, the nano-MOSFET width W used in this study is 125 nm or 250 nm depending on the type of logic families [5, 6, 7]. In this study, NOT logical functions are implemented using four different logic families, namely: (i) nano-CMOS NOT gate, (ii) nano-MOSFET loaded n-type nano-MOSFET

NOT gate, (iii) resistive loaded (800 Ω) nano-MOSFET NOT gate, and (iv) pseudo nano-MOSFET NOT gate. Timing requirements for these NOT gates are analyzed using WinSpice [8, 9, 10]. In addition, VTC curves are plotted using WinSpice and investigations on these VTC curves have shown that all these four NOT gates met the NOT logical operations [11, 12].

## II. METHODOLOGY AND THEORY

The CIR Spice code files for four different logic families NOT gate are simulated using WinSpice. The input timing diagrams, output timing diagrams and VTC plots are the output result of WinSpice. Input signal with a period of 10 ns is applied to each four different NOT gates. A standard VTC plot for NOT gate is shown in Figure 1.
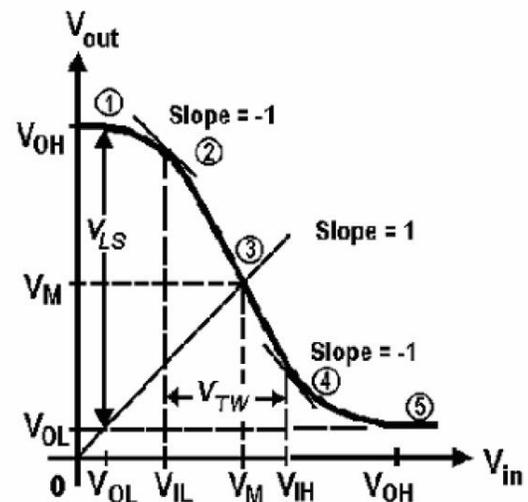


Figure 1: Standard voltage transfer characteristic (VTC) of a NOT gate

The parameters involved in VTC curve analysis are stated below:

- Output high voltage is $V_{OH}$. Output low voltage is $V_{OL}$.

- Input high voltage is $V_{IH}$. Input low voltage $V_{IL}$.
- The midpoint voltage in the VTC where $V_O = V_I$ is $V_M$.

As the input voltage is increased from 0, $V_{IL}$ is the maximum input voltage that provides a high output voltage (logical 1 output). Furthermore, $V_{IH}$ has the definition of being the minimum input voltage that provides a low output voltage (logical 0 output). The values $V_{OH}$, $V_{OL}$, $V_{IL}$ and $V_{IH}$ are referred to as the critical voltages of the voltage transfer characteristic. The midpoint voltage $V_M$ is defined as the point on the transfer characteristic, where $V_{out} = V_{in}$ and ideally appears at the center of the transition region. $V_M$ can be found graphically by superimposing (the unity slope) $V_{out} = V_{in}$ and finding its intersection with VTC.

In order to always distinguish between high and low voltage level, the following conditions must be satisfied:

$$V_{OH} > V_{IH} \text{ and } V_{OL} < V_{IL}.$$

Furthermore, logic swing $V_{LS} = V_{OH} - V_{OL}$. Transition width $V_{TW} = V_{IH} - V_{IL}$. The transition width is the amount of voltage change that is required of the input voltage to cause a change in the output voltage from the high to the low level (or vice-versa).

Variations in the steady-state voltage levels of digital circuits (i.e. the logical 1 and the logical 0 states) are undesirable and cause logic errors if the fluctuation from the desired or specified voltage levels is too great. This variation of steady state voltage levels in digital circuits is referred to as voltage level degradation and is termed *noise*. The voltage noise margins represent a safety margin for the high and low voltage levels. Extraneous noise voltages must have magnitudes less than the voltage noise margins. The exact magnitudes of the high and low level are not important. However, the high or low magnitude of voltage must remain in the range of voltages that provide positive noise margins. High noise margin is represented by $V_{NMH} = V_{OH} - V_{IH}$, while low noise margin is represented by $V_{NML} = V_{IL} - V_{OL}$. Figure 2 shows the noise margin conditions.
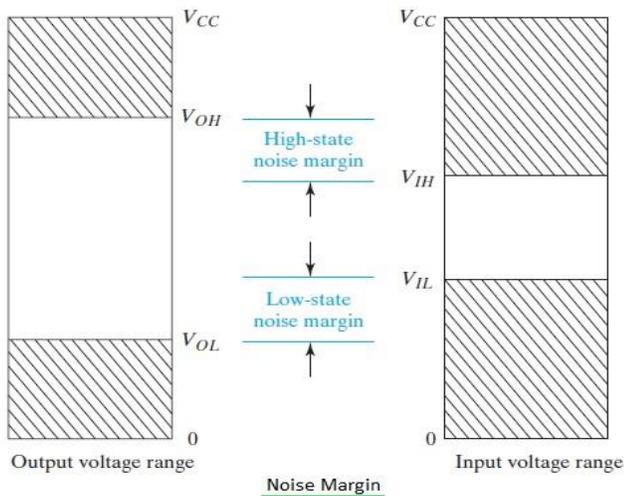


Figure 2: Noise margin conditions

- High noise sensitivity VNSH = VOH – VM.

- Low noise sensitivity VNSL = VM – VOL.

The quantity *noise immunity* is the ability of a gate to reject noise and being defined below:

- High noise immunity $V_{NIH} = \dfrac{V_{NSH}}{V_{LS}}$.

- Low noise immunity $V_{NIL} = \dfrac{V_{NSL}}{V_{LS}}$.

Figure 3 shows the VTC for an ideal NOT gate.
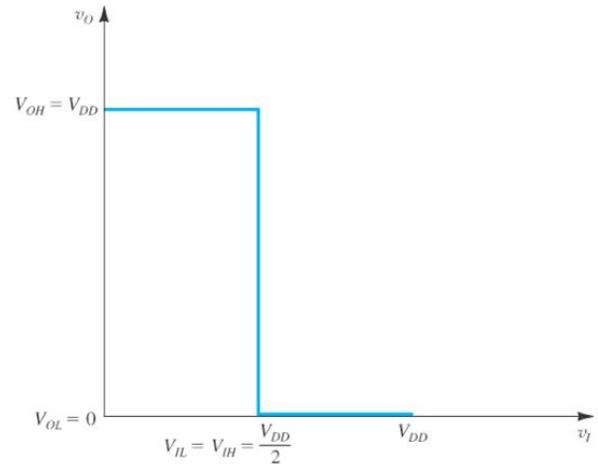


Figure 3: VTC for an ideal NOT gate

## III.  RESULTS AND DISCUSSIONS
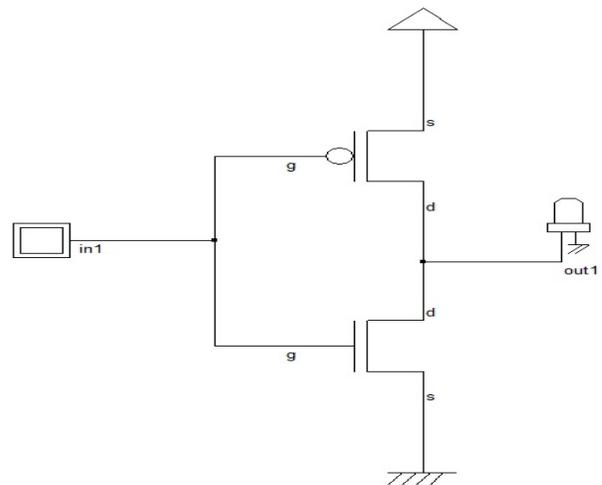


Figure 4: Nano-CMOS NOT transistor level circuit

Figure 4, Figure 5, Figure 6 and Figure 7 show the schematic circuits of all four logic families NOT gate. Their timing diagrams are shown in Figure 8(a) and 8(b), Figure 9(a) and 9(b), Figure 10(a) and 10(b) as well as Figure 11(a) and 11(b) accordingly.
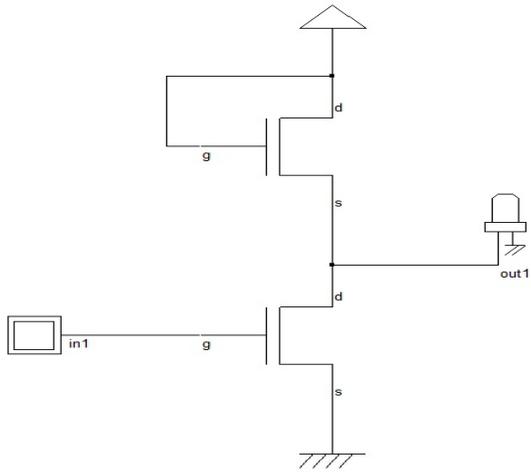


Figure 5: Nano-MOSFET loaded NOT transistor level circuit
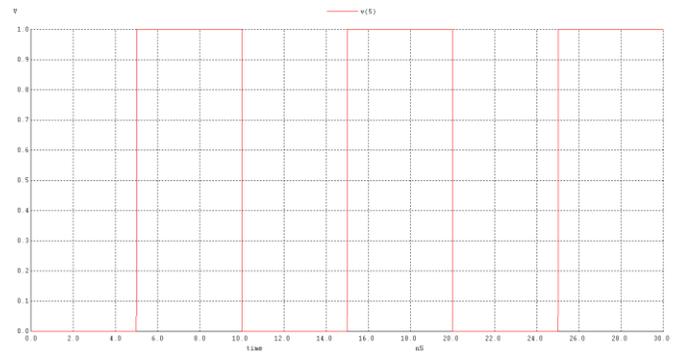


Figure 8(a): Input signal of nano-CMOS NOT circuit
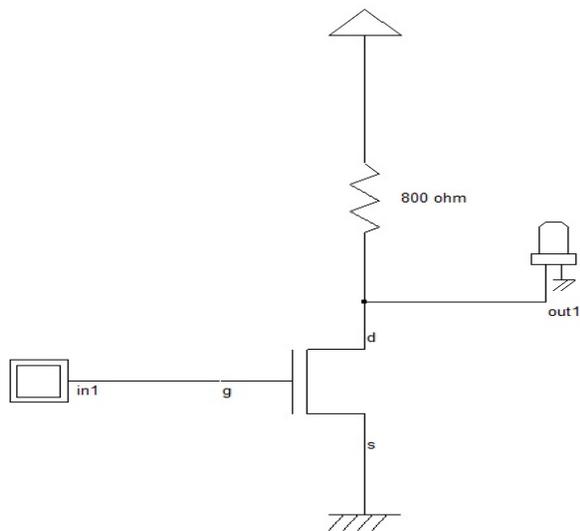


Figure 6: Resistive loaded NOT transistor level circuit
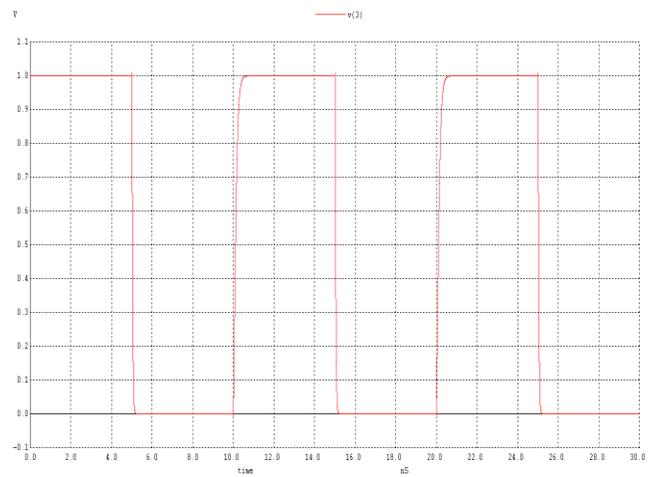


Figure 8(b): Output signal of nano-CMOS NOT circuit
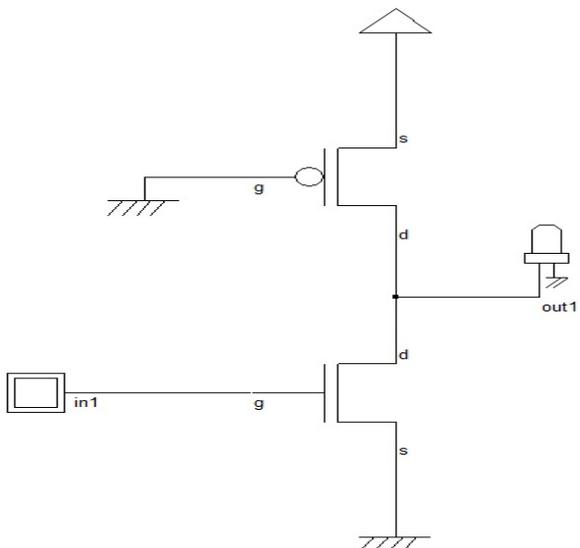


Figure 7: Pseudo nano-MOSFET NOT transistor level circuit
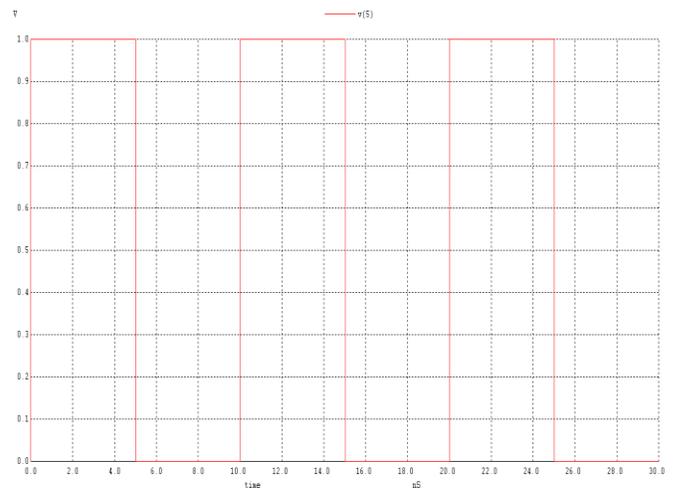


Figure 9(a): Input signal of nano-MOSFET loaded NOT circuit
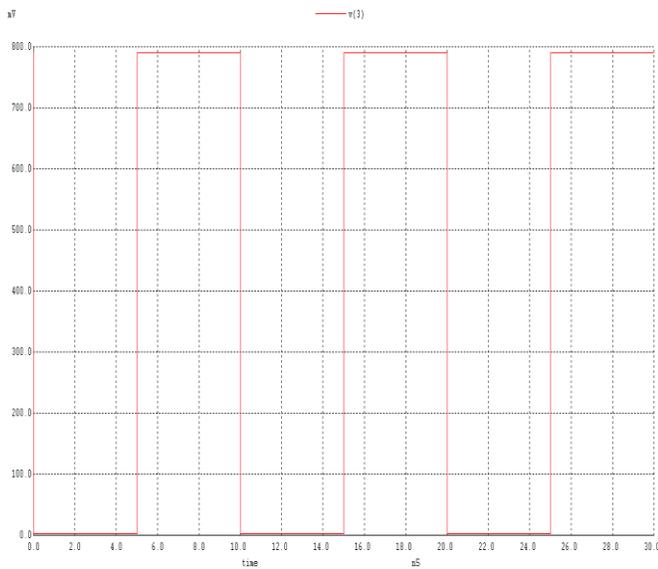
Figure 9(b): Output signal of nano-MOSFET loaded NOT circuit



Figure 11(a): Input signal of pseudo nano-MOSFET NOT circuit



Figure 10(a): Input signal of resistive loaded NOT circuit
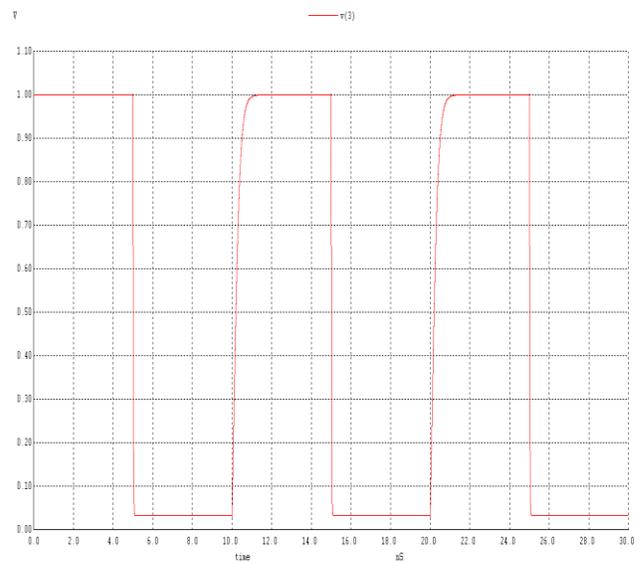


Figure 11(b): Output signal of pseudo nano-MOSFET NOT circuit



Figure 10(b): Output signal of resistive loaded NOT circuit

The above input and output signal timing diagrams show correct logical NOT operation for all four logic families. The period of the input signal to each NOT circuit is 10 ns. The output signal of nano-MOSFET loaded NOT circuit shows a threshold voltage loss of 0.2 V since the nano-MOSFET load acts as a pass transistor which passes a weak logic level 1 and passes a strong logic level 0. The threshold voltage loss 0.2 V corresponds to the threshold voltage of nano-MOSFET, which is 0.2 V [13, 14]. The nano-MOSFET pass transistor load is equivalent to 800 Ω load resistance. This 800 Ω resistance is calculated from the nano-MOSFET current-voltage (I-V) curve in the linear portion, where digital operation occurred as shown in Figure 12. By this way, resistive loaded 800 Ω nano-MOSFET NOT circuit is formed as shown in Figure 6.
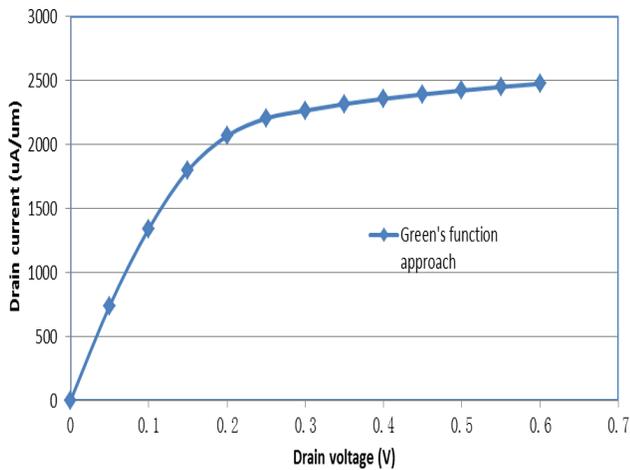
Figure 12: I-V curve of nano-MOSFET. Linear portion of this curve is used to calculate load resistance.

Figure 13, Figure 14, Figure 15 and Figure 16 show the VTC plots of all four logic families NOT circuit.
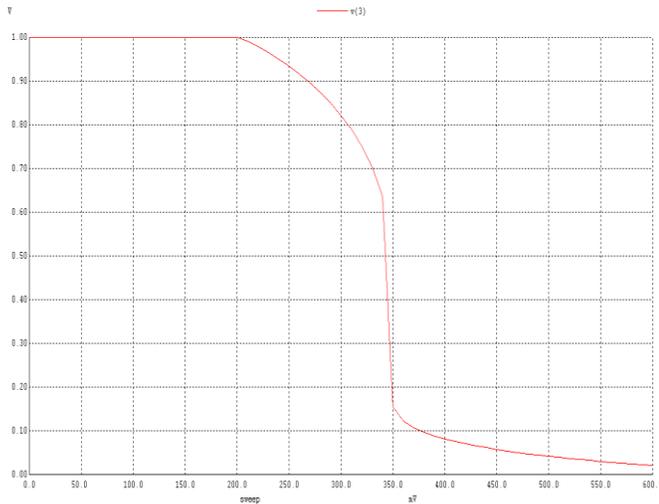


Figure 13: Simulated VTC curve of nano-CMOS NOT circuit
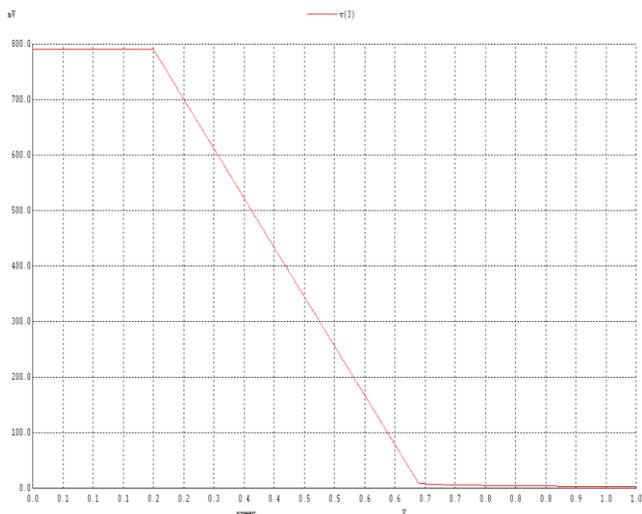


Figure 14: Simulated VTC curve of nano-MOSFET loaded NOT circuit
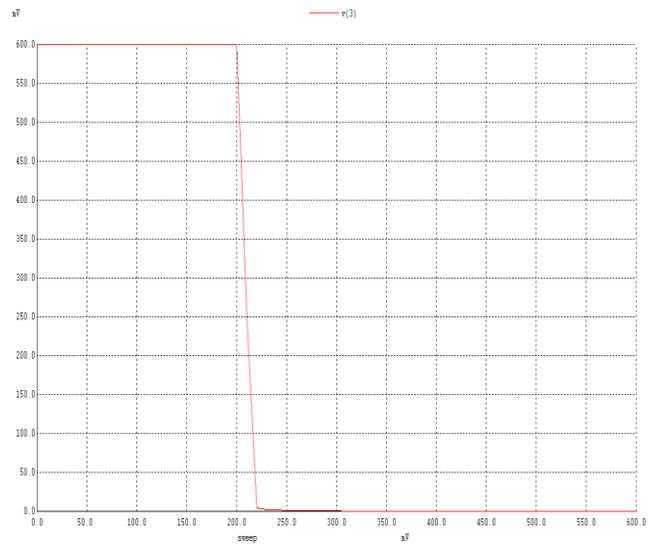


Figure 15: Simulated VTC curve of resistive loaded NOT circuit
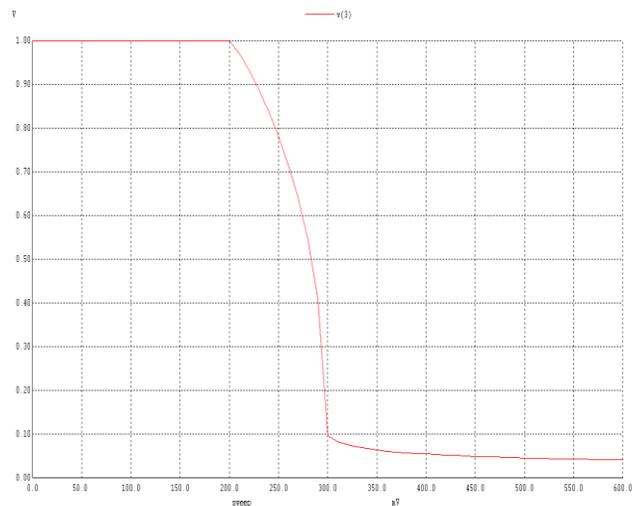


Figure 16: Simulated VTC curve of pseudo nano-MOSFET NOT circuit

Table 1, Table 2, Table 3 and Table 4 are the parameters calculated from the VTC plots using the expressions explained in the previous section. From these tables, the analysis indicates that the condition $V_{OH} > V_{IH}$ , $V_{OL} < V_{IL}$ and noise margins are met. Therefore, all four logic NOT gates designs formed by p-type and n-type nano-MOSFETs with channel length L=10 nm and width W= 125 nm or 250 nm can work properly. In nano-CMOS NOT circuit, n-type nano-MOSFET has W=125 nm and p-type nano-MOSFET has W= 250 nm to counter-balance the difference in electron and hole mobility. In nano-MOSFET loaded NOT circuit, the n-type nano-MOSFET load has W = 125 nm and the bottom n-type nano-MOSFET has W = 250 nm. This condition is needed to meet

$$\left(\frac{W}{L}\right)_n \geq 2\left(\frac{W}{L}\right)_{Load}.$$

in order to reduce $V_{OL}$.

Table 1: VTC parameters for nano-CMOS NOT circuit

| Nano-CMOS NOT Circuit | |
| --- | --- |
| $V_{OH}$ | 1.00 V |
| $V_{OL}$ | 0.02 V |
| $V_{IH}$ | 0.40 V |
| $V_{IL}$ | 0.20 V |
| $V_M$ | 0.35 V |
| $V_{LS}$ | 0.98 V |
| $V_{TW}$ | 0.20 V |
| $V_{NMH}$ | 0.60 V |
| $V_{NML}$ | 0.18 V |
| $V_{NSH}$ | 0.65 V |
| $V_{NSL}$ | 0.33 V |
| $V_{NIH}$ | 0.66 |
| $V_{NIL}$ | 0.37 |

Table 2: VTC parameters for nano-MOSFET loaded NOT circuit

| Nano-MOSFET loaded NOT Circuit | |
| --- | --- |
| $V_{OH}$ | 0.80 V |
| $V_{OL}$ | 0.00 V |
| $V_{IH}$ | 0.66 V |
| $V_{IL}$ | 0.20 V |
| $V_M$ | 0.42 V |
| $V_{LS}$ | 0.80 V |
| $V_{TW}$ | 0.42 V |
| $V_{NMH}$ | 0.14 V |
| $V_{NML}$ | 0.20 V |
| $V_{NSH}$ | 0.38 V |
| $V_{NSL}$ | 0.42 V |
| $V_{NIH}$ | 0.48 |
| $V_{NIL}$ | 0.52 |

Table 3: VTC parameters for resistive loaded NOT circuit

| Resistive loaded 800Ω NOT Circuit | |
| --- | --- |
| $V_{OH}$ | 0.60 V |
| $V_{OL}$ | 0.00 V |
| $V_{IH}$ | 0.22 V |
| $V_{IL}$ | 0.20 V |
| $V_M$ | 0.21 V |
| $V_{LS}$ | 0.60 V |
| $V_{TW}$ | 0.02 V |
| $V_{NMH}$ | 0.38 V |
| $V_{NML}$ | 0.20 V |
| $V_{NSH}$ | 0.39 V |
| $V_{NSL}$ | 0.21 V |
| $V_{NIH}$ | 0.65 |
| $V_{NIL}$ | 0.35 |

Table 4: VTC parameters for pseudo nano-MOSFET NOT circuit

| Pseudo nano-MOSFET NOT Circuit | |
| --- | --- |
| $V_{OH}$ | 1.00 V |
| $V_{OL}$ | 0.05 V |
| $V_{IH}$ | 0.30 V |
| $V_{IL}$ | 0.20 V |
| $V_M$ | 0.28 V |
| $V_{LS}$ | 0.95 V |
| $V_{TW}$ | 0.10 V |
| $V_{NMH}$ | 0.70 V |
| $V_{NML}$ | 0.15 V |
| $V_{NSH}$ | 0.72 V |
| $V_{NSL}$ | 0.23 V |
| $V_{NIH}$ | 0.76 |
| $V_{NIL}$ | 0.24 |

In pseudo nano-MOSFET NOT circuit, p-type nano-MOSFET has W = 125 nm and n-type nano-MOSFET has W = 250 nm. This condition is needed to meet the same criteria in the above expression in order to reduce $V_{OL}$. Meanwhile, in the resistive loaded 800 Ω NOT circuit, 800 Ω resistance is the load and n-type nano-MOSFET has W = 250 nm [15].

The effects of down scaling of MOSFET into nanometer regime, which will be discussed now include drain current, intrinsic delay and dynamic power. If the scaling factor is s, Table 5 lists the quantities of MOSFET involved in the down scaling.

Table 5: Quantities of MOSFET involved in down scaling

| Quantity | Before Scaling | After Scaling |
| --- | --- | --- |
| Channel Length | L | L'=L*s |
| Channel Width | W | W'=W*s |
| Gate Oxide Thickness | $T_{OX}$ | $T'_{OX}=T_{OX}*s$ |
| Power Supply | $V_{DD}$ | $V'_{DD}=V_{DD}*s$ |
| Threshold Voltage | $V_{TH}$ | $V'_{TH}=V_{TH}*s$ |

For scaling purpose, the alpha-power model of drain current is very useful:

$$I_{DS} = KWL^{-0.5}T_{OX}^{-0.8}\left(V_{GS} - V_{TH}\right)^{1.25}.$$

where K is the process transconductance. If L, $T_{OX}$ and V are all scaled by the scaling factor s, current should remain constant per micron of width (approximately 2500 μA/μm, refer to Figure 12). Since capacitance is

$$C = \frac{\varepsilon WL}{T_{OX}},$$

the intrinsic delay is given by:

$$\Delta t' = \frac{CV}{I} = s\Delta t$$

since C, V and I all were scaled down by the scaling factor s. Hence, logic gate formed by down scaled MOSFET has smaller delay and performed faster. To investigate the dynamic power during down scaled, refer to Table 6. The drain/source capacitance of nano-MOSFET is $1.184 \times 10^{-16}$ F.

Table 6: Dynamic powers for four different NOT logic

|  | nano-CMOS NOT | nano-MOSFET loaded NOT | Pseudo nano-MOSFET NOT | Resistive loaded NOT |
|---|---|---|---|---|
| Dynamic Power (Watts) | 2.36E-08 | 2.36E-08 | 2.36E-08 | 7.10E-09 |
| Voltage Supply (Volts) | 1 | 1 | 1 | 0.6 |
| Frequency of switching (Hertz) | 1.00E+08 | 1.00E+08 | 1.00E+08 | 1.00E+08 |

The equation used to obtain dynamic power is:

$$P(dyn) = C\, f\, V_{DD}^2.$$

where C is the capacitance at output node, f is the frequency of switching and $V_{DD}$ is the voltage supply. Normally, in conventional bulk micrometer MOSFET logic, the dynamic power is about µW. Therefore, from Table 6, reduction in dynamic power is observed during down scaling.

## IV. CONCLUSION

Logical NOT gate operation can be implemented by using nano-MOSFETs with four different logic families. Conventional bulk MOSFETs can be replaced by nano-MOSFETs to implement NOT transistor level circuits. In this paper, this development in semiconductor industry has been shown by a simulation study using WinSpice and observing the input timing diagrams, output timing diagrams and VTC plots. Correct logical NOT operations are observed from these simulation output. During the down scaling process, a faster logic gate is possible when the current per micron width remain constant, dynamic power is reduced and intrinsic delay becomes slower.

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