Impact of Different Dose, Energy and Tilt Angle in Source/Drain Implantation for Vertical Double Gate PMOS Device

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Abstract—In this paper, an investigation on the impact of different dose, energy and tilt angle of Source/Drain (S/D) implantation towards threshold voltage (V_{TH}) value in vertical double-gate PMOS device was conducted by using L_8 2k-factorial design. The level of significance for each process parameters on V_{TH} was determined by using analysis of variance (ANOVA). The virtual fabrication and electrical characterization of the device were performed by using a process simulator (ATHENA) and a device simulator (ATLAS) respectively. This procedure was followed by 2k-factorial design to aid in optimizing the process parameter variations towards V_{TH} value. Based on the final results, the most dominant factor that affects V_{TH} value was found to be S/D implant energy. Meanwhile, the nominal possible V_{TH} value after the optimization analysis was observed to be − 0.4509V. The percentage difference is only 0.87% higher than ITRS 2013 prediction for low power (LP) requirement in the year 2020.

Index Terms—ANOVA; Threshold Voltage; 2k-Factorial.

I. INTRODUCTION

As the Metal-oxide-semiconductor Field Effect Transistor (MOSFET) devices are further scaled down to submicron and nanometer dimension, the level of importance of device structure and fabrication technology increases. One of the major fabrication processes that needs to be considered is known as the Source/Drain (S/D) implantation. The S/D implantation is a very important fabrication process that is capable of reducing short channel effects (SCEs) in MOSFET device [1]. S/D regions are doped with the opposite conductivity type that acts as the well that surrounds them. Arsenic implants are often used to form n-type S/D for n-channel (NMOS) transistors while Boron or BF_2 implants are used to form p-type S/D for p-channel (PMOS) transistors.

These highly doped S/D regions are contacted by cobalt silicide (CoSi) to the other parts of the device for better electrical performance. The S/D regions are able to form back-to-back semiconductor junction diodes even in the absence of a bias on the gate and drain. When a sufficiently large bias is applied to the gate, a surface inversion layer will be formed, thereby creating a conducting channel between the source and the drain [2]. This will induce the current to flow in the channel by the application of a bias in the drain. Furthermore, the bias on the gate is varied to modulate the conductance of the MOSFET device.

The major challenge in scaling S/D implant is to satisfy the junction depth requirement while increasing the active dopant concentration. The junction depth must be ensured not to be too shallow; otherwise, the silicidation process will consume the entire junction. It is also important to minimize the electrically active residual damage in S/D regions, which could increase the leakage current (I_{OFF}). Dubois et al. [3] mentioned that the implantation energy of S/D implants in MOSFET fabrication processes is commonly optimized for better electrical performances. The lateral diffusion of the S/D dopant ions in channel region can be minimized by an excellent control of dosage doping, energy and tilt angle.

Many researchers have proposed methods not only to control the electrical characteristics, mainly threshold voltage and saturation current but also to optimize the process parameters variation. The process parameter fluctuations in general can be divided into global variations and local variations. Local variations in the MOSFET device is commonly arose from the random microscopic process variations. The examples of random distributions arose from the process parameters variation includes impurity concentration densities, energy, tilt angle and temperature, which eventually result in the variation of the threshold voltage (V_{TH}) [4].

This paper emphasizes on an attempt to identify semiconductor process parameters whose variability would impact most on the threshold voltage (V_{TH}) of vertical double-gate PMOS device by using 2k-factorial methods [5]. The 2k-factorial method is one of the common statistical tools that is mainly used for improving productivity during research and development (R&D). Generally, the 2k-factorial design is a simplified version of full-factorial design, in which experimental trials or runs are performed at all combinations of factor levels. But somehow, full-factorial design is very difficult to be implemented, especially when dealing with the large number of factors. Therefore, the 2k-factorial design is introduced for the easy analysis approach. The 2k-factorial design is utilized to determine the effects of k factors (process parameters) which have two levels. It also helps to sort out factors (process parameters) in the order of their impact on V_{TH} value [6].

II. MATERIALS AND METHODS

A. Process Simulation

Process simulation of p-channel Vertical DG-MOSFET device was done by using an ATHENA module of Silvaco International software. The process began with the selection of a p-type silicon (boron doped) with <100> orientation as the main substrate. The 16nm of buried oxide (t_{BOX}) was then developed beneath the silicon substrate. The remaining silicon substrate at the top was etched in order to form a very thin silicon pillar with the length of 12 nm (L_{sp}) and height of 80 nm (H_{sp}). The function of the ultrathin silicon pillar was to create a very sharp vertical channel that could increase the drive current (I_{ON}). The virtual process was followed by the gate oxidation process at temperature of 927° C. Since the device was a p-channel type, 1.57×10^{11} atom/cm^3 of phosphor was doped into the substrate at 21 Kev of energy and 10° of tilt angle in order to form n$^+$ region.

Polysilicon material was then deposited at the top of the gate oxide. After that, both polysilicon and polysilicon oxide were etched away to form a very thin gate with a length of 12nm. In order to enhance the performance of the device, 1.61×10^{12} atoms/cm^3 concentration of phosphor was doped at an energy level of 170 Kev and tilt angle of 24° (Halo implantation). Halo implantation was followed by depositing sidewall spacers. Sidewall spacers were used as a mask for source/drain implantation process. Boron with concentration of 6.91×10^{13} atom/cm^3 was implanted in order to supply free hole to form a p+ region as conductive channel.

Compensation implantation was utilized later by implanting phosphor dosage of 2.57×10^{12} atoms/cm^3 with an energy level of 64 Kev and tilt angle of 13°. The function of compensation implantation was to reduce parasitic effects that might increase the leakage current (I_{OFF}). Next, silicide (CoSi) was formed on top of the source and drain region by sputtering cobalt on a silicon surface. This step was done in order to reduce the sheet resistance (R_s). The majority of the silicides exhibit metallic conductivity [7], and the silicide-silicon junction will behave as a metal-semiconductor contact. This transistor was then connected with aluminum metal. The aluminum layer was deposited on the top of the Intel-Metal Dielectric (IMD) and unwanted aluminum was etched to develop the contacts [8, 9]. The procedure was completed after the metallization and etching were performed for electrode formation, and the bonding pads were opened. The final structure of the device was completed by mirroring the right-hand side structure. The completed structure of p-channel Vertical Double Gate PMOS device is illustrated as in Figure 1.
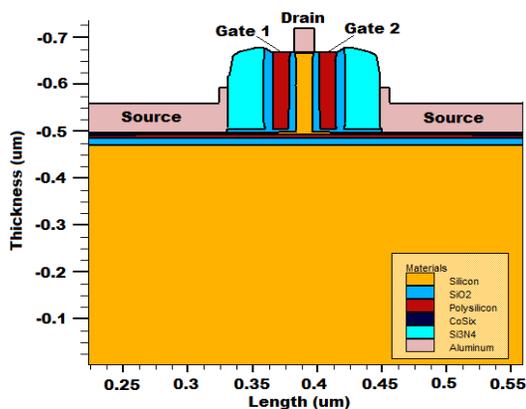

Figure 1: Structure of Vertical Double Gate PMOS device

B. 2k-factorial Design by using L8 Orthogonal Array Method

Initially, the experimental layout of L_8 orthogonal array 2k-factorial design has been auto-generated by using software Minitab. Table I shows the experimental layout for four process parameters using the L_8 orthogonal array. The threshold voltage (V_{TH}) values for eight sets of experiment were attained based on the allocated levels in Table 1. The value of the response, V_{TH} was recorded in order to analyze the dependability of the V_{TH} towards S/D Implant Dose, S/D Implant Energy, S/D Implant Tilt and Compensatation Implant Dose. The value of the response, V_{TH} was used as a significant determinant whether the device was working well or not. Table 2 lists the process parameters and their appropriate levels for the entire experiments. The process parameters, i.e: S/D Implant Dose, S/D Implant Energy, S/D Implant Tilt and Compensatation Implant Dose are represented by symbols, A, B, C and D respectively.

Table 1
L_8 orthogonal array 2k-factorial design

Exp no.	Process Parameter Level			
	A	B	C	D
1	1	1	1	1
2	1	-1	1	-1
3	-1	1	1	-1
4	-1	-1	-1	-1
5	-1	1	-1	1
6	1	1	-1	-1
7	1	-1	-1	1
8	-1	-1	1	1

Table 2
Process parameters and their levels

Symbol	Process Parameter	Units	(-1)	(1)
A	S/D Implant Dose	atom/cm^3	6.94E13	6.97E13
B	S/D Implant Energy	kev	12	14
C	S/D Implant Tilt	degree	10	13
D	Compensation Implant Dose	atom/cm^3	2.54E12	2.57E12

III. RESULTS AND DISCUSSION

The virtual fabrication results (device characteristics) of the first set of experiment simulated by using ATHENA module are discussed. The experimental results of threshold voltage (V_{TH}) were analyzed and optimized by using 2k-factorial design method in order to obtain the optimal design. The 2k-factorial analysis performed via Minitab 16 software.

A. Characterization of Vertical Double Gate PMOS Device

Figure 2 shows the graph of drain current (I_D) versus gate voltage (V_G) at the drain voltage V_D = - 0.05 V and voltage V_D = - 1.0 V for vertical double-gate PMOS device. The threshold voltage (V_{TH}) for this device is observed to be 0.411 V. In the next section, the impact of Source/Drain (S/D) implant variations upon V_{TH} value was investigated by using L_8 orthogonal array 2k-factorial method. Besides that, the doping concentration, energy and tilt angle levels for the involved process parameters were statistically optimized to obtain the nominal V_{TH} value close to ITRS 2013 prediction.
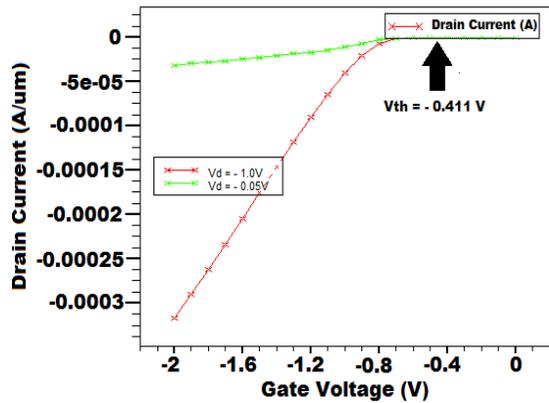

Figure 2: Graph of subthreshold drain current (I_D) versus gate voltage (V_G)

B. Analysis of 2k-factorial Design

This section describes the optimization process of four process parameters towards threshold voltage (V_{TH}) value in vertical double-gate PMOS device. The 2k-factorial design enables the investigation of the effect of several control factors implemented simultaneously in certain design. Normally, single repetition design is used for the experiment that involves many control factors [10]. Several experiments were run in order to determine which factor or variable that contribute the most significant impact on the output response, V_{TH}. Besides that, it can also give the most recommendable value or optimum value for certain factor.

The threshold voltage (V_{TH}) value for each set of experiment has been acquired by utilizing the Silvaco TCAD software. For each set of experiment, there were different process parameter levels, as shown in Table 2. The final results of the experiments were recorded in Table 3. It can be observed that the V_{TH} values are between the range of -0.389 V to -0.453 V. Therefore, all sets of experiment are suitable for the test of threshold voltage (V_{TH}). Since the nominal V_{TH} value for low power (LP) consumption requirement in the year 2020 listed in ITRS 2013 is -0.447 V [11], the optimization method using 2k-factorial design needed to be done for optimum result.

Table 3
Threshold Voltage (V_{TH}) values for Vertical Double gate PMOS device

Exp. no.	Process Parameter Level				Threshold Voltage (V_{TH})
	A	B	C	D	
1	1	1	1	1	-0.4114
2	1	-1	1	-1	-0.4524
3	-1	1	1	-1	-0.4110
4	-1	-1	-1	-1	-0.4512
5	-1	1	-1	1	-0.3905
6	1	1	-1	-1	-0.3899
7	1	-1	-1	1	-0.4519
8	-1	-1	1	1	-0.4535

C. Estimation of factor effects

The analysis of threshold voltage (V_{TH}) started with the estimation of the effects of factor (process parameter), A, B, C and D towards the variation of V_{TH} values as listed in Table 4. From Table 4, it can be observed that only factor B (S/D Implant Energy) has contributed a significant impact on the V_{TH} values due to its lower p-value.

Table 4
Estimation of Factor Effect and Coefficients for V_{TH}

Term	Effect	Coef	SE Coef	T	P
A	-0.00015	-0.00007	0.002830	-0.03	0.981
B	-0.05155	-0.02578	0.002830	-9.11	0.003
C	0.01120	0.00560	0.002830	1.98	0.142
D	0.00070	0.00035	0.002830	0.12	0.909

Based on the estimation effect analysis in Table 4, the normal plot for standardized effects can be developed. All the effects along the line can be ignored. Only the significant effects which are located far from the line will be considered. Figure 3 shows the most significant factor that contributes to the highest impact on the V_{TH} value, which is factor B (S/D Implant Energy). Meanwhile, factor A, C and D were observed to be located near to the straight line and they are considered as the non-significant factors. Factor A, C and D represent the S/D Implant Dose, S/D Implant Tilt and Compensatation Implant Dose respectively.
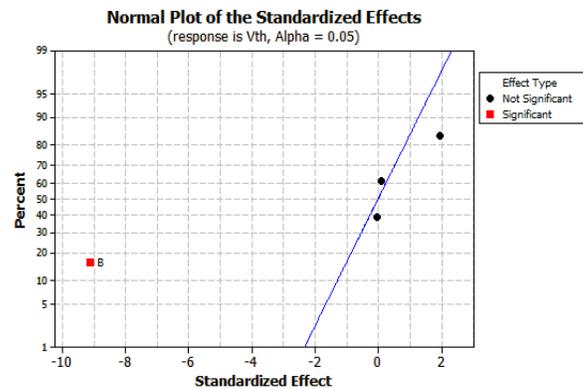

Figure 3: Normal Plot of Standardized Effects

The guideline that has been utilized for this analysis is based on 95 percent confidence level. If there are any effects exceed this line, the effect is considered significant. Figure 4 depicts a

Pareto chart of the standardized effects which indicates that the main effect of factor B has exceeded the line, thereby contributes to the most significant effect on V_{TH} values. Based on Pareto chart, the main effects of factor A, C and D do not exceed the line and they will be considered as the non-significant factors.
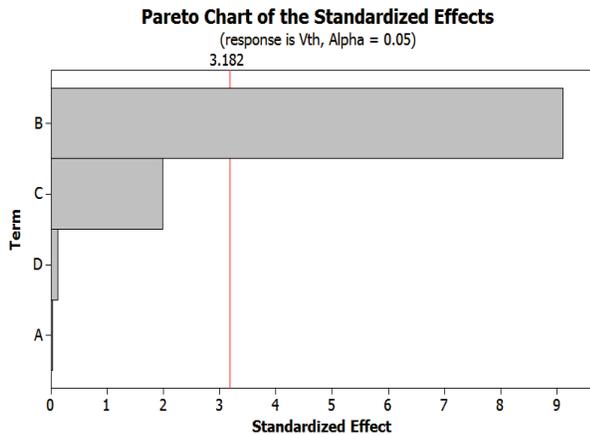

Figure 4: Pareto Chart of the Standardized Effects

Figure 5 depicts the main effects plot for threshold voltage (V_{TH}). It can be observed that only factor B (S/D Implant Energy) is negative. This is due to the reduction of V_{TH} value as the energy of S/D Implantation increases. Factor A is considered neutral, while factor C and D are positive as they do not give any significant impact on V_{TH} value and can be ignored.
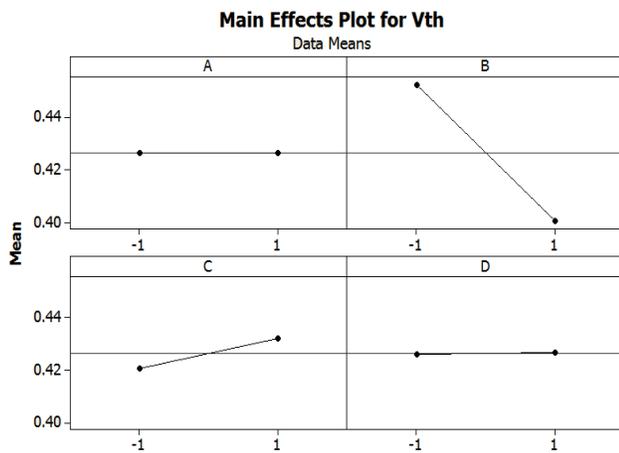

Figure 5: Main Effects Plot for V_{TH}

D. Analysis of Variance (ANOVA) for VTH

For the purpose of upgrading the built model, factors that are not significant are removed from the full model. Based on the analysis that has been done, factor A, C and D will be ignored as they are considered as the less significant factors. Only factor B will be analyzed in the new model. As shown in Table 5, analysis of variance (ANOVA) for V_{TH} is simplified for investigating the residual error in the model. The P-value represents the probability of residual error in order to determine certain factors as significant factors. Normally, the factor effects have to be below than 0.05 in order to let one

factor to be considered as a significant factor, in which it achieves 95 percent of confident level.

Table 5
Analysis of Variance (ANOVA) for V_{TH}

Source	DF	Seq SS	Adj MS	F	P
B	1	0.00531481	0.00531481	71.81	0.000
Residual Error	6	0.00044407	0.00007401		
Total	7	0.00044407			

Based on the results in Table 5, the main effect of factor B is significant with the p-value equals to 0.00. Residual error analysis can be implemented to ensure model adequacy and to check estimation. The analysis was done only for the main effect factor, which is factor B. Normal probability plot for residual error is shown in Figure 7. It is observed that all the points in the graph are located near to the straight line. Therefore, the conclusion that only factor B has significant effects on V_{TH} is true.
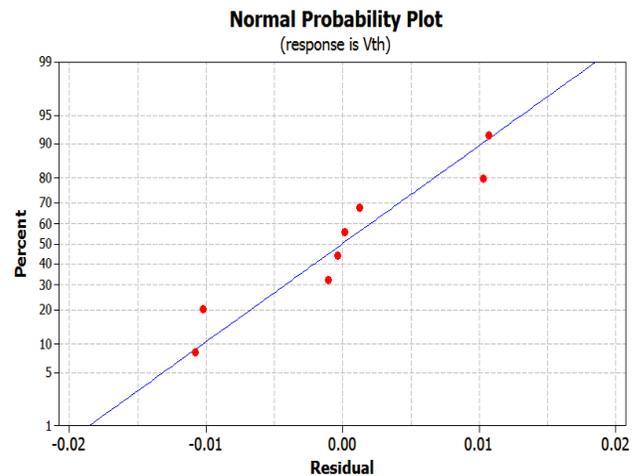

Figure 6: Normal Probability Plot

E. Optimization Analysis

An optimization plot is a Minitab Response Optimizer tool that shows how different experimental settings affect the predicted responses for 2k-factorial design. Minitab calculates an optimal solution and draws the plot. The optimal solution serves as the initial point of the plot, in which the designer can modify the level settings interactively to determine how different settings affect responses.

Figure 7 depicts the optimization plot for the 2k-factorial design. It is observed that the current value with red color is the optimal level value for factor A, B, C and D. For factor A, the level is set to be high (1.0). Meanwhile, for factor B, C and D, the level are set to be low (-1.0). Therefore, the most optimum combination of factor levels suggested by 2k-factorial in Minitab are A(1), B(-1), C(-1) and D(-1). Factor A, B, C and D represent for S/D Implant Dose, S/D Implant Tilt and Compensatation Implant Dose respectively.
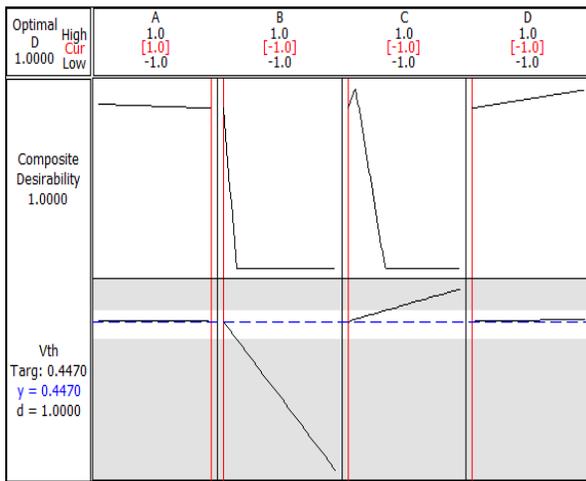
Figure 7: Optimization Plot

IV. CONFIRMATION TEST

Confirmation test is the final step in the design of the experiment (DoE) process. The main purpose of the confirmation test is to verify the results of V_{TH} value during analysis phase [12, 13]. Since the most optimum combination levels of process parameters, A(1), B(-1), C(-1) and D(-1) are different from any combination level of experiment rows in Table 3 the confirmation test of suggested setting of process parameters need to be conducted. The best settings of process parameters for vertical double-gate PMOS device which have been suggested by 2k-factorial design are shown in Table 6.

Table 6
Overall Best Setting of Process Parameters

Symbol	Process Parameter	Units	Best Value
A	S/D Implant Dose	atom cm^{-3}	6.97E13
B	S/D Implant Energy	kev	12
C	S/D Implant Tilt	degree	10
D	Compensation Implant Dose	atom cm^{-3}	2.54E12

The final step is to verify the improvement of threshold voltage (V_{TH}) value by simulating the device using the best setting of process parameters. The results of the final simulation of the device are shown in Table 7.

Table 7
Final result of Confirmation Test for Threshold Voltage

Experiment	Process Parameter Level				Threshold Voltage (V_{TH})
	A	B	C	D	
Confirmation Test	1	-1	-1	-1	-0.4509

The nominal V_{TH} value is observed to be -0.4509V and it is observed to be the closest V_{TH} value towards ITRS 2013 prediction (-0.447V) than any of the experiment rows in Table 3. The percentage difference is only 0.87% higher than the predicted value [11]. This result is still within the acceptable range of V_{TH} value of ITRS 2013 for low power (LP) requirement in the year 2020 ($\pm 12.7\%$ of 0.447V). S/D implant energy has been identified to be a significant process parameter that contributes to the most impact on the threshold

voltage (V_{TH}) value in vertical double-gate PMOS device. These results imply that 2k-factorial design is one of the efficient statistical methods that is capable of predicting the optimum solution in finding the best level of source/drain implantation for nominal threshold voltage (V_{TH}) value.

V. CONCLUSION

The optimum solution to obtain the nominal threshold voltage (V_{TH}) in accordance with ITRS 2013 prediction has been successfully done using L_8 2k-factorial design. Threshold voltage (V_{TH}) is an important electrical characteristic investigated in this research project as it is the main factor to determine the functionality of vertical double gate PMOS device. The level of significance of process parameters upon V_{TH} is determined by using analysis of variance (ANOVA). Based on ANOVA method, the process parameter that dominantly influences the V_{TH} variations was S/D implant energy. The nominal threshold voltage (V_{TH}) after the optimization analysis was observed to be –0.4509 V. The final result proves that the nominal V_{TH} characteristic of vertical double-gate PMOS device can be attained via L_8 2k-factorial design. The percentage difference is only 0.87% higher than ITRS 2013 prediction for low power (LP) requirement in the year 2020.

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