Challenges for 0.13µm Generation Shallow Trench Isolation on 0.18µm Equipment Platform

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***Abstract*— In order to stay competitive, the industry needs to process lower technology node from CMOS 0.18µm to 0.13µm on similar equipment platform. This will avoid at least USD 50 million CAPEX. The adaptation of lower geometry technology in older equipment platform is very challenging as similar approach can lead to yield loss to the wafer, hence not meeting the business requirement. This paper presents an integration engineering approach to enable process capability that meets circuit probe sort yield. The experiment will use series of 200mm wafer process equipment, KLA-Tencor 2367UV/Visible bright-field inspection system and data Power yield management systems to understand the root cause and implement new solution. The study found that the process recipe for shallow trench isolation (STI) deposition void that causes poly stringer defect is the stoppage for 0.13µm qualification on the 0.18µm equipment. Further defect formation will be discussed also. This paper reveals various process optimizations and re-designs of the STI layout with Optical Proximity Correction (OPC) tagging approaches that have been evaluated to eliminate the defects. The results from this paper demonstrate that a successful improvement method is able to qualify the CMOS 0.18µm to 0.13µm on similar equipment platform with outstanding sort yield.**

***Index Terms*— Shallow Trench Isolation (STI); Optical Proximity Correction (OPC); Complementary Metal-oxide Semiconductor (CMOS); Semiconductor Fabrication.**

I. INTRODUCTION

Semiconductor fabrication facilities (fabs) is one of the most capital intensive [1][2][3] and complicated industries and it is driven by Moore's Law for cost reduction and technology enhancement. In order to sustain semiconductor business, the industry needs to improve its competitiveness by enabling similar equipment platforms to enable more new advance technology capabilities [4] with good process margin and yield. This is the most challenging approach, but it results in a very minimum capital expenditure. As the technology scaled down from 0.18µm to 0.13µm in 200mm wafer fabs, the equipment platform has offered many new challenges for semiconductor manufacturing. The systematics wafer edge yield loss is one of the major yield loss contributions [3][4][5][6] due to process margin and equipment capability during initial technology development. A review on the 0.13µm technology process integration [7] showed that the edge fallout due to High Density Plasma (HDP) deposition void at the special Shallow Trench Isolation (STI) wall structure causes poly stringer after poly deposition process.

Shallow Trench Isolation (STI) is an integrated circuit feature that prevents electrical current leakage between the adjacent semiconductor device components. The STI integration process starts from the masking on the pad nitride and after the dry etch process to form the active island and shallow trench. Wet cleaning process is then applied to remove the polymer or residue on the side wall of shallow trench that was generated during the dry etch process. Liner oxidation processes are included in this stage to control the STI corner rounding to reduce the junction leakage and fix the damaged induced during STI plasma dry etch. The trench will be filled with the high density plasma oxide material and planarization by Chemical Mechanical Polishing (CMP) process. Pad nitride will be removed using phosphoric acid to form the STI structure as shown in Figure 1.

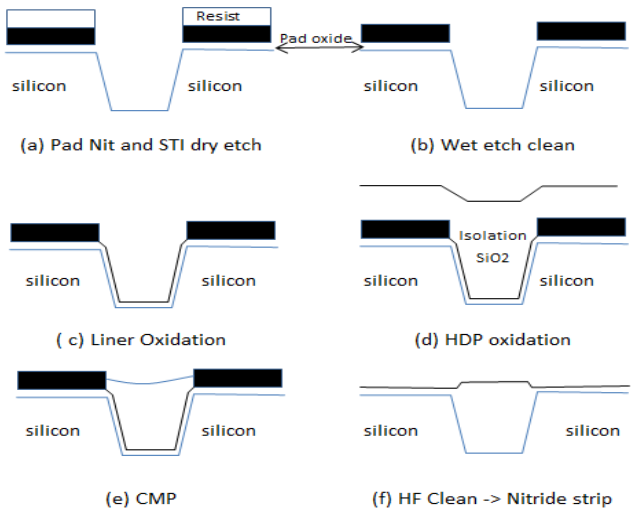


Figure 1: Generic STI process scheme [8]

The isolation aspect ratio scaling has been studied in order to provide a better isolation between the two semiconductor devices. Figure 2 illustrates a typical aspect ratio scaling from the 0.25µm to 0.07µm technology nodes in current semiconductor industry. The aspect ratio is increased by 66% from 0.18µm technology to 0.13µm technology in order to maintain the junction capacitance [9]. In contrast, the aspect ratio scaling for both semiconductor devices N+/N+ and

P+/P+ spacing is primarily driven by the HDP gap-fill capability of the process and equipment. During the gap-fill capability evaluation, it is very important to understand the aspect ratio of the minimum design rule. This is determined by the ratio of the sum of the STI trench depth and pad nitride thickness to the minimum space design rule critical dimension.

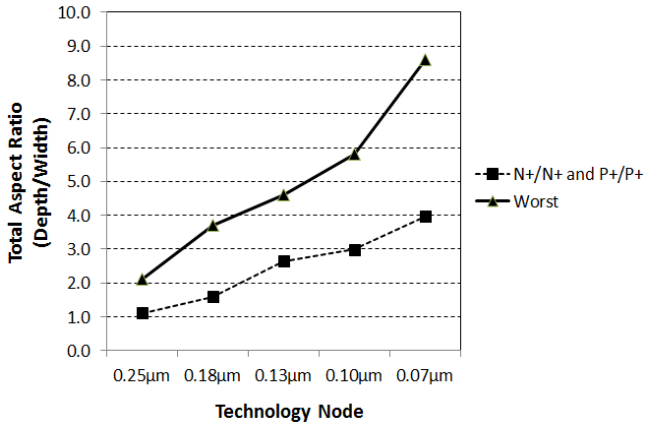


Figure 2: Isolation Aspect Ratio Scaling [9]

High Density Plasma (HDP) and Chemical Vapor Deposition (CVD) is the industry standard for STI oxide. It is full with high aspect ratio trenches due to its topography compatibility with CMP process and seamless void free for tight trench geometry. Gap-fill improvement strategies using HDP has been discussed by various authors [10][11][12]. Most of the researches emphasized the optimization of the deposition to sputter (D/S) ratio [13][14] and aspect ratio for better gap-fill capability. However, little research has been done on the STI three sides wall structure for the gap-fill mechanism. Therefore, this study will explore further understanding on the interaction impact between STI three sides wall structure, aspect ratio and D/S ratio to the wafer edge systematic yield loss.

II. Methodology

The methodology is defined in Figure 3 and it is divided into four main parts, which are the data collection and validation, yield loss investigation and characterization, process improvement and process implementation [15][16].

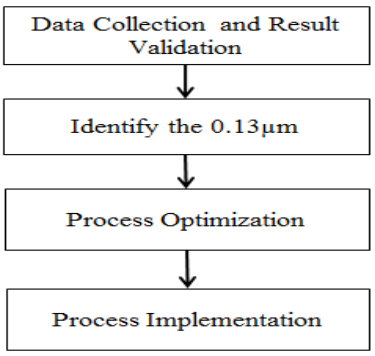


Figure. 3: Workflow for Low Yield Investigation and Process Qualification

A. Data Collection and Result Validation

Two high runner 0.13µm technology devices, L1 and K8 were selected in this study. In order to make a conclusive result, a total of 3000 wafers per device were retrieved from the dataPower yield management system to be used in this study and all of the results were validated by sort test. Based on the sort test result, 1000 low yields wafer were identified and they were used in this study.

B. The 0.13µm Main Yield Loss Identification

Based on the 1000 low yielding wafers, the failure bins base was reordered in a decreasing order and the top three failure bins signature with cumulative wafer sort map were analyzed. Once the failure signatures were identified, the correlation analysis was conducted with electrical parametric, inline measurement and inline inspection based on wafer levels. This approach helps to identify any strong correlating parameters to the failure bin. The next level was to analyze the wafer position tracking by lot level. This technique was used to identify the affected process steps and tools at the chamber level based on the lot failure pattern such as bimodal, continuously increasing or decreasing by wafer sequence failure signatures. This technique is capable of tracking wafer position at the individual process and equipment throughout the entire process that consists of at least 400 process steps on 0.13µm technology. Unique wafer positional histories were recorded for all wafers throughout the entire fabrication process to resolve most of the elusive sources of yield loss and process variation. Analysis of the equipment commonality and physical failure was tabulated to identify the root cause of the yield loss. The results based on the above investigation techniques are shown in Figure 4.

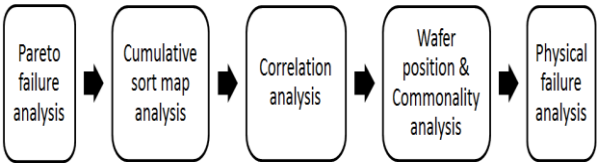


Figure. 4: Workflow for Low Yield Investigation Techniques

C. Process Optimization

This stage started with the process mapping and Cause-of-Effect Fish Born diagram to narrow down the most significant yield loss impact process. The process evaluation and characterization were conducted based on the Design of Experiment (DOE) technique. Inline defect inspection using high sensitive KLA-Tencor 2367UV/Visible bright-field inspection system, electrical parametric test and sort test are used to validate each experiments performance as illustrated in Figure 5.

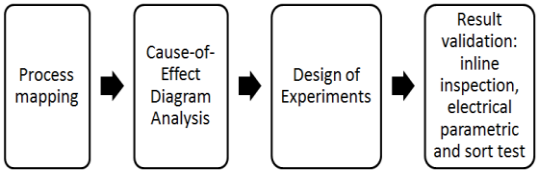


Figure. 5: Process Optimization Workflow

D. Process Implementation

Figure 6 shows the process implementation process workflow. A pre-requisite action is to verify that the new optimization process achieves good process margin. The process qualification must be planned to confirm the process margin, equipment capability and device reliability performance [15]. At the initial stage, a plan with a conditional release of small quantity of a device with new optimized process for process stability validation is implemented. Inline measurement, inline inspection, electrical parametric and sort test verification are the final condition before it is released to other 0.13µm technology devices. New process is released after the process capability confirmed that good margin is achieved by the multi devices.

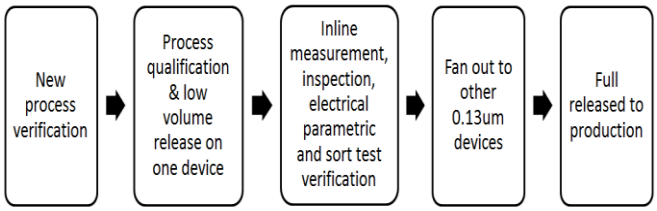


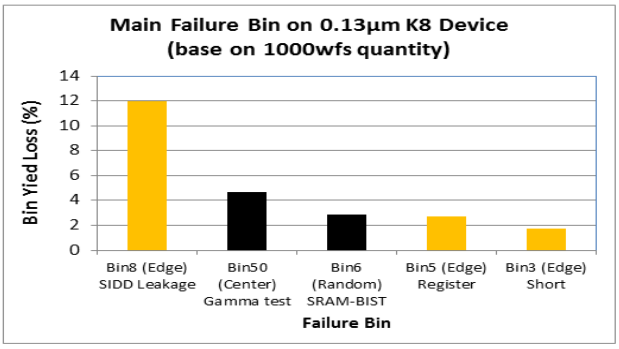
Figure. 6: Process Implementation Workflow

III. Result And Discussion

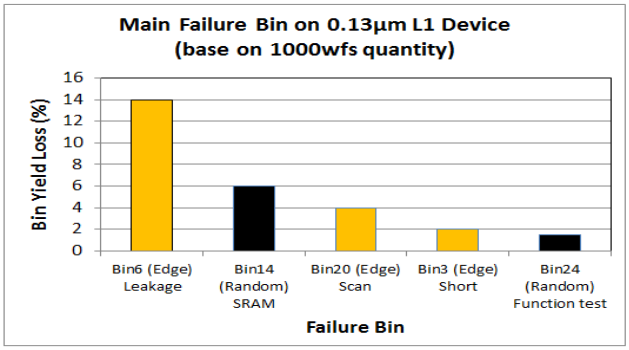
A. 0.13µm Technology Main Yield Loss Identification

In this research, two 0.13µm high runner production devices with 1000 low yield wafers validated by sort test were selected. The analysis was based on the high major failure bins, failure signatures and cumulative sort map. Figure 7 shows the failure sort bins Pareto Chart for both devices L1 and K8. Both devices showed wafer edge with high static leakage failure, which is the main contribution for the yield loss on 0.13µm technology. A detail sort map correlation analysis of the inline inspection was conducted to validate the source of the wafer edge yield loss, as shown in Figure 8. Both sort test maps in Figure 8a and inline defect inspection data map in Figure 8b are well correlated with the top view SEM images in Figure 8c. This shows that the yield loss was due to deposition void that was detected after the pad nitride strip process. On the top view SEM images, it was also observed that the deposition void defect only happens on the special STI wall structure with a specific direction.

In order to validate the failure mechanism, the Scanning Electron Microscope (SEM) physical failure analysis was performed. The cross section SEM, as shown in Figure 9 indicates that the main root causes of the edge leakage failure is due to Poly stringers and the defect was formed due to deposition void. The deposition void happened during the HDP oxide deposition and poly filled into the void during subsequent poly deposition process. This caused the device leakage and the stringers short between two semiconductor devices. The deposition void that happens in 0.13µm and below technology nodes are mainly due to high aspect ratio requirement with the tight STI spacing and high deposition to physical sputter (D/S) ratio because of the process and equipment hardware capability. Wafer edge observed more deposition void because wafer edge sputtering rate is lower compared to the center, resulting in high D/S ratio.

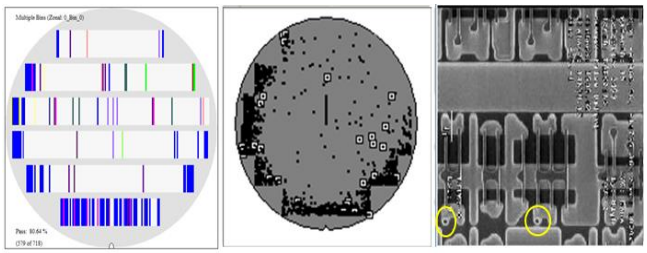


(a) Bin Loss Pareto for K8 device



(b) Bin Loss Pareto for L1 device

Figure 7: Yield loss Pareto Chart (a) Product K8 and (b) Product L1



(a) Sort Map (b) Inline Inspection Map (c) Inline SEM TopView

Figure 8: Sort map to inline inspection correlation study (a) Sort Yield Binmap, (b) Inline Inspection Defect Map and (c) Inline SEM TopView

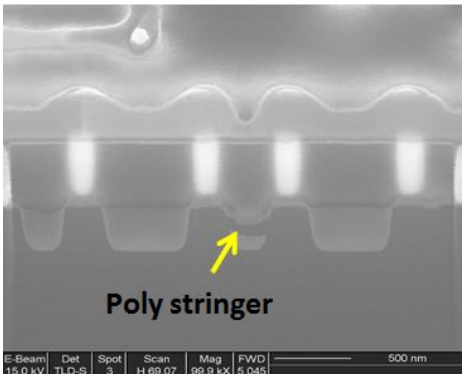


Figure 9: Cross- section SEM image showing poly stringers defect

On the top view of the SEM images as shown in Figure 10, it is observed that the deposition void defect only happens on the wafer edge special STI wall structure with specific direction. At the right side of the wafer, the deposition void defect was observed on the left side of the STI wall structure only. However, at the left side of the wafer, the deposition void existed on the right side of the STI wall structure. Deposition void happened on the special STI wall structure are due to deposition and re-deposition that is managed by sputter component. Lower re-deposition rate happened on the affected STI wall structure during HDP CVD oxide deposition process.

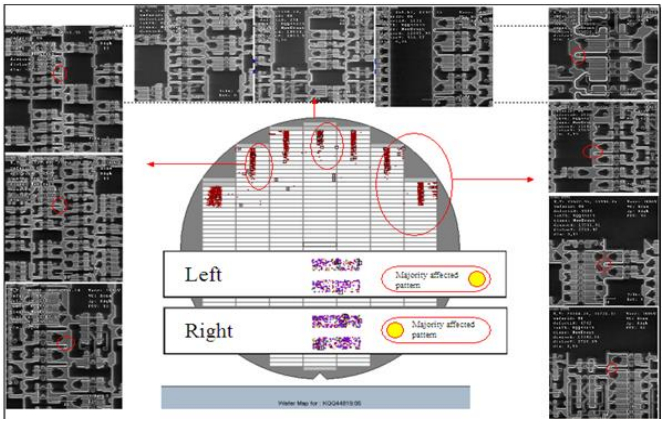


Figure 10: Void only seen at wall structure with special direction

B. Process Characterization and Optimization

Experiments were carried out on 200mm Applied Materials Centura Utima HDP-CVD reactors. It consists of two RF coils which allow the independent turning of the plasma in order to achieve a good uniform density across the wafer. The wafer was biased negatively with respect to the plasma to provide energy for ion sputtering. Generally, the process chemistries used in HDP-CVD includes SiH_4, O_2 and diluents such as Ar, He and H_2. During the deposition process, the wafer was not chucked and the backside helium cooling was not implemented.

HDP-CVD gap-fill improvement literature [12] can be categorized into two approaches, which are the aspect ratio and the deposition to physical sputter (D/S) ratio. In this study, a special STI wall structure OPC tagging approach is included to resolve the deposition void issue.

Aspect ratio process optimization: The aspect ratio of a STI trench gap is defined by the ratio of the trench height or depth to its width. HDP-CVD oxide gap-fill capability with the deposition and re-deposition process is primarily driven by the aspect ratio. A lower the aspect ratio provides a good gap-fill capability. STI spacing split evaluation was conducted to understand the impact of the gap-fill capability. Based on the experimental result as shown in Figure 11, the deposition void defect was improved by increasing the STI spacing and it was in line with previous study [14]. By increasing the STI space, the active island of the semiconductor device is reduced and gives impact to the semiconductor device performance especially on the narrow width semiconductor device, where the active island critical dimension is one of the sensitive parameters to control the semiconductor device performances. In order to minimize the impact of the semiconductor device performance, 3nm of STI space is increased at the wafer edge.

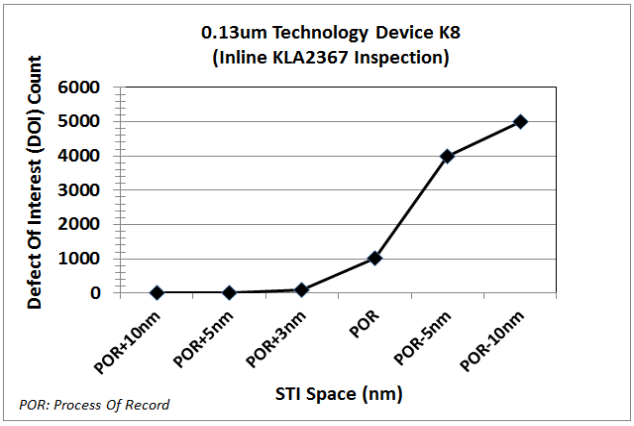


Figure 11: Deposition void defect count vs STI spacing performance

Deposition to physical sputter (D/S) ratio process optimization: HDP-CVD oxide deposition process is happens at the deposition and sputtering simultaneously. The deposition due to ions and neutrals contributes to bottom-up films with a very little sidewall growth. The sputtering ion bombardment was generated by an RF electrode power. The deposition to sputtering rate ratio (D/S) is an important measure of the gap-filling capability of the processes. The ratio is defined as below:

$$\frac{D}{S} = \frac{(net\_deposition\_rate + sputtering\_rate)}{sputtering\_rate} \quad (1)$$

In general, the use of a lower D/S ratio is for higher aspect ratio structures. Figure 12 shows a high net deposition rate at the wafer edge because the design of the equipment hardware is such that SiH_4 gasses flows from the wafer edge to the center. As a result, the wafer edge deposition rate is high compared to the center region. Figure 13 shows a low sputtering rate at wafer edge. The RF coil that generates RF plasma is located at the center of the chamber. This results in high sputtering rate at the center compared to the wafer edge. The interaction of the high deposition rate and low sputtering rate at the wafer edge results in the formation of voids.

With a detail understanding of the combination effect on aspect ratio and D/S ratio at wafer edge, the deposition void happen at the wall structure are explained in Figure 14. Assuming that the structure at 9 o'clock wafer edge position during the deposition process, the right side of trench received a higher sputtering rate that comes from the direction "A1", where the trench does not have any material for this source to sputter. While at the weak direction "A2", the low sputtering rate caused less re-deposition into the trench. As the result, deposition void happened at the right trench due to high D/S ratio. At the left side of the trench, it received a higher sputtering rate from the direction "B1" and met at the corner of the trench; hence, it generated a strong re-deposition into the bottom of the trench. Good deposition was received at the left side with low D/S ratio. Table 1 provides a deposition

void versus structure orientation summary which matches to the hypothesis.

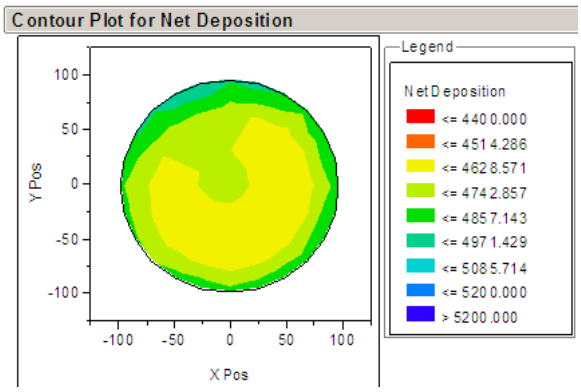


Figure 12: Net deposition rate contour wafer map

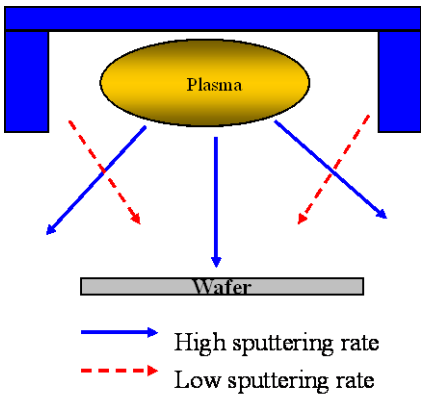


Figure 13: Plasma sputtering layout

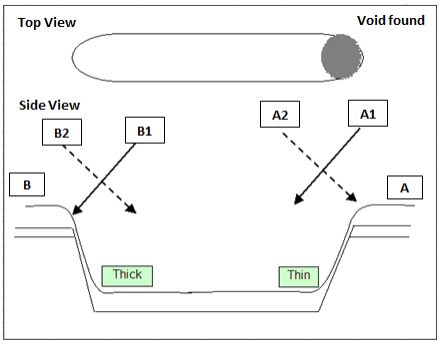


Figure 14: Gap-fill mechanism at STI wall structure

The deposition void can be addressed by increasing the RF bias power, which also increases the directional deposition and re-deposition. In high aspect ratio technology like 0.13µm node, the HDP-CVD deposition is divided into two steps: The first step is for gap-fill with low deposition rate process and second step is used for deposition with high deposition rate. In this study, the focus is on the first step that is, the use for gap-fill. Table 2 shows that an increment of the bias RF power that increases the sputtering rate or a reduction of the side SiH_4 gasses that reduces the deposition rate provide better gap-fill with low deposition void defect. This is aligned with the low D/S ratio that has good gap-fill capability. The change of the SiH_4 gas flow will change the oxide films properties, which may affect the device performance and result in longer process qualification time; therefore, increasing the bias RF power process. A more cost effective solution was selected. DOE was conducted with different bias RF power to understand the impact of the bias RF power.

The results show that the deposition void defect was not significantly reduced once the bias RF power beyond 300watt. This is because of the deposition and sputtering ratio balancing. From the experimental results, we can conclude that the additional 300watt bias RF power increased the re-deposition process and can improve the gap-fill process margin, but it did not fully resolve the deposition void issues.

Table 1
Summary of deposition void vs structure orientation

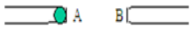
Structure Orientation	Remark
	• Assume structure at 9 o'clock location wafer position. • Structure "A" orientation has less impact gap fill but structure "B" has high gap fill impact.
	• Assume structure at 9 o'clock location wafer position. • Structure "A" orientation has more impact gap fill but structure "B" gap fill performance is good.
	• Assume structure at 12 o'clock location wafer position. • Structure "A1" and "A2" orientation has more impact gap fill void compared to "B1" and "B2"
	• Assume structure at 6 o'clock location wafer position. • Structure "A1" and "A2" orientation has more impact gap fill void compared to "B1" and "B2"

Table 2
Summary of HDP CVD process parameters vs DOI defect on K8 device

HDP-CVD Process Parameter	Inline Inspection Performance (DOI Defect) - Count
Bias RF (+300watt)	10
Bias RF (-300watt)	>5000
O_2 flow (+10sccm)	123
O_2 flow (-10sccm)	80
Side SiH_4 (+5sccm)	>5000
Side SiH_4 (-5sccm)	200

As shown in Figure 17, with the commination approach of aspect ratio and deposition to sputtering ratio, the sort yield improved by 2%. However, the wafer edge special STI wall structure deposition void defect is still not fully eliminated. This is due to the capability of the current HDP-CVD equipment. The next approach is to focus on the special STI wall structure design layout optimization.

STI wall structure design layout (Tag2A) optimization: Deposition void only happens at the wafer edge STI wall structure with special direction, as shown in Figure 10. This study focuses on the custom tagging of the weak STI structure with Mentor Graphics' Calibre CAD. Tagging is the function of post Optical Proximity Correction (OPC) applied to the unique structures with additional pre-defined rules [17]. To

prevent the post OPC STI tagging impact, the device performance is integrated with the process margin with some special rules are defined as below:

- Tagging is only allowed on STI wall structures that the line end pass the minimum design rule requirement.
- STI Wall structure overlay with Poly is not allowed to do the tagging.
- Post OPC STI tagging is required to pass the technology minimum design rule requirement, especially the contact to island overlap.

Custom post OPC STI tagging Tag2A is shown in Figure 15. Considering that the spacing of the special STI wall structures has increased by around 20nm, it has significantly reduced the STI aspect ratio and improved the HDP gap-fill capability. An experiment was carried out to understand the interaction of STI gap-fill capability on the new post OPC STI customs tagging structure Tag2A. Table 3 summarizes the interaction of engineering split results which shows that the deposition void defect was not fully eliminated, but was optimized with STI spacing and HDP-CVD bias RF. With the combination of Tag2A STI new optimized wall structure, the deposition voids defect was fully eliminated with good process margin; hence, overcoming the equipment capability. In order to increase the confident level of this new custom Tag2A STI wall design, multi 0.13µm devices were tape-out and inline inspection confirmed that all the devices that received the new process are clean of deposition void defect, as shown in Figure 16.

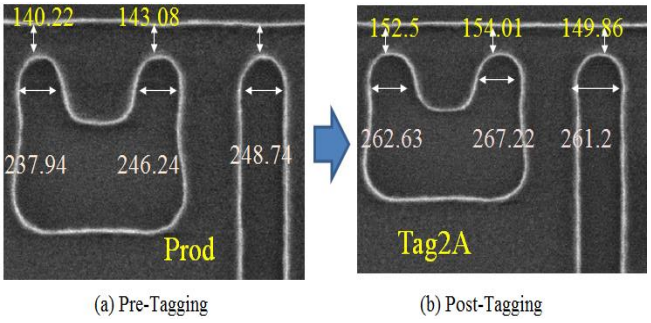


Figure. 15: Special wall structure with custom OPC tagging (a) Pre-Tagging and (b): Post-Tagging

Table 3
Summary of engineering split on STO OPC tagging. STI spacing and HDP-CVD process condition on K8

Island OPC	STI Spacing	HDP-CVD	Inline Inspection Result (DOI Count)
Old	POR	POR	120
Old	POR	POR+300W Bias RF	18
Old	POR-7nm	POR	>5000
Old	POR-7nm	POR+300W Bias RF	100
Tag2A	POR	POR	0
Tag2A	POR	POR+300W Bias RF	0
Tag2A	POR-7nm	POR	0
Tag2A	POR-7nm	POR+300W Bias RF	0
Tag2A	POR-11nm	POR	10
Tag2A	POR-11nm	POR+300W Bias RF	0

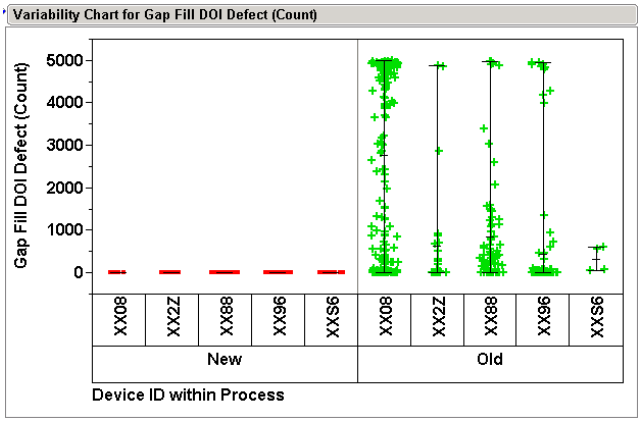


Figure 16: New process versus old process STI gapfill performance by devices

C. *Process Implementation*

The new optimized process that consists of Tag2A post OPC tagging on special STI wall structure increased the wafer edge 3nm STI spacing and an increase of 300watt HDP bias RF power process was proven and validated to solve the wafer edge deposition void defect with good process margin. Process and device qualification with three different lots were conducted and it passed the requirements. Small volume 125 wafers were released on one high runner K8 0.13µm device for inline process stability check, inline measurement, inline defect confirmation, electrical parametric and sort test verification. The test result passed all the device specification requirement and sort yield improved by 10% compared to old process. The new optimized process was fanned out to other 0.13µm devices L1 and X5. All inline performances were validated and it passed all the inline and Electrical test specification requirement and free of deposition void defect. 250 wafers sort test that run on a new optimization process was validated with yield improving by 10%, as shown in Figure 17.

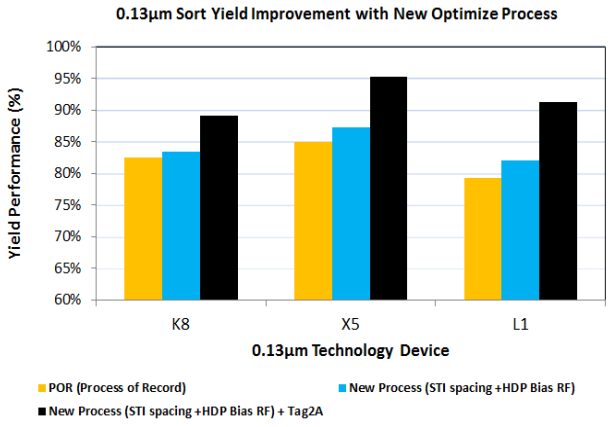


Figure 17: Sort yield performance of Process of Record (POR) versus New Process

IV. CONCLUSION

In this study, wafer edge yield optimization for 0.13µm devices processed on 0.18µm equipment platform had been successfully implemented. Wafer edge deposition void at the special STI wall structure was identified as the main contributor for the 0.13µm technology device edge yield loss. Aspect ratio and deposition to sputter (D/S) ratio that were correlated to the gap-fill capability were studied. Through re-optimization, the RF biasing for STI HDP process increased the re-deposition rate and reduced the wafer edge aspect ratio with an increasing STI spacing. Both processes have improved the gap-fill capability but not fully solved the wafer edge deposition void defect on special STI wall structure. This new process was combined with the Tag2A post OPC tagging on the special STI wall structure: The results show successful elimination of the wafer edge deposition void defect with good process margin on current 0.18µm HDP-CVD equipment platform. In order to increase the confidence level on the new optimized process, it was implemented on a few higher runner 0.13µm devices. Inline inspection and sort yield validation on 250 wafers confirmed that the new optimization process eliminated the wafer edge deposition void issue and sort yield improved by 10% compared to the old process. These findings have enabled the 0.13µm technology to be processed at the 0.18µm technology equipment platform.

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