Design and System C-AMS Modeling of a Parallel Direct Digital Synthesizer

Atman Jbari[1], Larbi Bellarbi[1], Abdelhamid Errachid[2]
[1]*Electrical Engineering Research Laboratory, High School of Technical Education (ENSET), Mohammed V University, Rabat, Morocco*
[2]*Claude Bernard-Lyon 1 University, Laboratory of Analytical Sciences, France*
atmjbari@gmail.com

***Abstract*— This paper presents a new parallel direct digital frequency synthesis (PDDS) circuit providing simultaneous multichannel. The proposed circuit has several applications in instrumentation, identification and data communications. After analysis of a set of design architectures and their limitations, we opted for a rapid and optimized architecture using Wave Arithmetic Unit (WAU) to operate in a largest frequency range. The effectiveness of our proposed circuit is demonstrated by a high-level design of digital blocks in SystemC and analog blocks in SytsemC-AMS language. Finally, the analysis of result responses of all modules confirms the correct PDDS performances for an open microelectronic integration technology.**

***Index Terms*— Direct digital synthesis, multiplexing blocks, signal approximation, spectral analysis, SystemC modeling, SystemC-AMS modeling.**

I. INTRODUCTION

Direct Digital Synthesis (DDS) aims at producing many different frequencies from a single stable digital source. It has been an important area of scientific research in the last few years, given its several applications: instrumentation [1]-[3], biomedical engineering [2]-[3] and telecommunications [4] [5]. The challenges of design techniques and methods include a high level of spectral purity, low power consumption, and high output frequencies [8] [9]. In addition, the complexity of applications in the multiple input-multiple output context requires a new circuit, which can produce a parallel and multichannel frequencies [10]. Therefore, our present work fits into the general field of digital synthesis techniques known as DDS (Direct Digital Synthesis). In the following subsection, we will recall the principle of DDS.

A. DDS principle

To illustrate the principle of DDS, we give the main structure in Figure 1, where the components are:

- *Phase Accumulator:* provides the time reference of the waveform as memory address for reading the instantaneous values.
- *Waveform Memory*: contains samples of the waveform to be synthesized.
- *D/A Converter*: converts each digital value into its proportional analog voltage.
- *Low-Pass Filter:* limits the spectrum of the synthesized wave at the Nyquist bandwidth related to the operating clock frequency F_{CLK}.

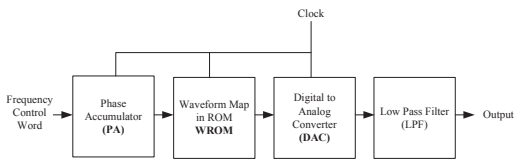

Figure 1: General structure of single output DDS [6]

The output frequency F_{OUT} depends on the reference clock frequency F_{CLK}, the frequency control word FCW and the size of the phase accumulator N, by the following expression [10][11]:

$$F_{OUT} = \frac{FCW}{2^N} F_{CLK} \quad (1)$$

Since the sine function is even relatively to $\frac{\pi}{2}$ and odd compared to π, the size of the data memory can be reduced by a ratio of 4. Thus, the phase accumulator-memory data association can be designed as depicted in Figure 2. To illustrate the role of each block, Fig.3 gives an example of intermediate signals for the following parameters: frequency control word $FCW = 40$; phase accumulator size: $10\ bits$; wave memory: 1024 words of 10bits; D/A converter: $10 bits$; and a low-pass filter. In this example, the complete wave period corresponds to the complete cycle of phase accumulator, and consequently the direct control of its frequency.

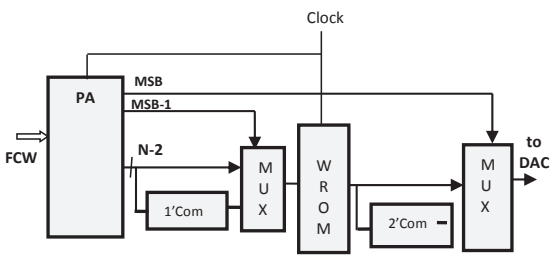

Figure 2: Phase Accumulator-ROM association [12]

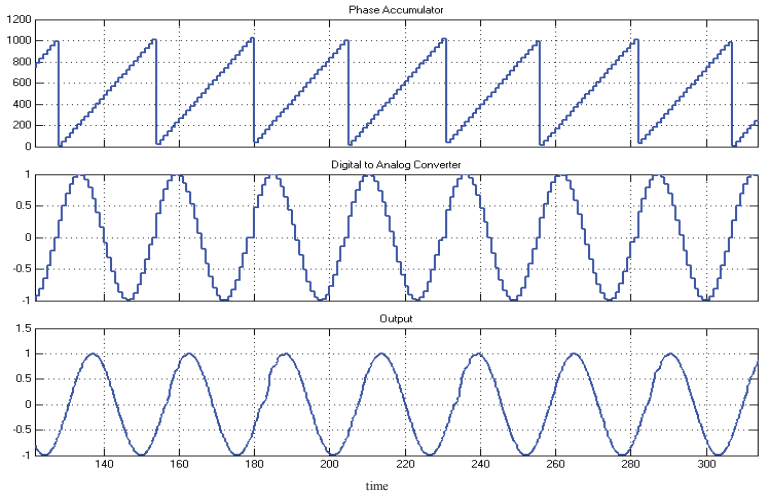

Figure 3: Example of single output DDS signals

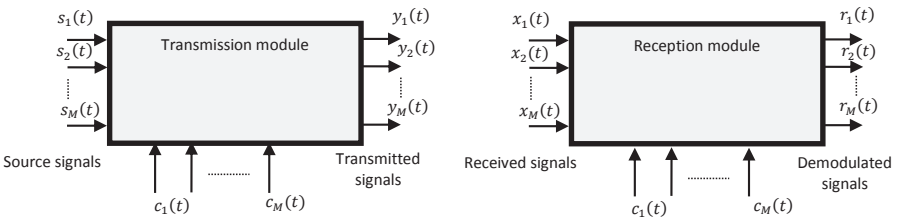

Figure 4: Parallel multicarrier modulation or demodulation for communication systems

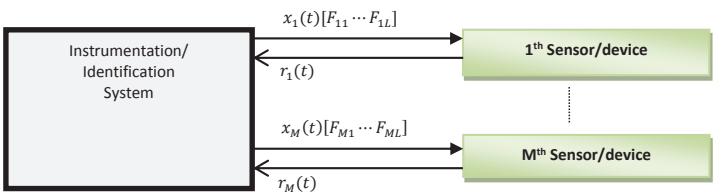

Figure 5: Parallel frequency identification or characterization of a set of sensors/devices

B. Parallel DDS and motivations

The main advantages of DDS technology are: high accuracy, stability, very low resolution, and precise control of the frequency change. In literature, the DDS circuits provide one output and several non-simultaneous channels. However, many applications such as simultaneous characterization of array sensors, radar objects tracking or analysis of data transmitted from several stations require the parallel production of multiple carriers whose frequencies have to be included in a dynamic analysis band [11]. Fig.4 shows an example of parallel modulation of sources $(s_1(t) \cdots s_M(t))$ and parallel demodulation of received signals $(x_1(t) \cdots x_M(t))$ that requires the parallel generation of local carriers $(c_1(t) \cdots c_M(t))$

Moreover, the identification or the study of frequency characteristics of a sensor or device, as shown in Fig.5, requires also L channels for each sensor due to the diversity of physical parameters. The main aim of this work is to respond to this demand by the proposal of a new DDS circuit. This circuit contains several outputs working in simultaneous

channels with different frequencies and modes. Our main contribution is to propose a new architecture of PDDS (Parallel Direct Digital Synthesizer) circuit and its SystemC/SystemC-AMS modeling. The functional diagram is shown in Figure 6, where input/output lines are used to define control words $DATA\_FREQ$, control signals to select channels and set internal operating modes and then to produce M outputs with L channels in synchronization with the reference clock CLK.

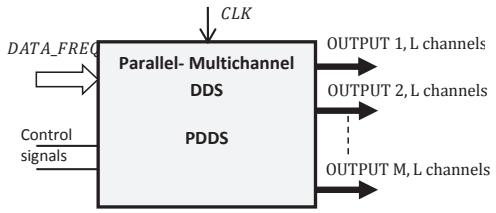

Figure 6: General description of the proposed PDDS circuit

The rest of this paper is structured as follows. Section II gives the formulation and comparison of design architectures. Section III describes a PDDS-4 circuit and its configuration. In section IV, we present a SystemC/SystemC-AMS modeling and performances evaluation. Finally, we conclude on potential applications of our proposed PDDS circuit.

II. Formulation and Design Architectures

The main function of PDDS circuit is to produce a set of M parallel outputs based on the same conventional structure: Phase Accumulators, a single sample ROM, Digital to Analog Converters and Low Pass Filters. For PDDS activating, a clock signal CLK is used to synchronize the evolution of each block according to rising or falling edges. We can distinguish two modes of synchronization:

A. Simultaneous synchronization

In this mode, all phase accumulators update their values at the same time $n \times \mathrm{T_{CLK}}$ with respect to Equation 2:

$$PA_i(nT_{CLK}) = PA_i\big((n-1)T_{CLK}\big) + FCW(i) \tag{2}$$

Thus the frequency of each output OUT_i is expressed as:

$$\mathrm{F_{OUT}}(i) = \frac{FCW(i)}{2^N}\ \mathrm{F_{CLK}} \tag{3}$$

B. Shifted synchronization

In this mode, the M phase accumulators update at different times $(nM + i) \times T_{CLK}$ by period of $M \times T_{CLK}$ according to Equation (4):

$$\mathrm{PA_i}\big((\mathrm{nM} + \mathrm{i})\mathrm{T_{CLK}}\big) = \mathrm{PA_i}\left(\big((\mathrm{n} - 1)\mathrm{M} + \mathrm{i}\big)\,\mathrm{T_{CLK}}\right) + \mathrm{FCW(i)} \tag{4}$$

This induces a delay of $M \times T_{CLK}$ at each output OUT_i. Then, the frequency becomes:

$$\mathrm{F_{OUT}(i)} = \frac{\mathrm{FCW(i)}}{\mathrm{M} \times 2^{\mathrm{N}}}\ \mathrm{F_{CLK}} \tag{5}$$

According to the two modes of synchronization, we propose the following design architectures:

A. Parallel Architecture

The direct design architecture of PDDS circuit is to operate separately on parallel DDS structures in addition to a configuration block as seen in Figure 7. This architecture has the advantage of the wider band frequency compared to F_{CLK} at the expense of the memory size, which is a multiple of the number of outputs.

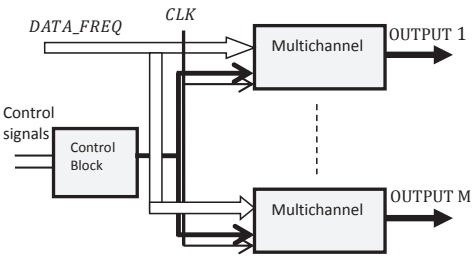

Figure 7: Parallel PDDS architecture

B. Multiplexed Architecture

To optimize the number of memories and then the semiconductor space, we have a phase accumulators multiplexing blocks (PA_1, …, PA_M, MUX) and demultiplexing block of data in a single memory as shown in Figure 8. Afterward, the obtained data are converted into analog signals and followed by a Low Pass Filter (DAC+ LPF) according to the standard structure of a DDS circuit.

C. Wave Arithmetic Architecture

The main drawback of the multiplexed architecture is to reduce the required speed by the number of outputs. In order to keep the same speed of the parallel architecture which is the maximum frequency of the clock signal, we propose to replace the wave memory by an arithmetic unit, which we denote WAU (Wave Arithmetic Unit), as shown in Figure 9. The role of this WAU unit is to provide a parallel computation of the sine value $\sin\left(2\pi \times \frac{PA_i}{2^N}\right)$ of each input phase PA_i.

In [7][8][13][14][15], many approximation methods have been used to compute the sine value and to propose a ROM-less design architecture. Basically, the solution corresponds to use mathematical expressions based on trigonometric properties or polynomial developments. In this way, the sine value of phase θ is computed by Taylor's series up the n^{th} order written as:

$$\sin\theta = \sum_{k=0}^{n} (-1)^k \frac{\theta^{2k+1}}{(2k+1)!} \tag{6}$$

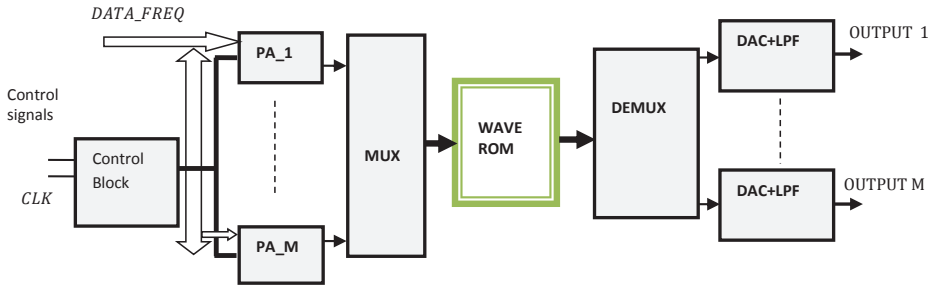

Figure 8: Multiplexed PDDS architecture

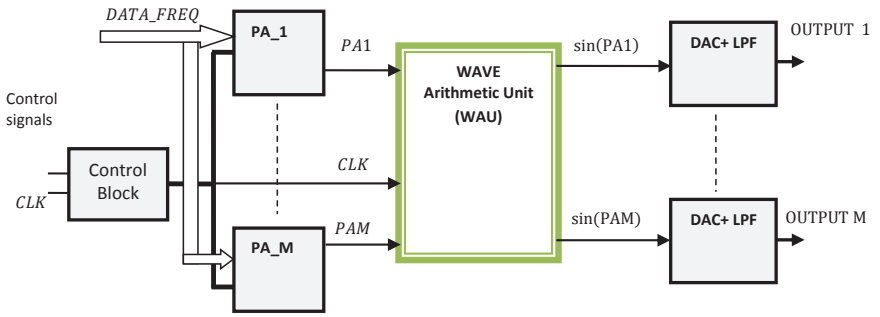

Figure 9: The proposed Wave Arithmetic PDDS architecture

To decrease the computation error for high phase values, it is important to increase the series order, which requires more adders, multipliers and consequently more computation time. In [13], an efficient hybrid polynomial approximation method was proposed to minimize the total residual error TRE between $\sin\theta$ and its approximation function (θ) . This TRE is expressed as:

$$TRE = \int_0^{\frac{\pi}{2}} \left(\sin\theta - f(\theta)\right)^2 d\theta \qquad (7)$$

Therefore, the approximation function can be expressed as follows [18]:

$$f(\theta) = \begin{cases} \alpha_{10}\theta & ,0 \le \theta \le \frac{7\pi}{128} \\ \alpha_{24}\theta^4 + \alpha_{23}\theta^3 + \alpha_{22}\theta^2 + \alpha_{21}\theta + \alpha_{20} & ,\frac{7\pi}{128} \le \theta \le \frac{\pi}{2} \end{cases} \qquad (8)$$

where the coefficients are:

$$\alpha_{10} = 0.9970862,$$
$$\alpha_{20} = 0.0011854, \alpha_{21} = 0.9894410,$$
$$\alpha_{22} = 0.0330064, \alpha_{23} = -0.2134780,$$
$$\alpha_{24} = 0.0312845.$$

To improve the computation precision of Taylor approximation method, we propose to subdivide the interval $\left[0 \quad \frac{\pi}{2}\right]$ into r subintervals. For this purpose, the sine function will be computed for each phase $\theta_i \le \theta < \theta_{i+1}$ around the point $\theta_i = i \times \frac{\pi}{2r}$, $i \in \{0, \cdots, r-1\}$ as follows:

$$\begin{aligned} \sin\theta &= \sin\theta_i + \sum_{k=1}^{n} (\sin\theta)'_{\theta=\theta_i} \frac{(\theta-\theta_i)^k}{k!} \\ &= a_{i,0} + \sum_{k=1}^{n} a_{i,k} \frac{(\theta-\theta_i)^k}{k!} \end{aligned} \qquad (9)$$

where:
$a_{i,0} = \sin\theta_i\,; a_{i,1} = \cos\theta_i\,;\ a_{i,2} = -\sin\theta_i\,;\ a_{i,3} = -\cos\theta_i\ ;$ and for every positive integer:
$p{:}a_{i,4p} = \sin\theta_i\,; a_{i,4p+1} = \cos\theta_i\,; a_{i,4p+2} = -\sin\theta_i\,; a_{i,4p+3} = -\cos\theta_i$.

In fact, the proposed approximation method corresponds to Taylor formula at order n referenced by the r angles of each subinterval. For the rest of the paper, we will call this method as "Taylor-REF-n/r ".

In order to compare the performances of each method, we illustrate in Fig. 10, the residual error of : Taylor-5th order, Taylor-7th Order, Hybrid polynomial approximation [13], Taylor-REF-3/4 and Taylor-REF-3/8, and also the total residual errors in Table 1. It is shown that Taylor-REF-3/8 presents least residual errors 7.949×10^{-7} providing more computation accuracy. This consequence is confirmed by the simulation results presented in Fig. 11, where the TRE decreases rapidly versus the number r of reference phases.

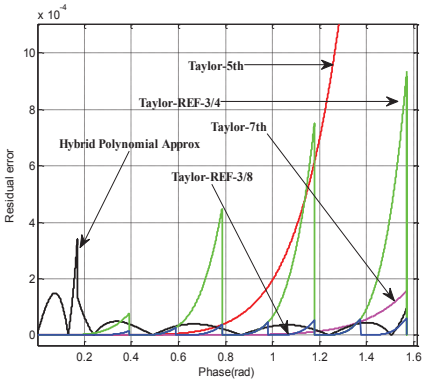

Figure 10: Residual error of five approximation methods in $\left[0 \quad \frac{\pi}{2}\right]$

Table 1
Total residual errors of approximation methods

Approximation method	Taylor-5th	Taylor-7th	Hybrid Polynomial Approx. [18]	Taylor-REF3/4	Taylor-REF 3/8
TRE	5.646×10^{-3}	5.341×10^{-6}	1.146×10^{-5}	1.856×10^{-4}	7.949×10^{-7}

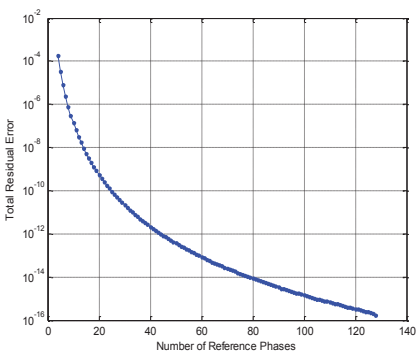

Figure 11: Total residual error of Taylor-REF-3/8 versus number of reference phases

In addition to the previous motivate consequence; we will now perform a hardware comparison. Among the most important constraints for choosing design architectures of circuit or electronic block, there are the consumption energy and semiconductor area. To this end, we summarize in Table 2, the required blocks: adders, multipliers and coefficients set to compute the sine of input phase. As a consequence, our proposed approximation Taylor-REF-3/8 involves an economical architecture because it requires the same amount of blocks (three adders and five multipliers) for different coefficients, which improves directly the approximation process.

For implementation task, we propose to illustrate the interconnection of required blocks for Taylor-REF-3/8 approximation method. The required coefficients $c_{i,k} = \frac{a_{i,k}}{k!}$ are presented in Table 3. Moreover, Figure 12 shows the design architecture of WAU block for 16 bits phase accumulator and single input- single output. First, the bit $PA(14)$ activates the 1st complement of input phase to compute symmetric value according to $\frac{\pi}{2}$. After this operation, three bits $PA(13 \cdots 11)$ constitute the address i available to select a group of required coefficients $\{c_{i,0}, c_{i,1}, c_{i,2}, c_{i,3}\}$ from multiplexers, among constant data coefficients indexed by $i = 0, \cdots, 7$. Thus, the real phase value is a vector of lower 11bits: $PA(10 \cdots 0)$. Hence, each term $c_{i,k} \times \theta^k$ will be evaluated using multipliers and adders. Finally, the most significant bit $PA(15)$ enables the 2nd complement block in order to compute the negative value corresponding to angle in the interval $[\pi \; 2\pi]$ if $PA(15) = 1$.

Generally, for PDDS-M outputs, the WAU circuit corresponds to a group of M parallel blocks according to design architecture of Fig.12. These blocks exploit the same data coefficients and run simultaneously to compute the sine value of inputs $\{PA_1, \cdots, PA_M\}$. Based on the simulation results of residual error and design architecture, we can assert that our proposed approximation method Taylor-REF-3/8 demonstrates its effectiveness to compute the sine values with high precision and optimized architecture against to related techniques.

Table 2
Required blocks of approximations methods

Approximation method	Adders	Multipliers	Coeffs.
Taylor-5th	2	5 (2 fixed coeffs, 3variable coeffs)	2
Taylor-7th	3	7 (3 fixed coeffs, 4 variable coeffs)	3
Hybrid polynomial approximation [18]	4	7 (3 fixed coeffs, 4 variable coeffs)	5
Taylor-REF3/4	3	5 (3 fixed coeffs, 2 variable coeffs)	16
Taylor-REF 3/8	3	5 (3 fixed coeffs, 2 variable coeffs)	32

III. DESCRIPTION OF PDDS-4 OUTPUTS

The objective of this section is to present the proposed PDDS-4 circuit with four outputs and two operating modes. The general description of PDDS-4 is illustrated in Figure 13.

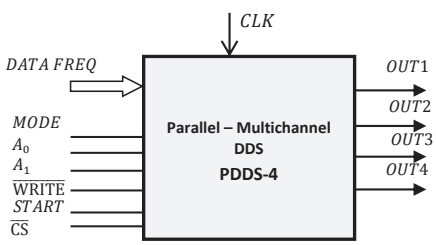

Figure 13: General description of PDDS-4

Table 3
Floating and quantized coefficients of Taylor-REF 3/8.

Reference subinterval	Floating coefficients $c_{i,k} = \frac{a_{i,k}}{k!}$	Quantized coefficients (16bits)
0	$c_{0,0} = 0;\ c_{0,1} = 1;$ $c_{0,2} = 0;\ c_{0,3} = -0.1666$	$c_{0,0} = 0;\ c_{0,1} = 32767;$ $c_{0,2} = 0;\ c_{0,3} = -5462$
1	$c_{1,0} = 0.1951\ ;\ c_{1,1}0.9808\ ;$ $c_{1,2} = -0.0975\ ;\ c_{1,3} = -0.1635$	$c_{1,0} = 6392\ ;\ c_{1,1} = 32137\ ;$ $c_{1,2} = -3197;\ c_{1,3} = -5357$
2	$c_{2,0} = 0.3827\ ;\ c_{2,1} = -0.1913;$ $c_{2,2} = 0.9239;\ c_{2,3} = -0.1540$	$c_{2,0} = 12539;\ c_{2,1} = 30272\ ;$ $c_{2,2} = -6270;\ c_{2,3} = -5046$
3	$c_{3,0} = 0.5556\ ;\ c_{3,1} = 0.8315\ ;$ $c_{3,2} = -0.2778;\ c_{3,3} = -0.1386$	$c_{3,0} = 18204;\ c_{3,1} = 27244;$ $c_{3,2} = -9103;\ c_{3,3} = -4541$
4	$c_{4,0} = 0.7071\ ;\ c_{4,1} = 0.7071;$ $c_{4,2} = -0.3536;\ c_{4,3} = -0.1179$	$c_{4,0} = 23169;\ c_{4,1} = 23169;$ $c_{4,2} = -11585;\ c_{4,3} = -3862$
5	$c_{5,0} = 0.8315\ ;\ c_{5,1} = 0.5556;$ $c_{5,2} = -0.4157;\ c_{5,3} = -0.0926$	$c_{5,0} = 27244;\ c_{5,1} = 18204;$ $c_{5,2} = -13623;\ c_{5,3} = -3035$
6	$c_{6,0} = 0.9239\ ;\ c_{6,1} = 0.3827;$ $c_{6,2} = -0.4619;\ c_{6,3} = -0.0638$	$c_{6,0} = 30272;\ c_{6,1} = 12539;$ $c_{6,2} = -15137;\ c_{6,3} = -2090$
7	$c_{7,0} = 0.9808\ ;\ c_{7,1} = 0.1951;$ $c_{7,2} = -0.4904;\ c_{7,3} = -0.0325$	$c_{7,0} = 32137;\ c_{7,1} = 6392;$ $c_{7,2} = -16069;\ c_{7,3} = -1066$

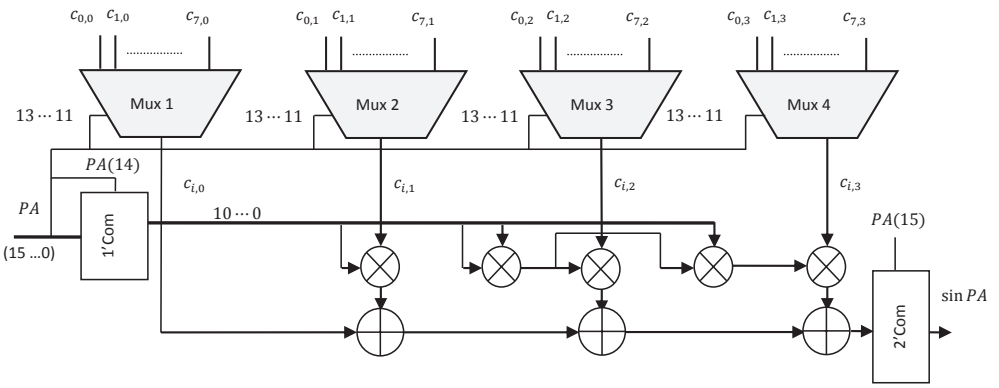

Figure 12: Architecture of the proposed WAU based on Taylor-REF 3/8.

Here we describe the different signals:

- CS: Low active signal to validate the configuration block and control words for each channel. If $CS = 1$, the outputs are set to a low level.
- $DATA\_FREQ$: Frequency control word for each channel of output.
- $MODE$: The PDDS operates on two modes:
  - *Mode 0*: Independent mode. The output channels are working independently, i.e. the frequencies are defined separately by control words ($FCW(i) = DATA\_FREQ$).
  - *Mode 1*: Dependent mode. The channels are working by step relatively to the reference channel $OUT1$: $FCW(1) = DATA\_FREQ$; $for\ k > 1$: $FCW(k) = FCW(k-1) + DATA\_FREQ$.
- A_1A_0: Address of the configuration register of each output channel. The four outputs are addressed as follows: 00: output 1; 01: output 2; 10: output 3 and 11: output 4.
- $WRITE$: Low active signal for enabling write operation of $DATA\_FREQ$, according to a rising edge of the clock signal CLK.
- $START$: High active signal to start the synthesis process by connecting the clock to all blocks of the DDS circuit. If START = 0, the outputs are set to a low level.

Figure 14 summarizes the setup process and running of the proposed PDDS-4 circuit.

IV. SystemC-AMS Modeling and Performances Evaluation

To validate the design of our PDDS-4 circuit with a wave arithmetic architecture, we have implemented the model in SystemC language for digital modules and SystemC-AMS for analog or mixed-modules, in addition to driving and verification modules. The SystemC language is widely used for modeling and verification of embedded systems [6] [16][17] [18]. Our development environment is "Eclipse software" after compiling libraries **"SystemC-2.3.1; SystemC-AMS 1.0"** followed by configuration path to active

the libraries **"systemc.h ;systems-ams.h".** Then, each block is modeled by a module with input ports, output ports, and the internal signals in addition to the processing methods according to the list of sensitivity parameters.

The modeling project is structured in such a way that for each module, there are a declaration file "name_module.h" and an implementation file "name_module.cpp" according to the following specifications:

- *Phase accumulator :* 16 bits.
- *Wave Arithmetic Unit :* Taylor-REF 3/8 for 16 bits.
- *D/A Converter* : 16 bits, supply voltage : $V_{cc} = 5V$.
- *Low-Pass Analog Filter :* defined by the transfer function model with a Chybechev type: $Fc = 200MHz$, order = 8 and passband ripple $Rp = 0.1dB$.

The construction of the top model of PDDS-4 circuit, shown in Figure 15, and it is implemented by interconnecting modules by ports and signals of type **sc_signal** or **sca_tdf :: sca_signal**.

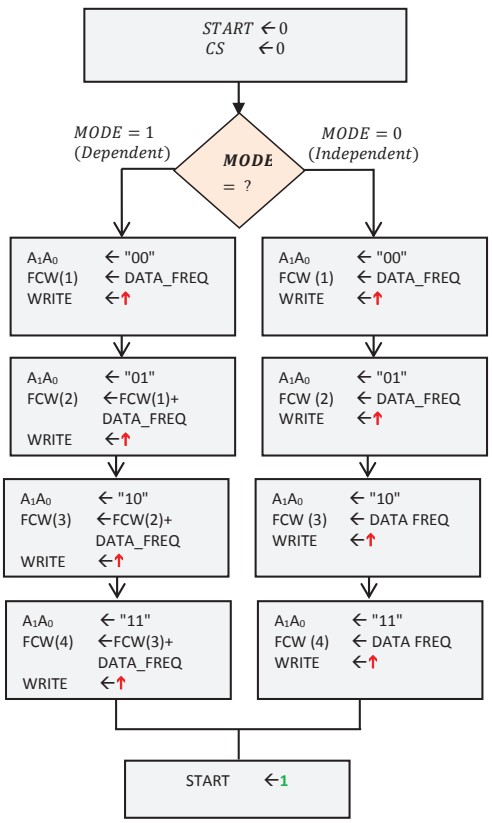

Figure 14: Configuration and running chart of PDDS-4

To evaluate the PDDS-4 model, we have built a driver module whose role was to generate 3000 clock cycles 1ns-low and 1ns-high level. Then, the frequency control is $F_{CLK} = 500MHz$, giving a frequency resolution: $R_F = \frac{500}{2^{16}} = 7.6294KHz$. In the main file sc_main.cpp, the analog modules DAC and LPF were set to the timestep of 2ns: **DAC1.set_timestep(2,SC_NS); LPF1.set_timestep(2,SC_NS)**. The instantaneous values of different signals based on the clock were stored in a csv file: **sca_util::sca_trace_file *wf2=sca_util::sca_create_tabular_trace_file ("PDDS4Result");** Finally, the result data was analyzed with MATLAB tool in two modes.

A. Independent Mode

In this mode, phase accumulators were controlled separately by the following words: $FCW1 = 5000; FCW2 = 10000; FCW3 = 20000\ and\ FCW4 = 25000$. The evolution of the phases is shown in Figure 16 over a duration of $27ns$. These phases will produce the PDDS signals in Figures 17,18,19 and 20 for outputs PDDS_OUT1, PDDS_OUT2, PDDS_OUT3, and PDDS_OUT4 respectively. In these figures, the phase accumulators increase by $5000 / T_{CLK}$, $10000 / T_{CLK}$,$20000 / T_{CLK}$, $25000 / T_{CLK}$ respectively, where the clock period corresponds to $2ns$ and a PDDS period corresponds to $2^{16} \times T_{CLK} = 131.072\mu s$.

Furthermore, content spectral with resolution bandwidth of $7.6294KHz$ is shown in Figure 21 whose fundamental frequencies are given in Table 4.

Table 4
Required blocks of approximations methods

Approximation method	Adders	Multipliers	Coeffs.
Taylor-5th	2	5 (2 fixed coeffs, 3variable coeffs)	2
Taylor-7th	3	7 (3 fixed coeffs, 4 variable coeffs)	3
Hybrid polynomial approximation [18]	4	7 (3 fixed coeffs, 4 variable coeffs)	5
Taylor-REF3/4	3	5 (3 fixed coeffs, 2 variable coeffs)	16
Taylor-REF 3/8	3	5 (3 fixed coeffs, 2 variable coeffs)	32

B. Dependent Mode

In this mode, the three outputs OUT2, OUT3 and OUT4 follow the main output OUT1 controlled by the main word: $FCW = 5000$ as a step: $Step = 4000$. The spectrum of these outputs with resolution bandwidth of $7.6294KHz$, is shown in Figure 22. We measured the following frequencies: $F_{OUT1} = 38.147MHz, F_{OUT2} = 68.664MHz,$ $F_{OUT3} = 99.182MHz, F_{OUT4} = 129.699MHz,$ and the frequency difference $30.517MHz$.

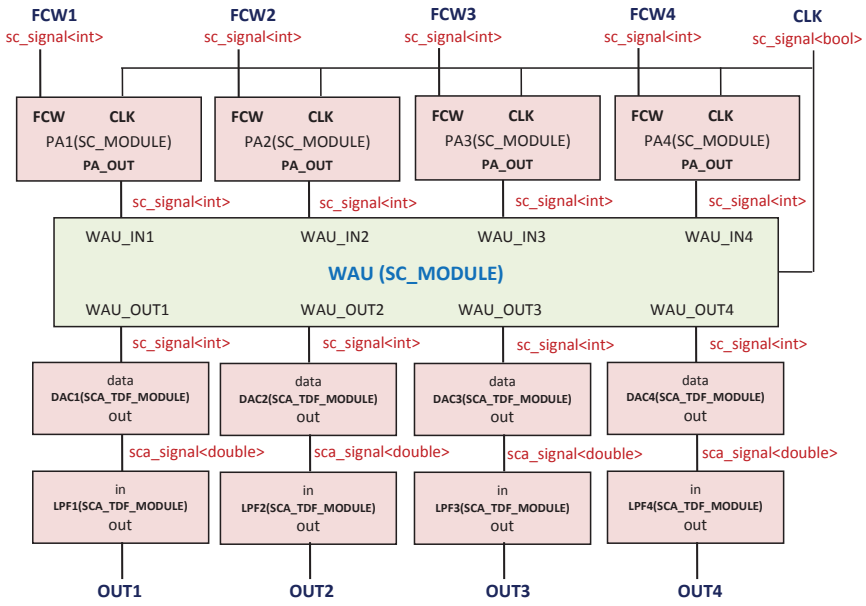

Figure 15: SystemC Top Model of PDDS-4

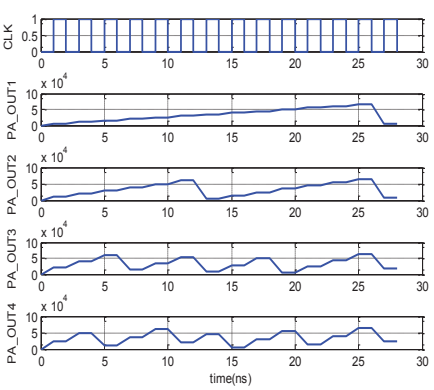

Figure 16: Phase accumulators of PDDS4-independent mode

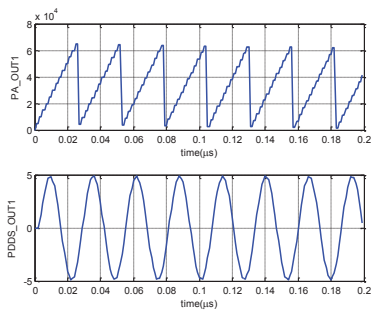

Figure 17: Phase and wave of output 1 of PDDS4-independent mode

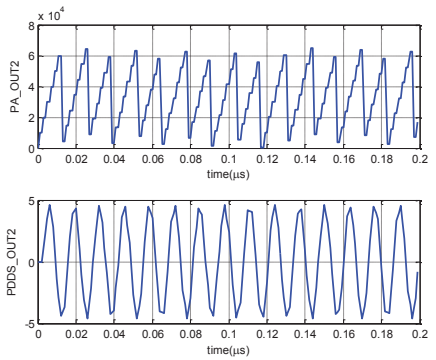

Figure 18: Phase and wave of output 2 of PDDS4-independent mode

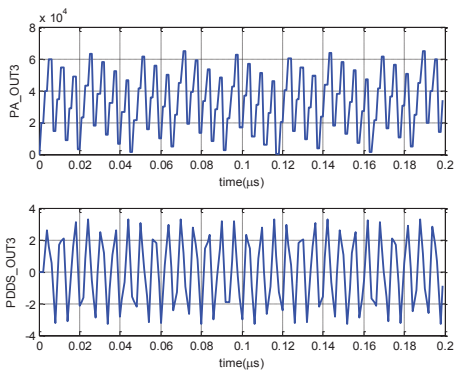

Figure 19: Phase and wave of output 3 of PDDS4-independent mode

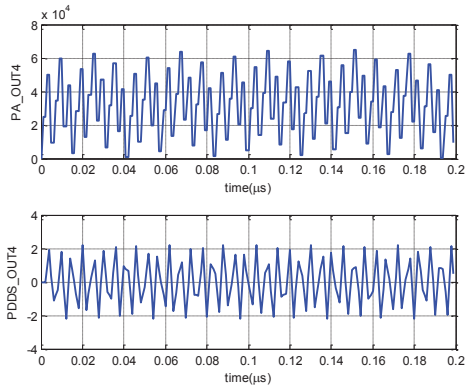

Figure 20: Phase and wave of output 4 of PDDS4-independent mode

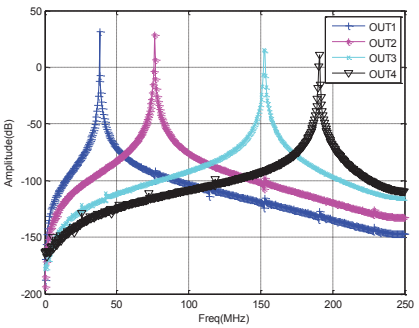

Figure 21: Spectrum of output waves of PDDS4-independent mode

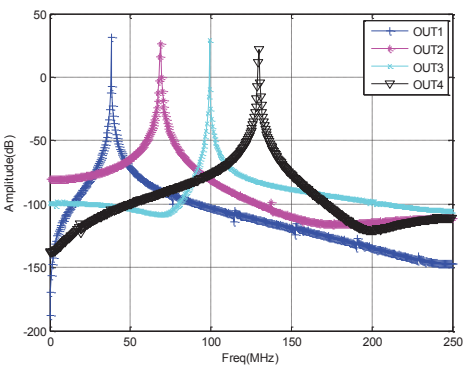

Figure 22: Spectrum of output waves of PDDS4-dependent mode

V. CONCLUSION

In this work, we have proposed a new circuit that produces a set of parallel multichannel. The importance of this circuit corresponds to its several applications in instrumentation and communications. The proposed circuit improves the reduction of time analysis and ensures the coherence of signals of the studied system. It has also shown that the SystemC/SystemC-AMS design and the simulation results have demonstrated the effectiveness and the performances of the PDDS-WAU architecture in two configuration modes: independent frequency synthesis and step frequency synthesis. As a result, the proposed circuit can be manufactured with all microelectronic integration technology on FPGA, ASIC or System on Chip.

REFERENCES

[1] M.-B. Santos, C. Sporer, N. Sanvicens, N. Pascual, A. Errachid, E. Martinez, M.-P. Marco, V. Teixeira, and J. Samiter. "Detection of pathogenic Bacteria by Electrochemical Impedance Spectroscopy: Influence of the immobilization strategies on the sensor performance", Procedia Chemistry, Volume 1, Issue 1, Proceedings of the Eurosensors XXIII conference, September 2009, Pages 1291-1294.

[2] A. Jbari, L. Bellarbi, N. Zine, C. A. Mills, J. Samitier, and A. Errachid, "Multiplexed Frequency Spectrum Analyzer Instrumentation for the Characterization of Multiple QCM-Based Biosensors", International Conference on Sensor Technologies and Applications SENSORCOMM, 2007, pp.436-440, Valencia, Espagne.

[3] X. Jinwen, C. Yang, A. Mason, and P. Zhong, "Adaptive Multi-Sensor Interface System-On-Chip", IEEE SENSORS 2006, EXCO, Daegu, Korea / October 22 25, 2006.

[4] L. Baosheng, S. Zhou, M. Stojanovic, L. Freitag, and P. Willett, "Multicarrier Communication Over Underwater Acoustic Channels With Nonuniform Doppler Shifts", IEEE Journal of Oceanic Engineering , vol.33, no.2, pp.198,209, April 2008.

[5] B. –F. Boroujeny, and R. Kempter, "Multicarrier communication techniques for spectrum sensing and communication in cognitive radios", Communications Magazine, IEEE , vol.46, no.4, pp.80,85, April 2008.

[6] J. Vankka, "Direct Digital Synthesizers: Theory, Design and Applications", Boston, London : Kluwer Academic Publishers, 2001.

[7] B.-D. Yang, L.-S. Kim, and H.-K. Yu, "A high speed direct digital frequency synthesizer using a low power pipelined parallel accumulator", in Proceedings of the IEEE International Symposium on Circuits and Systems, vol. 5, pp. 373376, May 2002.

[8] A.L. Mcewan, and S. Collins, "Efficient, ROM-less DDFS using non-linear interpolation and non-linear DAC", Analog Integrated Circuits and Signal Processing 48 (3) (2006) 231–237.

[9] T. Xinguang, Z. Zhilong, and E. Ryangzhang, "Spurious signals due to amplitude quantization in direct digital frequency synthesizers", Microelectronics Journal 41 (2010) 114–120.

[10] H. Ke-Nung, and H. Yu-Pei, "Multiple-frequency ultrasonic distance measurement using direct digital frequency synthesizers", Sensors and Actuators A 149 (2009) 42–50.

[11] J. M. Riera Salis, "Spurious Performance of Direct Digital Synthesizers Generating Modulated Signals", IEEE electrotechnical conference, Vol.1, pp. 223-226, April 1994.

[12] J. Tierney, C. M. Rader, and B. Gold, "A digital frequency synthesizer", IEEE Transactions on Audio and Electroacoustics, vol. 19, pp. 4857, 1971.

[13] O. –Q. Khalaf, I. –M. Tariqul, M. Norbahiah, and I. –M. Rashed, "ROM-Less Direct Digital Frequency Synthesizer Based on Hybrid Polynomial Approximation", The Scientific World Journal, Volume 2014, Article ID 812576.

[14] A. Ashrafi, R.Adhami, and A. Milenkovic, "A Direct Digital Frequency Synthesizer Based on the Quasi-Linear Interpolation Method", IEEE Transactions on Circuits and SystemsI: Regular papers, vol. 57, pp. 863872, no. 4, April. 2010.

[15] DR. R. K. Sharma, and G. Upadhyaya, "Memory Reduced and Fast DDS Using FPGA", International Journal of Computer Theory and Engineering, vol. 2,pp. 1793-8201, no. 4, august, 2010.

[16] P. François, L. Marie-Minerve, and E. Karsten, "SystemC AMS and cosimulation aspects", In: Bechtold, Tamara (Ed.): System-level Modeling of MEMS. Weinheim: Wiley-VCH, 2013. (Advanced Micro and Nanosystems 10), pp. 357-375.

[17] M. Zhou, and R.V. Leuken, "Systemc-AMS model of a dynamic large-scale satellitebased AIS-like network", Specification and Design Languages (FDL), 2011 Forum on, On page(s): 1 - 8, Volume: Issue: , 13-15 Sept. 2011.

[18] A. Vachoux, C. Grimm, and K. Einwich, "Analog and mixed signal modelling with SystemC-AMS, Circuits and Systems", ISCAS '03. Proceedings of the 2003 International Symposium on , vol.3, no., pp.III-914,III-917 vol.3, 25-28 May 2003.