Defect-oriented Test and Design-for-Testability Technique for Resistive Random Access Memory

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***Abstract*— Resistive Random Access Memory (ReRAM) is one of the main emerging memories that has great potential to replace existing semiconductor memories. However, it cannot be denied that ReRAM prone to have defects that lead to test escape and reliability problems. Bridge defects that occurred in the memory array might cause Undefined State Faults (USFs) during read operation. USFs cause the faulty ReRAM cell difficult to be set to the desired logical value. Hence, this paper proposed a design-for-test (DfT) technique, namely Adaptive Sensing Read Voltage (ASRV) to detect the USFs that arise during three types of bridge defects injection. For this study, a faulty ReRAM was used to be tested during simulation using Silvaco EDA simulation tools and implementation of defect-oriented test. A DfT circuitry is added in the existing sense amplifier so that this memory device can operate during the normal mode and testing mode. Based on the simulation result, the proposed DfT technique will be able to detect the USFs.**

***Index Terms*— Resistive Random Access Memory (ReRAM), bridge defect, defect-oriented test, design-for-test (DfT), Undefined State Faults (USFs).**

I. INTRODUCTION

Recently, there has been an increasing number of emerging memory technologies that are being investigated for future use. Emerging memory technologies, such as Ferrolectric RAM (FRAM), Magnetoresistive RAM (MRAM), Spin-transfer torque RAM (STTRAM), phase-change RAM (PCRAM), Resistive RAM (ReRAM) and Organic RAM (ORAM) that are used to trade the conventional memories. Among them, ReRAM offers a simple structure due to the ability to operate without the access transistors. Because of this advantage, ReRAM can provide the most dense capacity where it can reach up to 1Tbit in a square centimetre chip area of the storage density [1]. Other attractive potentials offered by this novel device are non-volatility, fast data access and low power consumption [2-4].

However, it cannot be denied that ReRAM prone to have defects such as an open, bridge or short that will decrease the quality and reliability. Undetectable fault will arise, especially when this device is still in immature research. Moreover, the size of the components used to form the memory is very tiny (less than 22nm) and closely structured. It is still in infancy stage on the perspective of quality improvement of ReRAM[5]. Studies related to faulty ReRAM that are impacted by open defects have been revealed by [5-6]. ReRAM cell also can be impacted by the bridge defect that occurred due to the imperfection fabrication process [3].

This paper presents the proposed design-for-testability (DfT) technique for testing faulty ReRAM that is impacted by the bridge defects. The difficulty and time of testing can be reduced by using DfT technique. The defect will cause the memristor cell to give the arbitrary logic value which is known as Undefined State Faults (USFs) during read operation. Simulation during implementation of the proposed DfT technique shows that the fault is successful detected.

II. LITERATURE REVIEW

This section briefly explained the background of ReRAM, including the ReRAM architecture, ReRAM cell model and ReRAM operation. Then, a defect-oriented test for the possibility of bridge defects in ReRAM was reviewed. Lastly, a review regarding the principle of DfT technique used in this research is explained.

A. ReRAM Architecture

To ease the process of simulation, this memory system is adopted in the form of functional model and electrical model. The functional model is a collection of functional blocks that are related to each other to conduct a particular function. The proposed functional model is illustrated in Figure 1 [7]. The ReRAM architecture consists of five main blocks, which are the memory cell array, row decoder, column decoder, write/read circuit and sense amplifier.

Each of the functional blocks is translated into the electrical components, i.e, transistor, memristor and resistor. This electrical model is used during the simulation. In general, ReRAM comprises (a) Complementary Metal Oxide Semiconductor (CMOS) peripheral circuit (row decoder, column decoder, write/read circuit and sense amplifier) designed to use 22nm CMOS technology and (b) non-CMOS cell known as memristor used to form the memory array.

The row and column decoders are used to ensure that the selected nanowordlines (NWLs) and nanobitlines (NBLs) receive the proper signal from the peripheral circuit. Write/read circuit is used to generate the write and read signal. The sense amplifier functions to sense the read current from the accessed memory cell and convert into a voltage. For the

structure of the memory array, this study used 2x2 arrays that consist of two NBLs crossing over two NWLs. The memristor is located at each of the cross points [7].

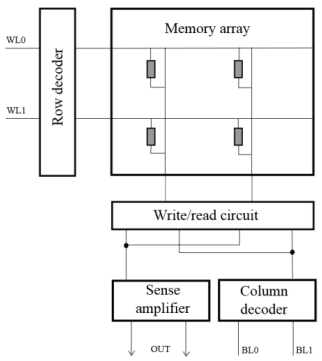

Figure 1: Functional model of ReRAM [7]

B. ReRAM Cell Model

Chua [8] claimed that the fourth fundamental passive element after the resistor, capacitor and inductor is known as the memristor. Memristor gets many attentions to be used as nonvolatile memory cells due to its special behavior. It can hold the last resistive state (memristance) when the power is switched off. Figure 2(a) shows that the memristor model is composed of two metal electrodes, Pt and separated by a thin film known as titanium oxide. The thin film, L is divided into two regions, which are (i) doped (TiO2-x) region with length w and (ii) undoped (TiO2) region with length (L-w) [9].

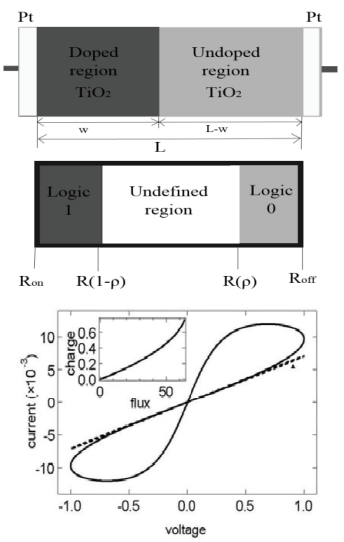

Figure 2: Memristor: (a) model (b) I-V curve

The memristance is reduced when a positive voltage is applied through the memristor because the oxygen vacancies drift to undoped region and can be reached until $M=R_{off}$. Otherwise, the memristance can be increased by applying a negative voltage. The oxygen vacancies drift towards the doped region and can be reached until $M=R_{on}$. Its special feature is that when the power supply is removed, the oxygen vacancies stop and remain in its last memristance [4]. Another special property of memristor is the existence of a pinched current-voltage (I-V) hysteresis effect as illustrated in Figure 2(b). Hence, due to its persistent and controllable abilities, the memristor is suitable to be used as the memory cell for non-volatile memory device.

Much of the available memristor model is proposed based on its physical and electrical characteristics. In this study, Biolek's memristor SPICE model is chosen as an optimal memory cell that has been implemented in this study [10]. This model is proposed by modifying the ideal Strukov's memristor model by considering the boundary effect. The model can be described as in (1) that represents the memristance as a function of the native variable q [11]:

$$R(q(t)) = R_{off} + \frac{R_{on} - R_{off}}{ae^{-4kq(t)} + 1}; \mathrm{a} = \frac{R_{ini} - R_{off}}{R_{off} - R_{ini}} \quad (1)$$

where k is a constant and R_{on} and R_{off} are the limiting values of the memristance.

C. ReRAM Operation

The ReRAM operation is performed based on the memristance mechanism described previously. Hence, the write operation can be performed by applying the appropriate voltage. Based on Figure 3, a positive voltage is supplied through the memristor for a specific time in order to make the memristence achieved the state $M=R_{on}$. Meanwhile, negative voltage is applied for a fixed duration during write 0 operation to decrease the memristance until $M=R_{off}$. Due to this mechanism, the read operation holds the concept to maintain the memristance. That is why a negative pulse followed immediately with a positive pulse with the same value and duration to create the zero net change in memristance [6].

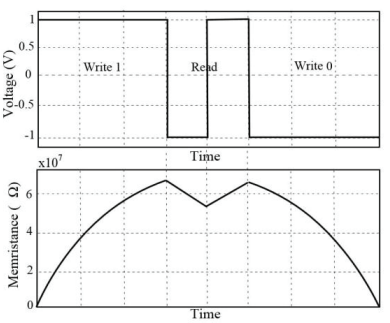

Figure 3: Changes in memristance due to voltage versus time [6]

D. Defect-oriented test

Each type of semiconductor memory devices is not spared from the suffering defects. Defects such as broken or missing metal lines and extra metal lines can lead to unintended disconnection or connection to the memory device [5]. There are two types of defects that have high occurrence possibility in the memory array, which are the open defect and bridge defect. Open defects can be defined as an unintended series resistance within a connection, while bridge defects are an unintended parallel resistance between two connections. Table 1 provides the classification of the open and bridge defect that might occur in memory array.

Table 1
Defect classification in memory array

Classification	Locations	Notation
Open	Within cells	OC
	At nanowire bit lines (NBLs)	OB
	At nanowire word lines (NWLs)	OW
Bridge	Between NBLs	BB
	Between NWLs	BW
	Between NBLs and NWLs	BBW

A test is needed to identify the defects. Hence, this work implements the use of defect-oriented test in order to detect defects that affect any measurable memory behavior such as the output voltage. In this test, the defects are modeled as a spot of extra metal or missing metal in the layout of the memory circuit. Then, the appropriate test algorithm is applied and observed the memory behavior.

Only bridge defect will be discussed in this paper. Since this study focuses on the electrical level, so the defect is modeled using a resistor. Figure 4 shows the example of the possible location of the bridge defect that occurs in the memory array.

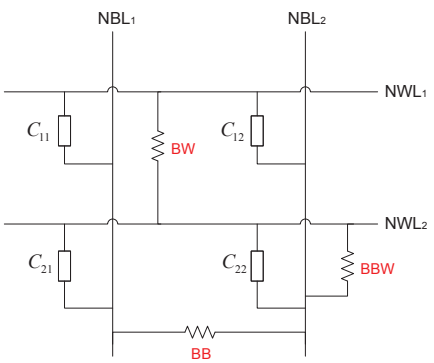

Figure 4: Possible locations of bridge defect

E. Design-for-Testing

Defects that occur in the memory array can cause the memory cell to enter the undefined state. Unfortunately, quality test that use a sequence of write and read operation such as march tests cannot guarantee the detection of this faults. DfT is a testing technique that implements a specialized circuit. Slight modification on original circuit is needed for this technique. The DfT circuitry inserted in the circuit is often idle during normal operation and used during test mode.

There is still immature research on DfT technique for this ReRAM. Zaidi [13] proposed two DfT technique to detect fault caused by the open defect. The techniques are Short Write Time (SWT) and Low Write Voltage (LWV). The SWT technique is proposed by reducing the write access time and maintainung the normal supply voltage. Meanwhile, the LWV technique maintained the access time and reduced the write level. Both techniques are developed based on two parameters, namely the durations of access time and the value of the applied voltage. These parameters are used to stress the faulty cell in order to shift the cell state from an undefined state to an incorrect state.

As mentioned before, the bridge defect may cause the memory cell to enter an undefined state and cause faults, namely the Undefined State Faults (USFs). USFs is difficult to be detected because the faults cause a random logic value to be read from the faulty ReRAM cells[5]. For example, the defective ReRAM might give a reading of 1 or 0 during read 1 operation. However, there is still no DfT technique proposed by researchers to detect this fault.

Therefore, a special DfT technique is required. In order for USFs detection, a new DfT technique is proposed in this paper. This new DfT technique is referred as the Adaptive Sensing Read Voltage (ASRV). ASRV technique is created based on how the sense amplifier functions. Sense amplifier produces output voltage during read operation. A DfT circuitry is required as an adjunct circuitry in the sense amplifier.

Sense amplifier as shown in Figure 5 is based on the hybrid current-voltage mode sense amplifier, where it has two inputs. The first input receives the current from memory array and the second input as an input for reference voltage (V_{ref}). The output voltage produced by this hybrid sense amplifier is suitable for high-performance memory [12]. The sense amplifier senses the reading current from the accessed memory cell and is converted into a voltage. If the faulty cell is already in an undefined state, applying the reduced read voltage during read operation will push the cell to shift from undefined state to defined state (high or low state).

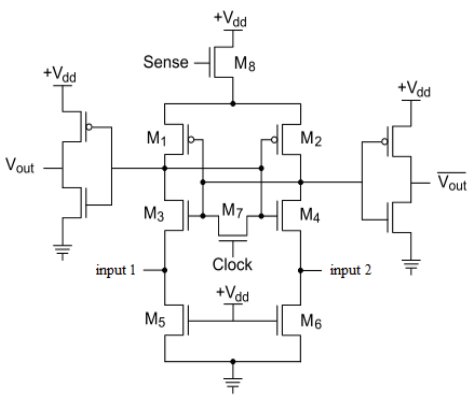

Figure 5: Hybrid current-voltage sense amplifier

III. Research Methodology

The research execution is based on simulation and physical modelling of ReRAM cell performance. The software package used for this research is known as SILVACO Electronic Design Automation (EDA). Since the bridge defects have high probability occurred between two adjacent ReRAM cells, the 2x2 ReRAM cell array is adequate to be used in the simulation. There are two main steps involved in this research, which are the defect-oriented test and DfT technique.

A. Defect-oriented test

After conducting some background studies about ReRAM, defect-oriented test and DfT, the bridge defect is injected in the memory array. Three types of bridge defect are injected into the memory array, which are the (i) bridge between NBLs (BB), (ii) bridge between NWLs (BW) and (iii) bridge between NBLs and NWLs (BBW). Firstly, the considered bridge defects are modeled electrically by using an additional resistor as illustrated in Figure 4. Then, the simulation is carried out based on the type of the defect. The value of the resistor modeled as the bridge defect is varied between 0Ω till 1kΩ. During simulation, the test algorithm is applied through the faulty model. The test algorithm is shown in Table 2. The output voltage is measured and recorded. All of the data are analyzed to observe the memory behavior.

Table 2
Test Algorithm

1.	Write 1 to aggressor cell and victim cell (Initialize memory cell to 1).
2.	Write 0 to aggressor cell
3.	Read 0 from aggressor cell.
4.	Read 1 from victim cell.

B. DfT Technique.

After the completion of the defect-oriented test for all of the bridge defects, the new DfT technique is proposed and developed based on the principle explained previously. Based on the defect-free simulation, voltage produced by the memristor cell during read operation is 0.15V. This voltage is adopted as a reference voltage during the implementation of ASRV technique.

During the simulation for DfT test mode, the V_{ref} is reduced by 0.01V until the achievement of the optimum voltage that is able to shift the state. Hence, the optimum V_{ref} supplied to second input of the sense amplifier is 0.11V. The next step is to obtain the value for each resistor. The circuit as illustrated in Figure 6 is based on the voltage divider concept as in Eq. 2:

$$V_{ASRV} = \frac{V_{ref} \times R_2}{R_1 + R_2} \quad (2)$$

where V_{ASRV} is 0.11V, and V_{ref} is 0.15V. To get the value for resistors, R2 is fixed, which is 100Ω. By using Equation 2, the value for R1 is 50Ω. The DfT circuitry in Figure 6 consists of two transistors (one nmos transistor and one pmos transistor) and two resistors. Test algorithm can be applied in faulty ReRAM in order to detect the bridge effects that occur in the memristor cell array.

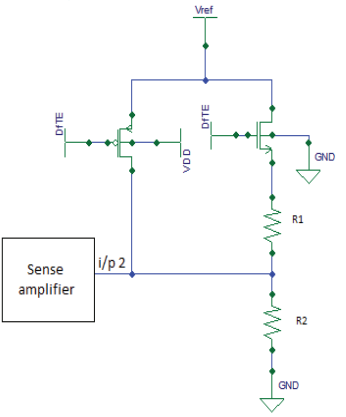

Figure 6: DfT Circuitry

Then, the same test algorithm is applied. However, there is a little change in the algorithm at step 4. The DfT technique is enabled during step 4. The same observation is done to the output voltage.

IV. Results And Discussion

This section presents the simulation results and analysis for the implementation of the DfT technique during testing. There are three types of bridge defects considered in this study, which are the bridge between NBLs (R_{BB}), bridge between NWLs (R_{BW}) and bridge between NBLs and NWLs (R_{BBW}). Each of the simulations is carried with the sequence of memory operation based on the proposed test algorithm.

A. Bridge between NBLs (RBB)

The first sub-section considered bridge defect occurred between nanobitlines (NBLs). This bridge defect, R_{BB} is modeled electrically using the resistor between NBL_1 and NBL_2. The value for the resistor is varied between the range of 0Ω and 1kΩ. The results include the value of output voltage before and after implementation of DfT technique. The voltage is measured during the read operation. Only resistive bridge value caused the USFs is considered in this paper. Table 3 gives the results of the simulation for this bridge defect, RBB for sequence $S = w1(C_{11}), w1(C_{12}), w0(C_{11}), r0(C_{11}), r1(C_{12})$. The results only covered the output voltage produced by the victim cell.

In this sequence, C_{11} is the aggressor cell, and C_{12} is the victim cell. Before the implementation of the DfT, the victim cell gives an undefined value when $36\Omega \leq R_{BB} \leq 360\Omega$. The results of the analysis of this simulation is done by illustrating all the data in terms of the graph as shown in Fig 7. During the bridge injection (before implementation of DfT technique), the output voltage is in an undefined state. The sense amplifier might produce incorrect logic state. After the implementation of this technique, the output voltage managed to shift down to defined state, which is the low state.

Table 3
Results for R_{BB} before and after implementation of DfT

$R_{BB}(\Omega)$	Output voltage before DfT (V)	Output voltage after DfT (V)
36	0.3273	0.0549
40	0.3417	0.0621
50	0.3718	0.0776
60	0.3959	0.0962
70	0.4222	0.1123
80	0.4434	0.1271
90	0.4607	0.1407
100	0.4759	0.1529
200	0.5634	0.2296
300	0.602	0.2657
350	0.6141	0.2774
360	0.6162	0.2816
370	0.6182	0.2835

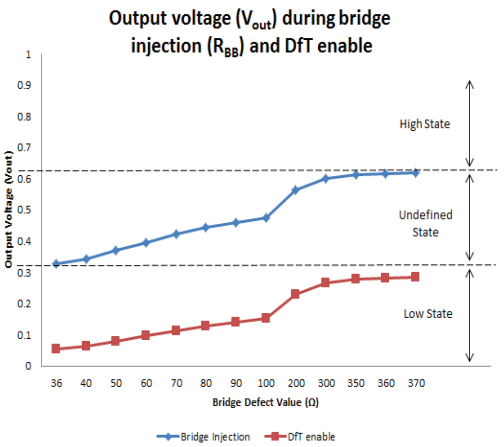

Figure 7: Graph comparison of output voltage (V_{out}) during bridge injection (R_{BB}) and DfT enable

B. Bridge between NWLs (RBW)

This sub-section presents the simulation results and analysis for bridge defect, R_{BW}. This resistive bridge defect is located within two nanowordlines, NWLs which are the NWL_1 and NWL_2. The same simulation setup for R_{BB} is applied to simulate this faulty ReRAM with R_{BW} injection. The results obtained from the simulation are presented in Table 4. It gives the output voltage during read 1 operation at the victim's cell before and after performing the DfT technique. The sequence used in this simulation was $S = w1(C_{12}), w1(C_{22}), w0(C_{12}), r0(C_{12}), r1(C_{22})$. C_{12} is acted as the aggressor cell while C_{22} is the victim cell. It is apparent in this table that the victim cell before performing the DfT technique gives the output voltage in the region of undefined state when $0\Omega \leq R_{BW} \leq 50\Omega$.

Figure 8 compares the results obtained from the simulation. The result shows that the faulty ReRAM gives the undefined state during normal mode. In order to detect this defect, the DfT technique is enabled during testing. This implementation of DfT technique is managed to shift down the output voltage for achieving the low state. It shows that this technique is able to detect this fault because it returns the wrong value of 0 (low state).

Table 4
Results for R_{BW} before and after implementation of DfT

$R_{BW}(\Omega)$	Output voltage before DfT (V)	Output voltage after DfT (V)
0	0.4779	0.1039
10	0.5236	0.1382
20	0.5577	0.1677
30	0.5858	0.1944
40	0.6089	0.2171
50	0.6074	0.2368

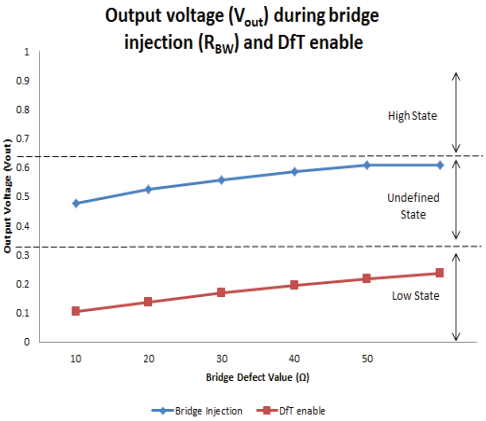

Figure 8 Graph comparison of output voltage (V_{out}) during bridge injection (R_{BW}) and DfT enable

C. Bridge between NBLs and NWLs (R_{BBW})

The last type of bridge defect considered in this study is a bridge between NBLs and NWLs (R_{BBW}). The location of R_{BBW} in this simulation is located within NBL_2 and NWL_1. The same simulation setup similar to previous simulation is also applied for this R_{BBW}. Table 5 provides the simulation data on R_{BBW} before and after the DfT technique execution. The results are quite different from R_{BB} and R_{BW}. The sequence employed for this simulation is $S = w1(C_{12}), w1(C_{22}), w0(C_{12}), r0(C_{12}), r1(C_{22})$. Due to the location of the bridge defect, there is no aggressor cell in this simulation. However, the adjacent cell needs to be considered. In this situation, C_{12} is the victim cell, and C_{22} is the adjacent cell. The output voltages of both cells are measured during both conditions (before and after DfT). The victim cell gives the undefined states when $140\Omega \leq R_{BBW} \leq 210\Omega$.

Table 5
Results for R_{BBW} before and after implementation of DfT

R_{BBW} (Ω)	Victim cell		Adjacent cell	
	Output voltage before DfT (V)	Output voltage after DfT (V)	Output voltage before DfT (V)	Output voltage after DfT (V)
140	0.611	0.2899	0.8154	0.4017
150	0.5654	0.2443	0.8167	0.4022
160	0.5225	0.2044	0.8183	0.4056
170	0.4823	0.1681	0.8201	0.4086
180	0.4485	0.1359	0.8222	0.4182
190	0.41	0.1081	0.8244	0.4178
200	0.3778	0.0845	0.8266	0.4216
210	0.3479	0.0655	0.8288	0.4302

To simplify the analysis of this result, the data are illustrated using two graphs. Each of the graph compared the voltages during the bridge injection (normal mode) and during the implementation of the DfT technique. Figure 9 shows the results for the victim cell, C_{12}. During the normal mode, the voltages are identified in an undefined state. The cell might give a reading value between logic 1 or logic 0. It is difficult to be detected. After the implementation of this DfT technique, the output voltage managed to be shifted down to low state (logic 0) and at the same time, it is able to ensure that the ReRAM is faulty.

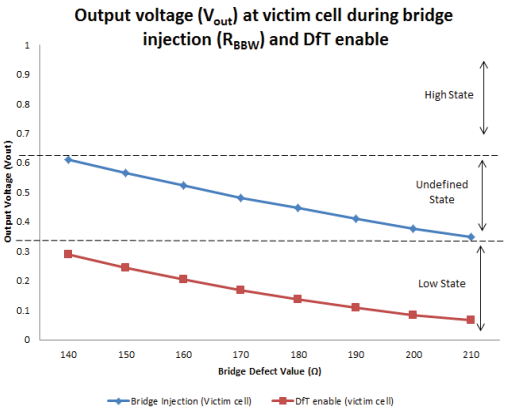

Figure 9: Graph comparison of output voltage (V_{out}) at victim cell during bridge injection (R_{BBW}) and DfT enable

Unfortunately, the adjacent cell, C_{22} is impacted during the DfT implementation. Figure 10 shows that the voltage during normal mode is in high state, which is the right value for read 1 operation. When DfT circuit is enabled, the graph is shifted down to undefined state. It shows that this technique might kill the healthy cell.

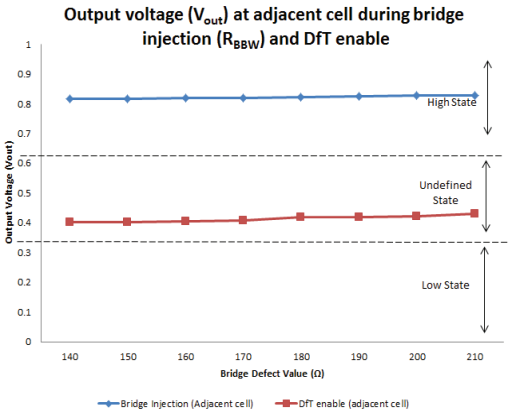

Figure 10: Graph comparison of output voltage (V_{out}) at adjacent cell during bridge injection (R_{BBW}) and DfT enable

V. Conclusion

This paper set out to propose the DfT technique that is able to detect USFs that occur in the memory array caused by the bridge defects. The results confirmed that the ASRV technique managed to detect USFs. This technique can be applied for off-line and on-line testing at the manufacturing plant in order to increase the product quality and reliability of the system. However, more research is needed to avoid overkilling the healthy cell as happened in testing for R_{BBW}.

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References

[1] J. Callaham, "Newly revealed Resistive RAM (RRAM) tech puts 1 TB of storage on one chip," 2013. [Online]. Available: http://www.neowin.net/news/newly-revealed-resistive-ram-rram-tech-puts-1-tb-of-storage-on-one-chip.

[2] K. K. Likharev, "Hybrid CMOS/Nanoelectronic Circuits: Opportunities and Challenges," *J. Nanoelectron. Optoelectron.*, vol. 3, no. 3, pp. 203–230, Dec. 2008.

[3] N. Z. Haron and S. Hamdioui, "On Defect Oriented Testing for Hybrid CMOS/Memristor Memory," *2011 Asian Test Symp.*, pp. 353–358, Nov. 2011.

[4] Y. Ho, G. M. Huang, and P. Li, "Nonvolatile Memristor Memory : Device Characteristics and Design Implications," *IEEE/ACM Int. Conf. Comput. Aided Des. Dig. Tech. Pap.*, pp. 485–490, 2009.

[5] S. Hamdioui, M. Taouil, and N. Z. Haron, "Testing Open Defects in Memristor-Based Memories," *IEEE Trans. Comput.*, pp. 1–14, 2013.

[6] S. Kannan, J. Rajendran, R. Karri, and O. Sinanoglu, "Sneak-path Testing of Memristor-based Memories," *2013 26th Int. Conf. VLSI Des. 2013 12th Int. Conf. Embed. Syst.*, pp. 386–391, Jan. 2013.

[7] N. Arshad, N. Z. Haron, Z. Zakaria and N. Soin, "Development of Resistive RAM Simulation Model for Defect Analysis and Testing," *Adv. Sci. Lett.*, vol. 20, no. 10-12, p. 1745-1750, 2014.

[8] L. Chua, "Memristor - The Missing Circuit Element," *IEEE Trans. Circuit Theory*, vol. CT-18, no. 5, pp. 507–519, 1971.

[9] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found.," *Nature*, vol. 453, no. 7191, pp. 80–3, May 2008.

[10] N. Z. Haron, N. Arshad, and F. Salehuddin, "Performance Analysis of Memristor Models for RRAM Cell Array Design using SILVACO EDA," *J. Teknologi*, vol. 3, pp. 1–6, 2014.

[11] D. Biolek, M. D. I. Ventra, and Y. V Pershin, "Reliable SPICE Simulations of Memristors , Memcapacitors and Meminductors," *Radioengineering*, vol. 22, no. 4, pp. 945–968, 2013.

[12] C.-C. Chung, H. Lin, and Y.-T. Lin, "A Multilevel Read and Verifying Scheme for Bi-NAND Flash Memories," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1180–1188, May 2007.

[13] N. Zaidi, "Testability and Fault Tolerance for Emerging Nanoelectronic Memories," TU Delft, 2012.