A New Symmetric/Asymmetric Multilevel Inverter Based on Cascaded Connection of Sub-Multilevel Units Aiming less Switching Components and Total Blocked Voltage

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***Abstract*— In this paper, a new multilevel inverter is designed to improve the power and voltage quality, which contains a lesser number of switches in the specified voltage levels. The proposed inverter includes power electronic devices such as switches and diode, and DC inputs. In the proposed structure the desired output voltage can be produced by considering a series connection of a novel sub-multilevel module. This structure can be designed in both the symmetric and asymmetric topologies. The proposed structure has superior condition in terms of semiconductor switches and drivers count as well as switching loss. Additionally, the Total Blocked Voltage (TBV) of the proposed converter is compared with the conventional and the novel converters. This topology is studied by symmetric as well as asymmetric topologies through simulations in Matlab/Simulink environment as well as experiments by a laboratory prototype.**

***Index Terms*— Multilevel Inverter, Number of Switch, Number of Gate Driver; Power Loss.**

I. INTRODUCTION

Multilevel inverters (MLIs) are an appropriate choice for converting DC-AC voltages, especially in moderate and high power range to improve power quality. These inverters have several advantages over a typical two-level inverter, as they have low Total Blocking Voltage (TBV), low electromagnetic interference, high output power, high efficiency and low losses. With these features, they have been employed in many industrial applications, such as locomotives, navies, reactive power compensators, and power conversion in renewable energy systems [1].

Conventional multilevel inverters consist of NPCs, flynig capacitors (FCs) and cascaded H-bridge (CHB) [2-4]. Clamp diode inverters face challenges, such as DC link voltage balance and a large number of power semiconductor devices at high output levels. More switching devices have the ability to reduce the reliability of the converter [5, 6]. Among the disadvantages of flynig capacitor multilevel inverters, the large number of flynig capacitors and the complex control scheme to maintain the voltage equilibrium of each capacitor at the desired value as well as the need for multiple voltage sensors can be mentioned. These disadvantages increase the switching losses, volume and cost [7, 8]. The CHB multilevel inverters consist of several H-bridges, in which each H-bridge comprises four switches and a DC source that can add two levels to the output voltage levels. Modularity, easy control and high reliability are the advantages of the CHB inverter, while the main disadvantages of this type of multilevel inverters are the large number of DC sources and switching devices at higher levels [9, 10].

Considering the above cases, the main disadvantages of conventional multilevel inverters are the large number of switches and diodes at high output levels. It causes to increase system complexity and cost. Also, it can reduce system reliability and efficiency. Therefore, in addition to achieve high quality output waveform, the count of switches and drivers which includes bulk portion of the cost, should be minimized. For this reason, researchers have always come up with structures to reduce the number of devices in multilevel inverters. New proposed structures, which are designed to reduce switching devices are divided into two main categories: topological changes and asymmetrical resources.

This paper presents an improved structure of voltage source multilevel inverters with the aim of reducing power electronic devices, which has fewer power switches than the classical structures and the recent researches. This switch difference is observed more clearly at higher levels and makes the proposed structure more tangible. This structure uses an improved basic cell that generates three voltage levels. The proposed basic cell is capable of producing one voltage level more than structure of [11] with only one more DC source. This approach reveals a significant decrease in the required number of power switches compared to classical topologies and similar researches. The proposed structure can be employed as the converter of the medium voltage and power drive systems. Also, it may be applied in photovoltaic power systems, which several separated DC sources are available.

The rest of this paper is organized as follows. In the next section, general structure of the proposed topology is presented. Also, operational principles of the proposed basic cell and its extended structure are described. The mathematical equations deal with the output voltage, number of the switches, gate drivers, and total blocking voltage are also given in this section. The calculations of power losses and comparison between loss of the proposed and some other similar structures are carried out in Section 3. A comprehensive comparison is made between the proposed topology and similar studies in Section 4. Simulation and experimental results are given in Section 5. Finally, Section 6 concludes the paper.

I. TOPOLOGY OF THE PROPOSED MULTILEVEL INVERTER

In this section, the proposed structure is introduced. Next, its operation principles are explained in a single phase nine-level inverter by related equations.

A. Basic Cell

In this paper, the proposed multilevel inverter is derived from the extension of a basic cell. Figure 1 shows the proposed basic cell. This cell includes three DC voltage sources, four power electronic switches. It can produce three positive voltage levels. The switch can be implemented by a transistor (e.g. MOSFET, IGBT), which contains an antiparallel diode. The output voltages of the proposed cell for all possible states are given in Table 1.

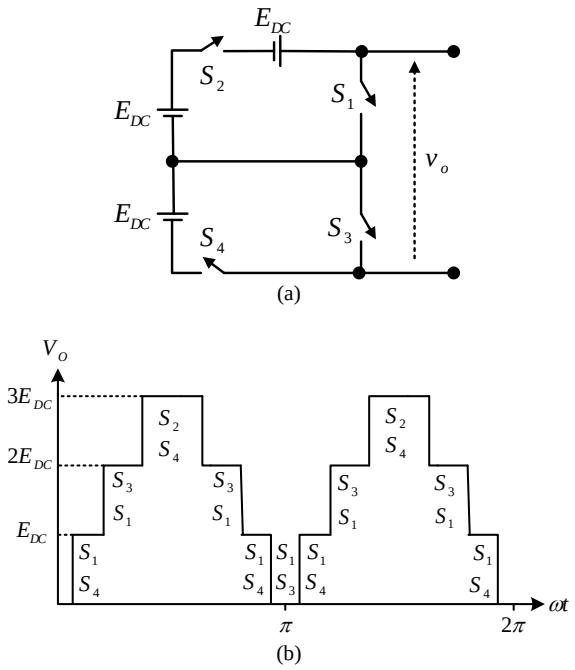


Figure 1: (a) Proposed basic cell, and (b) output voltage waveform of proposed cell

Table 1
Output Voltage of the Proposed Basic Cell for All States

Mode	S_1	S_2	S_3	S_4	V_o
1	1	0	1	0	0
2	1	0	0	1	E_{DC}
3	0	1	1	0	$2E_{DC}$
6	0	1	0	1	$3E_{DC}$

The proposed basic structure is constructed from the basic cell and an H-Bridge. Basic cell produces positive voltage levels. The task of the H-Bridge is voltage polarity change as well as zero voltage level production. The proposed structure for nine-level voltage is shown in Figure 2. This structure contains eight switches and four DC sources to produce nine-level voltage. The proposed structure has less switch count in comparison with the similar ones.

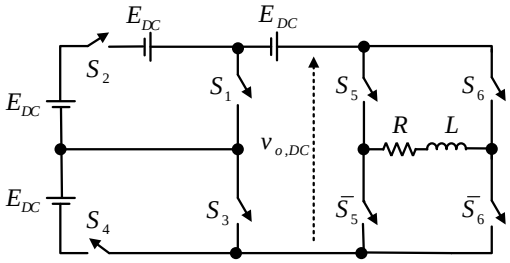


Figure 2: Basic structure of the nine-level proposed inverter

B. Extended Structure

Extended structure of the proposed multilevel inverter is shown in Figure 3. The structure has the capability to produce all voltage levels for low load power factors. The voltage across the H-bridge ($v_{o,dc}$) is resulted from the sum of all output voltages of cells and V_d , shown in (1).

$$v_o = v_{o1} + v_{o2} + ... + v_{on} + V_d \ , \ n \geq 1 \tag{1}$$

where: n = Number of basic cells used in the proposed multilevel inverter structure
$v_{o,dc}$ = Positive DC value of this voltage or its inverse can be applied to the load by the H-bridge module

It is worth noting that the zero voltage level can also be generated by H-bridge switches. The extended structure is analyzed for symmetric and asymmetric topologies in the following sub-section.

i. Symmetric Topology

For the equal DC sources mode, the DC sources values are considered as $E_{1,n} = E_{2,n} = E_{3,n} = V_d = V_{DC}$, $n \geq 1$. In such situation, output voltage peak and possible level count can be determined by (2) and (3), respectively as:

$$V_{o,max}^{sym} = (3n+1).V_{DC} \tag{2}$$

$$N_{level}^{sym} = 6n+3 \tag{3}$$

where: n = Number of basic cells

In the proposed structure for the state of symmetric sources, required switches count, drivers count, and TBV can be determined as:

$$N_{switch}^{sym} = 4n+4 \tag{4}$$

$$N_{driver}^{sym} = 4n+4 \tag{5}$$

$$TBV^{sym} = (18n+4).V_{DC} \tag{6}$$

Maximum Blocking Voltage (MBV) by switches is an important parameter in the converters especially in cost calculations. If blocked voltage by switches is low, the inverter cost will be reduced. On the other hand, MBV is one of main parameters in the switch selection. Therefore, for calculating the MBV, blocked voltage of each switch should be considered. According to Figure 3, blocked voltage of the switches is yielded as:

$$V_{S_{1n}} = V_{S_{2n}} = E_{1,n} + E_{2,n} \ , \ n \geq 1 \tag{7}$$

$$V_{S_{4n}} = V_{S_{3n}} = E_{3,n} \ , \ n \geq 1 \tag{8}$$

$$V_{S_5} = V_{\bar{S}_5} = V_{S_6} = V_{\bar{S}_6} = v_{o1} + v_{o2} + ... + v_{on} + V_d \ , n \geq 1 \tag{9}$$

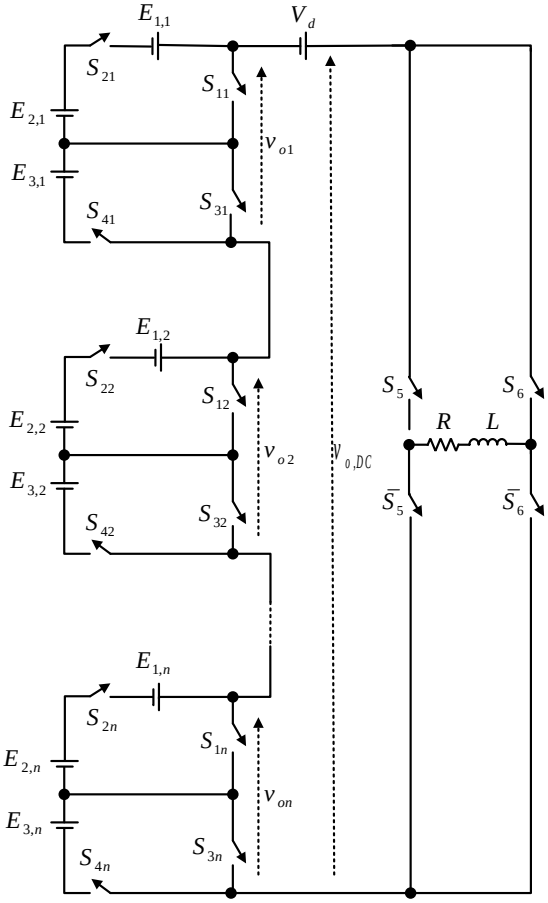


Figure 3: Extension of the proposed structure

ii. *Asymmetric Topology*

For unequal DC sources mode, different strategies may be developed. In this paper, the voltage of the first cell is assumed to be V_{DC} and the other cells $4V_{DC}$ ($E_{1,1} = E_{2,1} = E_{3,1} = V_d = V_{DC}$ & $E_{1,n} = E_{2,n} = E_{3,n} = 4V_{DC}$, $n \geq 2$). In this condition, the output voltage peak and the possible level count can be determined by (10) and (11), respectively as:

$$V_{o,max}^{asym} = (12n - 8).V_{DC} \ , \ n \geq 2 \tag{10}$$

$$N_{level}^{asym} = 24n - 15 \ , \ n \geq 2 \tag{11}$$

where: n = Number of basic cells

In the proposed structure for asymmetric topology, the required switches count, drivers count, and TBV can be calculated as:

$$N_{switch}^{asym} = 5N + 9 \tag{12}$$

$$N_{driver}^{asym} = 5N + 9 \tag{13}$$

$$TBV^{asym} = (72N + 22).V_{DC} \tag{14}$$

where: N = Number of the basic cells, which their DC voltage sources are $4V_{DC}$.

Although the produced voltage levels in asymmetric condition are more than the symmetric state, the voltage stress and the switches loss are higher. In this condition, the generation of the different values of DC voltage is more complex than the symmetric topology.

II. POWER LOSS CALCULATIONS

The loss of a power electronic converter is the summation of all its semiconductor devices power losses. A semiconductor device loss can be studied in three conditions: 1) when the device blocks current (OFF mode) by assuming that the leakage current is negligible [12], the loss can be ignored. 2) when the device conducts (ON mode). 3) when the device is in switching mode (transient from ON to OFF mode or vice versa). Therefore, the proposed inverter losses include the conduction and the switching loss.

A. Conduction Loss

Power transistors, which are utilized in the proposed topology, can conduct in two directions and block in one direction. The conduction loss of the conventional transistor and diode can be given as [13], according (14) and (15).

$$\rho_{c,Transistor}(t) = \left(V_T + R_T i^{\beta}(t)\right) i(t) \tag{14}$$

$$\rho_{c,Diode}(t) = \left(V_D + R_D i(t)\right) i(t) \tag{15}$$

where: $\rho_{c,T}(t)$ = Conduction loss of transistor
$\rho_{c,D}(t)$ = Conduction loss of diode
V_T = Voltage drop on transistor in ON mode
V_D = Voltage drop on diode in ON mode
R_T = Resistance of transistor in ON mode
R_D = Resistance of diode in ON mode
β = Constant corresponds to transistor characters

As mentioned in the previous section, the conduction of the switches depends on the instantaneous load current $i_L(t)$. It also depends on the output voltage level and the load current polarity, the transistor or the parallel diode. At each moment, the number of conductive transistors and diodes are $N_D(t)$ and $N_T(t)$ respectively. By using (14) and (15), the average conduction loss can be derived as:

$$\rho_{c,avg} = \frac{1}{\pi}\int_0^{\pi}\Big[\big(N_T(t)V_T + N_D(t)V_D\big)i_L(t) + \Big(N_T(t)R_T i_L^{\beta+1}(t)\Big) + \Big(N_D(t)i_L^2(t)\Big)\Big]d(\omega t) \tag{16}$$

where: $E_{on,j}$ = Turn on energy loss

t_{on} = Required time for the j-th switch to be turned on

The switch current just after the switch is turned on, which is shown by I and $V_{o,j}$ is the blocking voltage of the j-th switch at off state. Similarly, the energy loss of the j-th switch during turning off can be calculated as:

$$E_{off,j} = \int_0^{t_{off}} v(t)i(t)dt = \int_0^{t_{off}} \left[\left(V_{o,j} \frac{t}{t_{off}} \right) \left(-\frac{I'}{t_{off}} (t - t_{on}) \right) \right] dt = \frac{1}{6} V_{o,j} I t_{off} \quad (17)$$

where: t_{off} = Required time for the j-th switch to be turned off

I' = Switch current just before it starts to be turned off

The switching loss is the function of the switch state changes and the modulation scheme. During a time period of one second, the state of the j-th switch is changed f_j times, where f_j is the switching frequency. Therefore, the total switching losses of the inverter can be evaluated as:

$$\rho_s = \sum_{j=1}^{M} \left[\frac{1}{6} V_{o,j} I (t_{on} + t_{off}) f_j \right] \quad (18)$$

Using (16) and (18), the total power losses can be calculated as:

$$\rho_{losses} = \rho_{c,avg} + \rho_s \quad (19)$$

After that, by employing (20), the efficiency of the inverter is equal to (21).

$$P_{out} = V \times I \times \cos\theta \quad (20)$$

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + \rho_{losses}} \quad (21)$$

The power losses of the proposed structure is compared with a number of symmetric multilevel topologies including the CHB and the recently introduced topologies.

The loss of the proposed basic structure is calculated by simulation. The calculated power losses caused by every switch and diode are illustrated in Figure 5. Meanwhile, the efficiency of the proposed inverter and the recently introduced ones plus the symmetric CHB in the same conditions are shown in this figure. All of these simulations were carried out for nine-level output voltage using symmetric sources and SPWM scheme. In addition, the switching frequency is 450 Hz and the switches are loaded by 80% of their rating i.e. 480 volts and 40 amps for the output power of the 8673 W and with pure resistive load. For the loss calculation, the data of IKFW60N60DH3E (600 V, 50 A) IGBT was used. As can be seen in Figure 5, the efficiency of the proposed topology is the highest.

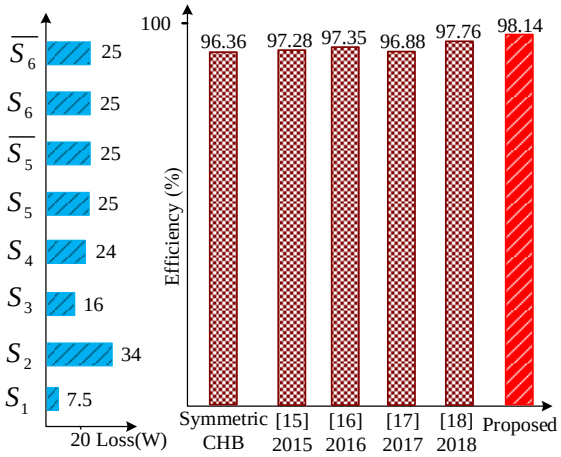


Figure 5: Loss and efficiency of the structures

III. COMPARISONS WITH OTHER STRUCTURES

In this section, the proposed structure is compared with the other ones for symmetric voltage sources in the same voltage level. Although there are several strategies for asymmetric condition, comparisons for this condition were conducted based on one of them. Some of the most important parameters of the multilevel inverters are the switch, gate driver count and TBV. Other supplementary components like the heatsinks and snubbers directly increase the cost. The total Blocked Voltage (TBV) is defined as the sum of the Maximum Blocking Voltage (MBV) of each switch. It can be calculated as:

$$TBV = \sum_{Switch=1}^{M} MBV \quad (22)$$

Multilevel inverter costs deal directly with the parameters. Higher number of switches, gate drivers and TBV will result in a higher cost of the inverter. Researchers endeavor to propose a structure with low total cost to be applicable in industrial applications. Inverter size deals with device counts: Lower device number causes lower size.

The proposed topology in comparison with the recently introduced topologies has a lower number of switches for the same number of output voltage levels. Figure 6 presents a comparison in the switch count between the structure and other multi-level symmetrical converters for different voltage level. The slope of each curve in Figure 6 deals with the cost and the size of the relative structure. CHB structure is a set of several H-bridge units, which include a DC source and four switches. In CHB structure, H-bridge (adding two levels to output voltage) is increased by adding four switches to the structure. In other words, the slope of the switch count-voltage level curve is two., in all other structures, the slope is approximately one. It means that the bulk number of the structures for increasing two levels, two switches are added to the structure. In the proposed structure, this slope is 0.75. In other words, to increase it to six levels, only four switches are added to our structure. It is clear that the proposed structure shows a remarkable improvement in the switch count reduction, especially in high voltage levels. Since the count of the drivers and other supplementary components are approximately proportionate to switch count, their number is reduced by decreasing the switch count.

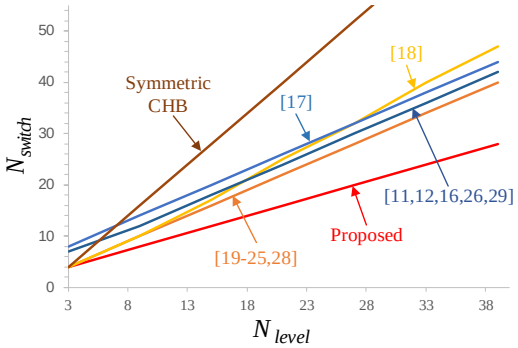


Figure 6: Comparison of switch count in different multi-level inverter structures

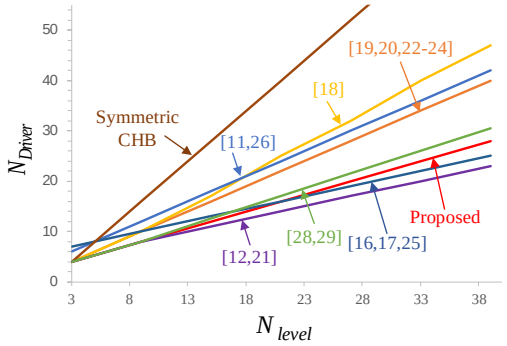


Figure 7: Comparison of driver in different multi-level inverter structures

Figure 7 shows variation of the driver count of the investigated structures in term of the level number. As shown, the use bidirectional switches structures of [12] and [21] are partially better than the proposed structure with respect to the driver count. On the contrary, the proposed structure has less switch count and TBV in comparison with the mentioned structures for the same voltage level.

TBV values of the proposed structure and other investigated structures are given in Table 2. These values are for the 15-level output voltage and 33-level output voltage in the symmetric and asymmetric topologies, respectively. In addition to TBV, the switch and driver counts were compared. In Table 2, some of the structures are discussed only in the symmetric state. It is because that they cannot operate in the asymmetric topology. TBV of the proposed structure is only more than the CHB structure. In other words, excluding the symmetric and asymmetric CHB structures, the proposed structure has the least TBV among the investigated structures. This upper hand of the CHB structures is due to the high count of the switches and the drivers, which is a drawback from the other point of views. According to Figure 6 and 7, represented in Table 2, the proposed structure has the least count of switches and drivers for both symmetric and asymmetric topologies for all investigated structure. These comparisons were carried out for the same voltage level.

IV. SIMULATION AND IMPLEMENTATION RESULTS

The results of the simulation and implementation for the proposed multilevel inverter are presented in this section. There are many different modulation strategies for multilevel inverters, which can be generally classified as fundamental frequency switching and high frequency switching strategies. Among high frequency modulation strategies, SPWM and space vector techniques are the most famous ones while the staircase modulation, active harmonic elimination, and Selective Harmonic Elimination (SHE) can be mentioned for the fundamental frequency switching strategies. The proposed topology is compatible with all of these methods.

Table 2
Comparative Parameters of Different Multilevel Inverters with Symmetric 15-Level and Asymmetric 33-Level Outputs

		N_{level}	N_{Switch}	N_{diode}	N_{source}	*TBV*	N_{Driver}
CHB	Symmetric	*15*	*28*	*0*	*7*	*28*	*28*
	Asymmetric	*33*	*20*	*0*	*5*	*64*	*20*
[11], 2014	Symmetric	*15*	*18*	*0*	*7*	*42*	*18*
[12], 2012	Symmetric	*15*	*18*	*0*	*7*	*42*	*11*
[15], 2015	Symmetric	*15*	*16*	*0*	*7*	*46*	*16*
	Asymmetric	*33*	*21*	*0*	*10*	*106*	*21*
[16], 2016	Symmetric	*15*	*18*	*0*	*7*	*48*	*13*
	Asymmetric	*33*	*22*	*0*	*9*	*152*	*15*
[17], 2017	Symmetric	*15*	*20*	*0*	*7*	*50*	*13*
	Asymmetric	*33*	*24*	*0*	*9*	*154*	*15*
[18], 2018	Symmetric	*15*	*19*	*12*	*7*	*31*	*19*
[19], 2015	Symmetric	*15*	*16*	*0*	*7*	*42*	*16*
[20], 2015	Symmetric	*15*	*18*	*0*	*7*	*46*	*18*
[21], 2017	Symmetric	*15*	*16*	*0*	*7*	*70*	*11*
[23], 2017	Symmetric	*15*	*19*	*12*	*7*	*32*	*19*
	Asymmetric	*33*	*14*	*8*	*5*	*70*	*14*
[25], 2012	Symmetric	*16*	*16*	*0*	*7*	*52*	*13*
[26], 2011	Symmetric	*15*	*18*	*0*	*7*	*42*	*18*
	Asymmetric	*33*	*16*	*0*	*7*	*96*	*16*
[27], 2019	Symmetric	*15*	*16*	*0*	*7*	*58*	*11*
	Asymmetric	*33*	*20*	*0*	*9*	*169*	*13*
Proposed	Symmetric	*15*	*12*	*0*	*7*	*40*	*12*
	Asymmetric	*33*	*12*	*0*	*7*	*94*	*12*

In this paper, the proposed structure, which is shown in Figure 8, is simulated using fundamental frequency switching method in MATLAB/Simulink. To validate and verify the simulation results, an experimental setup of the proposed structure by using fundamental frequency switching method has been implemented. The simulation and the implementation were conducted for symmetric 15-level and asymmetric 33-level topologies. The experimental implementation data are given in Table 3. An overview of the experimental setup can be seen in Figure 9.

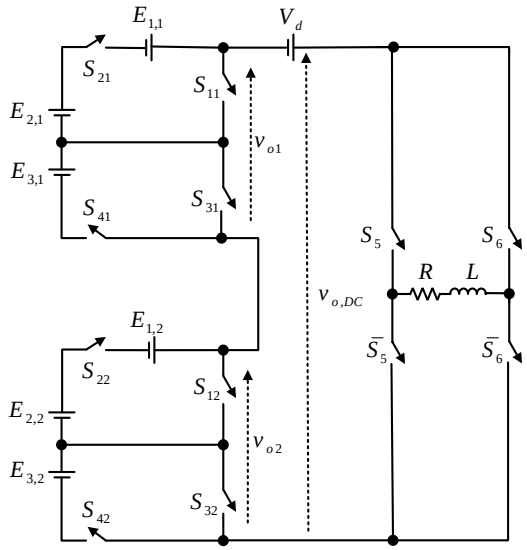


Figure 8: Symmetric 15-level and asymmetric 33-level structures for simulation and implementation

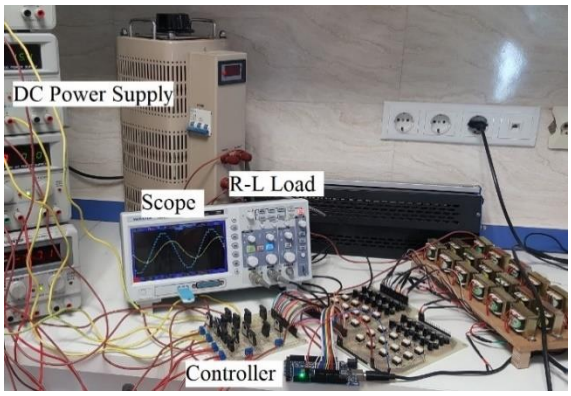


Figure 9: Overview of the experimental setup

Table 3
Experimental Setup Data

Parameters	Specification
DC Sources	4-16v
Output Voltage (Peak)	63-64v
Output Current (Peak)	1.8A
R_{Load}	25Ω
L_{Load}	80mH
MOSFETs	IRFP 450
GATE Driver	TLP 250
Diodes	1N5408
Controller	Arduino Mega 2560

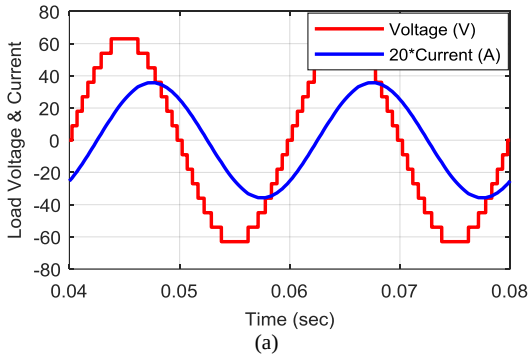
A. Symmetric Topology

In symmetric DC source mode, all input sources are equal to $E_{1,1}=E_{2,1}=E_{3,1}=E_{1,2}=E_{2,2}=E_{3,2}=V_d=9V$. In this situation, the output voltage peak which is 63 V that produced different voltage levels are given in Table 4.

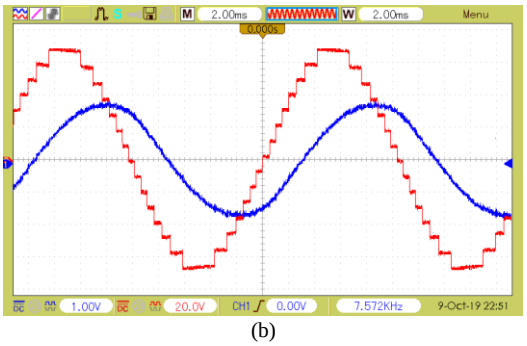
Table 4
States of Produced Voltage Levels

Level	Switch States (1=on & 0=off)									
	S_{11}	S_{21}	S_{31}	S_{41}	S_{12}	S_{22}	S_{32}	S_{42}	S_5	S_6
7	0	1	0	1	0	1	0	1	1	0
6	0	1	0	1	0	1	1	0	1	0
5	0	1	0	1	1	0	0	1	1	0
4	0	1	0	1	1	0	1	0	1	0
3	1	0	0	1	1	0	0	1	1	0
2	1	0	0	1	1	0	1	0	1	0
1	1	0	0	1	1	0	1	0	1	0
0	1	0	1	0	1	0	1	0	1	1
-1	1	0	1	0	1	0	1	0	0	1
-2	1	0	0	1	1	0	1	0	0	1
-3	1	0	0	1	1	0	0	1	0	1
-4	0	1	0	1	1	0	1	0	0	1
-5	0	1	0	1	1	0	0	1	0	1
-6	0	1	0	1	0	1	1	0	0	1
-7	0	1	0	1	0	1	0	1	0	1

The output voltage and current using fundamental frequency switching method for an inductive-resistive load are shown in Figure 10. In this figure, the 15-level output voltage constructed by 9-volt steps can be seen together with the output current. The current lags the voltage by 45 degrees.



(a)



(b)

Figure 10: 15-level output voltage and current waveforms and their THD for an R-L load using fundamental frequency switching: (a) simulation, and (b) experimental

Figure 10 (a) and (b) show the simulation and the implementation results, respectively. These are quite coincident between both results. The total harmonic distribution of the output voltage is presented in Figure 11. The value of THD is 4.89%. It is important to mention that this output voltage and THD are derived without the output filter. With respect to the THD value, the filter utilizing at inverter output is not required.

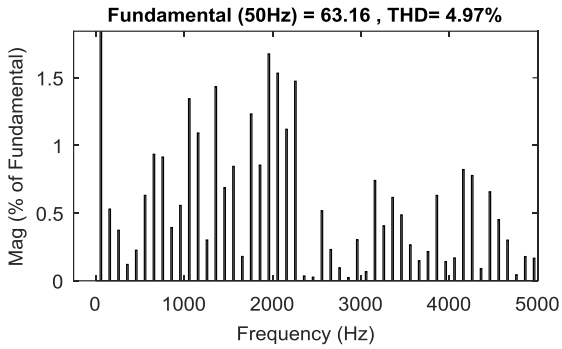


Figure 11: Total harmonic distribution of the output voltage (THD)

The generated voltage across the proposed cell-1 for the symmetric topology are shown in Figure 12. Also, the generated voltage across the proposed cell-2 for symmetric topology are shown in Figure 13. As illustrated in these figures, each cell generates voltage levels from1 to 3.

The voltage across the H-bridge module is shown in Figure 14. As mentioned, the H-bridge voltage includes positive levels only. Negative and zero levels are produced by switching off the H-bridge switches.

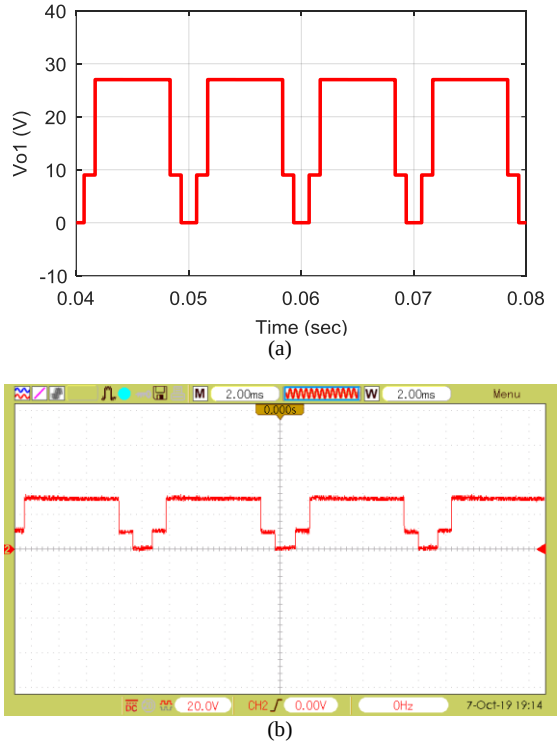


Figure 12: Generated voltage for symmetric sources across cell-1: (a) simulation, and (b) implementation

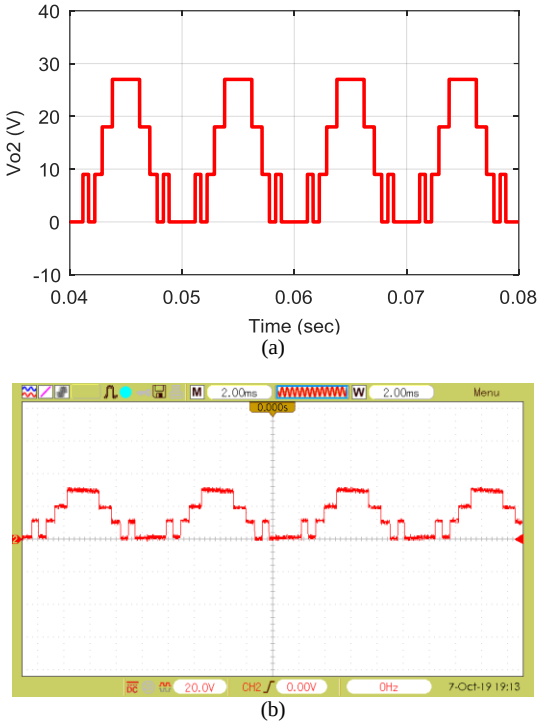


Figure 13: Generated voltage for symmetric sources across cell-2: (a) simulation, and (b) implementation

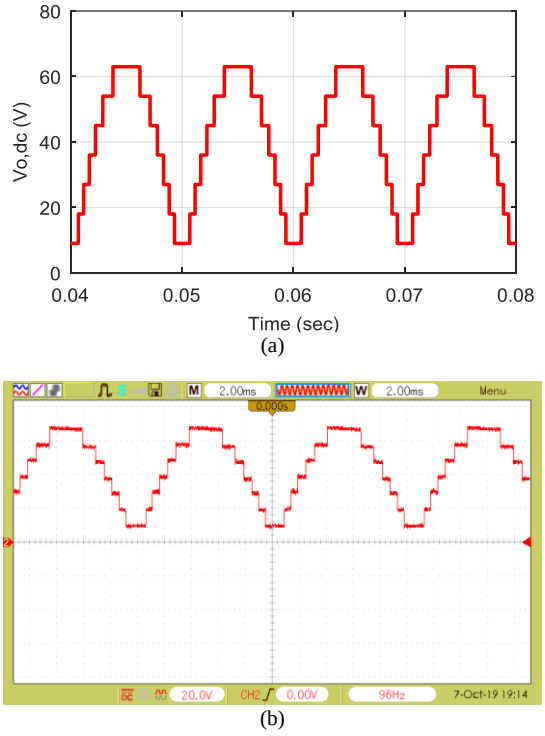


Figure 14: Voltage across the H-bridge module for symmetric sources mode: (a) simulation, and (b) implementation

B. Asymmetric Topology

For the state of the asymmetric sources, the DC source voltage of cell-2 is assumed to be fourfold of DC source voltage of cell-1. In this condition, 18 levels will be added to the output levels. The input DC sources are presented by $E_{1,1} = E_{2,1} = E_{3,1} = V_d = 4V$ & $E_{1,2} = E_{2,2} = E_{3,2} = 16V$. In this situation, the output voltage peak was 64 V.

The output voltage and current of using fundamental frequency switching method for an inductive-resistive load

are shown in Figure 15. This 33-level inverter with asymmetric topology operates properly. The output voltage constructed by 4 V steps. Figure 15 (a) and (b) show the simulation and the implementation results, respectively. These are quite coincident between both results. The total harmonic distribution of the output voltage is presented in Figure 15 (c). The THD has an appropriate value and is equal to 1.98%, which is a suitable value for the total harmonic distortion of the output voltage.

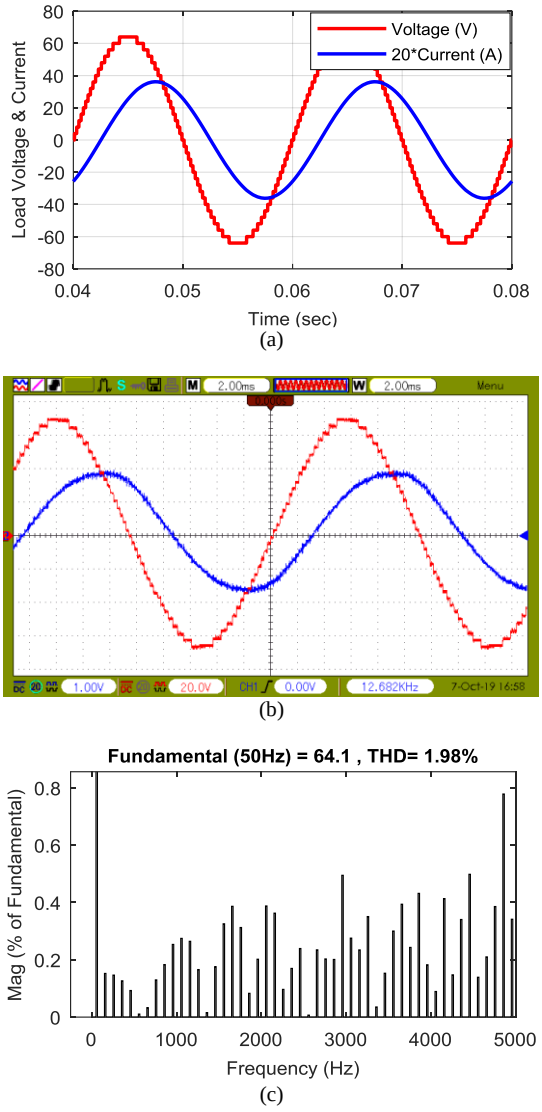


Figure 15: 33-level output voltage and current waveforms and their THD for an R-L load using fundamental frequency switching: (a) simulation, (b) experimental, and (c) voltage THD

The generated voltage by the proposed cell-1 and cell-2 for asymmetric topologies are shown in Figure 16. For the considered asymmetric DC sources, cell-1 produces voltage level from 1 to 3. Cell-2 produces voltage level 4, 8, and 12. Other output voltage levels are produced by composing the generated voltage levels and V_d. Agreement between the simulation and the implementation results is clear in Figure 16.

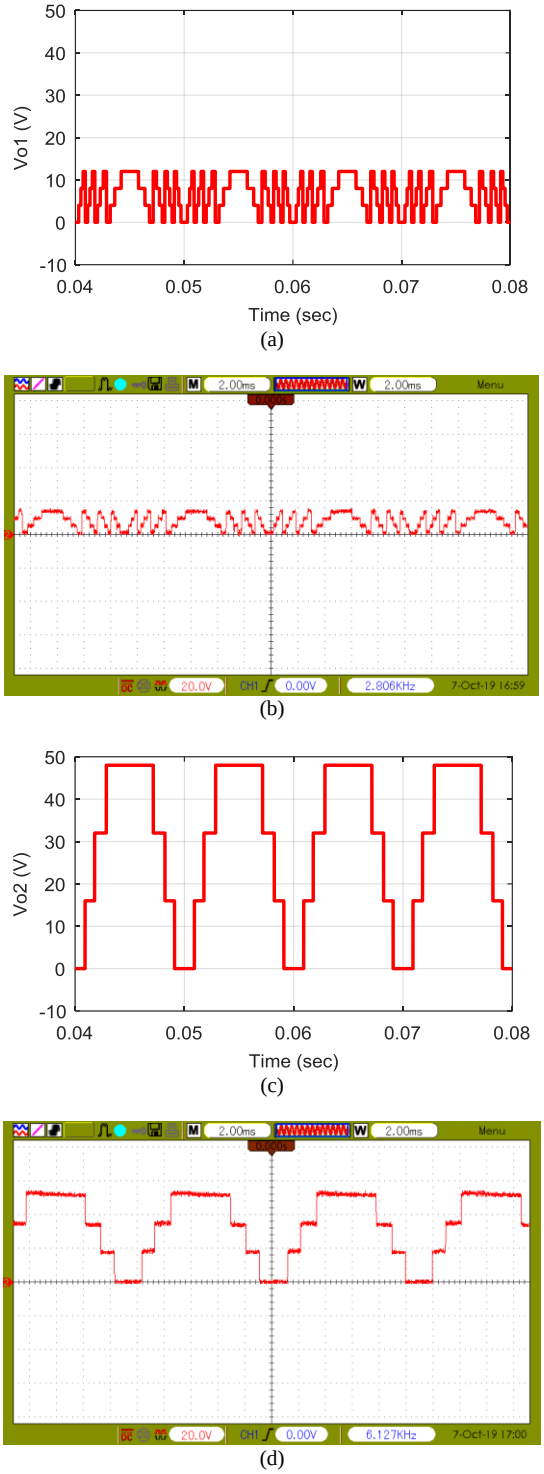


Figure 16. Generated voltage for asymmetric topology across cell-1 and cell-2: (a) cell-1 simulation, (b) cell-1 implementation, (c) cell-2 simulation, and (d) cell-2 implementation

The voltage across the H-bridge module is shown in Figure 17. Similar to symmetric condition, the H-bridge voltage includes positive levels in the asymmetric topology and the negative and zero levels are produced by switching off the H-bridge switches. There are quite coincident between the results.

As it can be seen, the provided results confirm that the proposed multilevel inverter is able to generate the desired output voltage waveform. These figures show good agreements in the simulation and experimental results.

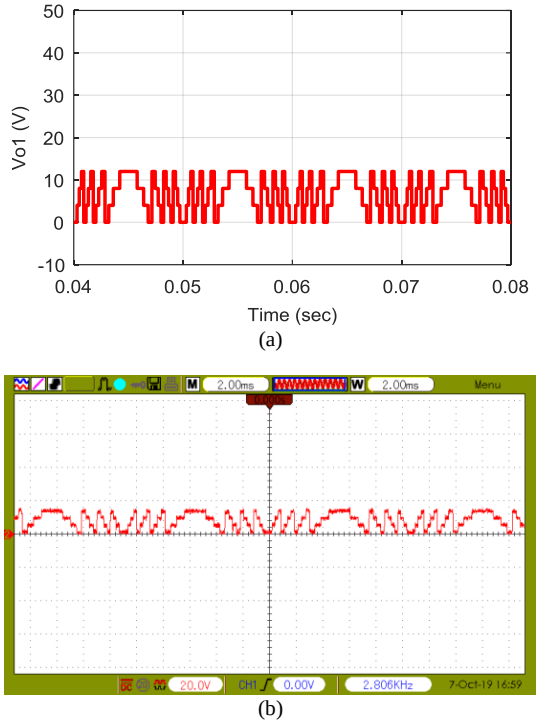


Figure 17: Voltage across the H-bridge module for asymmetric topology: (a) simulation, and (b) implementation

V. CONCLUSION

In this paper, a new basic cell is introduced for multilevel inverters. Then, a new structure is introduced by cascade connecting of a certain number of basic cells. The proposed structure is based on the H-bridge and, it is capable of operating in both symmetric and asymmetric topologies. Comparing the proposed structure with the recently proposed multilevel inverter structures in terms of power loss and efficiency, the number of switches, number of gate drivers, and total blocking voltage indicate that the proposed structure is a more suitable option and will require lower number of switches and lower volume and cost. A lower number of required devices lead to the reduction of the total implementation cost of converter. In addition, the implementation and control will be simple. The results of the laboratory implementation for both symmetric and asymmetric topologies indicate the suitable performance of the proposed structure and the complete agreement with the simulation results.

REFERENCES

[1] M. Vijeh, M. Rezanejad, E. Samadaei, and K. Bertilsson, "A general review of multilevel inverters based on main submodules: Structural point of view," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9479-9502, 2019.

[2] [2] M.A Jagabar Sathik and K. Vijayakumar, "An assessment of recent multilevel inverter topologies with reduced power electronics components for renewable applications," *Renewable and Sustainable Energy Reviews*, vol.82,no.3, pp.3379-3399, Feb-2018.

[3] [3] J. Rodriguez, . Bernet, P. K. teimer and I. E. Lizama, "A Survey on Neutral-Point-Clamped Inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[4] W. A. Halim, S. Ganeson, M. Azri, T. T. Azam, "Review of multilevel inverter topologies and its applications," *Journal of Telecommunication, Electronic and Computer Engineering (JTEC)*, vol.8, no. 7, pp. 51-56, 2016.

[5] M. Y. Lada, A. Khamis, M. Azri, N. I. Zolkifri, M. R. M. Nawawi, C. K. Gan, "A New Improvement of Reverse Voltage Single Phase Multilevel Inverter Topology," *Journal of Telecommunication, Electronic and Computer Engineering (JTEC)*, vol. 10, no. 2-6, pp. 65-70, 2018.

[6] E. Babaei, M. F. Kangarlu, and M. A. Hosseinzadeh, "Asymmetrical multilevel converter topology with reduced number of components," *IET Power Electron.*, vol. 6, no. 6, pp. 1188–1196, 2013.

[7] M. M. Rahimian, M. Hosseinpour, A. Dejamkhooy, "A Modified Phase-Shifted Pulse Width Modulation to Extend Linear Operation of Hybrid Modular Multi-level Converter," *J. Oper. Autom. Power Eng.*, vol. 6, no. 2, pp. 183-192, 2018.

[8] M. Hosseinpour, A. Seifi, A. Dejamkhooy, F. Sedaghati, "Switch Count Reduced Structure for Symmetric Bi-directional Multilevel Inverter Based on Switch-Diode-Source Cells," *IET Power Electronics*, 2020, Early Access.

[9] X. Sun, B. Wang, Y. Zhou, W. Wang, H. Du, and Z. Lu, "A Single DC Source Cascaded Seven-Level Inverter Integrating Switched Capacitor Techniques," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7184-7194, 2016.

[10] M. Hosseinpour, S. Mansouri, H. Shayeghi, "Selective Harmonics Elimination Technique in Cascaded H-Bridge Multi-Level Inverters Using the Salp Swarm Optimization Algorithm," *J. Oper. Autom. Power Eng.*, vol. 8, no. 1, pp. 32-42, 2020.

[11] E. Babaei, M.F. Kangarlu, M. Sabahi, "Extended multilevel converters: an attempt to reduce the number of independent DC voltage sources in cascaded multilevel converters," *IET Power Electron.*, vol. 7, no. 1, pp. 157-166, 2015.

[12] J. Ebrahimi, E. Babaei, and G. B. Gharehpetian, "A new multilevel converter topology with reduced number of power electronic components," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 655–667, 2012.

[13] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modulation, losses, semiconductor requirements of modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2633–2642, 2010.

[14] M. Ned, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications and Design* (2nd ed. Hoboken, NJ, USA: Wiley, 2001).

[15] E. Babaei, S. Laali and Z. Bayat, "A Single-Phase Cascaded Multilevel Inverter Based on a New Basic Unit with Reduced Number of Power Switches," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 922-929, 2015.

[16] R. S. Alishah, S. H. Hosseini, E. Babaaei and M. Sabahi, "A New General Multilevel Converter Topology Based on Cascaded Connection of Sub-Multilevel Units with Reduced Switching Components, DC Sources and Blocked Voltage by Switches," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7157–7164, 2016.

[17] M. Jayabalan, B. Jeevarathinam and T. Sandirasegarane, "Reduced switch count pulse width modulated multilevel inverter," *IET Power Electron.*, vol. 10, no. 1, pp. 10-17, 2017.

[18] C. Dhanamjayulu and S. Meikandasivam, "Implementation and Comparison of Symmetric and Asymmetric Multilevel Inverters for Dynamic Loads," *IEEE Accsess*, vol. 6, pp. 738-746, 2018.

[19] K. K. Gupta and S. Jain, "A Novel Multilevel Inverter Based on Switched DC Sources," *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3269 – 3278, 2014.

[20] M. R. J. Oskuee, M. Karimi, S. N. Ravadanegh and G. B. Gharehpetian, "An Innovative Scheme of Symmetric Multilevel Voltage Source Inverter with Lower Number of Circuit Devices," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 6965-6973, 2015.

[21] H. Samsami, A. Taheri, and R. Sammanbakhsh, "New bidirectional multilevel inverter topology with staircase cascading for symmetric and asymmetric structures," *IET Power Electron.*, vol. 10, no. 11, pp. 1315-1323, 2017.

[22] S. M. Ali, R. S. Alishah, and V. Krishnasay, "A New Generalized Multilevel Converter Topology with Reduced Voltage on Switches, Power losses and Components," *IEEE J. Emerging and Selected Topics Power Electron.*, vol. 7, no. 2, pp. 1094-1106, 2019.

[23] M. Saeedian, J. Adabi and S. M. Hosseini, "Cascaded multilevel inverter based on symmetric–asymmetric DC sources with reduced number of components," *IET Power Electron.*, vol. 10, no. 12, pp. 1468-1478, 2017.

[24] J. S. M. Ali, R. S. Alishah, N. Sandeep, S. H. Hosseini, E. Babaei, V. Krishnasay and U. R. Yaragatti, "A New Generalized Multilevel Converter Topology Based on Cascaded Connection of Basic Units," *IEEE J. Emerging and Selected Topics Power Electron.*, vol. 7, no. 4, pp. 2498–2512, 2019.

[25] M. F. Kangarlu, E. Babaei and S. Laali, "Symmetric multilevel inverter with reduced components based on non-insulated dc voltage sources," *IET Power Electron.*, vol. 5, no. 5, pp. 571–581, 2012.

[26] J. Ebrahimi, E. Babaei and G. B. Gharehpetian, "A New Topology of Cascaded Multilevel Converters With Reduced Number of

Components for High-Voltage Applications," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3109-3118, 2011.
[27] M. D. Siddique, S. Mekhilef, N.M. Shah and M. A. Memon, "Optimal Design of a New Cascaded Multilevel Inverter Topology With Reduced Switch Count," *IEEE Access*, vol. 7, pp. 24498-24510, 2019.
[28] R.S. Alishah, S.H. Hosseini, E. Babaei, M. Sabahi. "A new single-phase multilevel converter topology with reduced power electronic devices, voltage rating on switches, and power losses," *Int J Circ Theor Appl.*, vol. 46, no. 7, pp. 1372-1391, 2018.
[29] S. Yousofi-Darmian, and S.M. Barakati, "A New Asymmetric Multilevel Inverter with Reduced Number of Components," *IEEE J. Emerging and Selected Topics Power Electron.*, Early access.