Performance Investigation of Binary Counter with Different Clock Gating Networks

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***Abstract*— Three different clock gating network (CGN) have been used in this work to study their impact on the performance of binary counter. Different NMOS and PMOS transistor arrangements were used as CGN network. Its effect on the design of a synchronous binary counter i.e. 4-bit SBC-1T, -2T and -4T was observed to compute some of the essential performance parameters such as delay, slack time, maximum operating frequency, power dissipation, PDP and occupied area. The proposed counter design has been extended for 8 and 16-bit also. For synthesizing (TSMC 180-nm CMOS process) the proposed design, Leonardo Spectrum Tool provided by mentor Graphics has been used. For FPGA synthesis (Spartan-3E) of the proposed design, the ISE design suite provided by Xilinx has been used.**

***Index Terms*— Binary Counter; Clock Gating Network (CGN); Delay; FPGA; Layout; Operating Frequency; PDP; Power Dissipation; Slack Time; Verilog HDL.**

I. INTRODUCTION

In many VLSI systems, binary counters are the basic building blocks. An n-bit binary counter is a design that consists of a series of n-flip flops, and its count value can be 0 to $(2^n - 1)$ [1]. Fast binary counters design with low power consumption is the basic point of concern when designing high speed and low power digital systems for various applications. Counting time for process allocation in scheduling can be used as clock dividers (used in on-chip processor because sometimes processor works at lower processor than the actual frequency of the processor). Binary counter is broadly used in single or double slope analog to digital converter (ADC). In this case, the synchronous counter that increments at every clock pulse corresponds to sampled analog signal to rising and falling ramp generator and its value is further fed into digital to analog converter (DAC) to create its analog value [2-5]. In digital phase-locked loops (DPLL), time to digital converter (TDC) is used as a phase detector, in which the TDC is made up of up- and down-counter. It is used for capturing the information of fractional voltage controlled oscillator (VCO) to improve the accuracy of frequency detection [6-13]. Counter modules are used to design the variable of LFSR in the electronic-product-code (EPC) Gen-2 standard for ultra-high-frequency or radio frequency identification in various security problems [14]. High speed binary counter is used to count the number of photons in the photon counting camera [15]. In modern automation technology, some events are very fast, which cannot be detected in the program cycle. To detect such a high-speed event, a new technique term as high-speed counter (HSC) is introduced. HSC is advantageous when determining the speed of rotary motion in case of only one or few pulses per rotation. A part of this HSC is applicable at automation, process control, programmable logic controller, motor, stepper drives and motion control application i.e. step counter to collect the acceleration data [16], a counter is used to count the acceleration pulse delay in bipolar stepper-motor controller for slide application [17] and unified modeling language (UML) models [18].

Design techniques of counter are categorized into asynchronous [19] and synchronous counter. In synchronous counter, all flip-flops (FFs) are operated by the same clock pulse; however, in asynchronous counters design, LSB FF operated by the master-clock signal and output of each FF acts as a clock signal for succeeding FF. It is unreliable at higher frequency of clock signal due to large propagation delay. The synchronous counters designed with low power dissipation, high operating speed, and high reliability is important for designing parameters. Its power dissipation can be decreased by decreasing the power associated with the clock signal so that the wrong counter design decision may result in degradation of the performance of the overall system. The major source of power dissipation in the counter is the clock source due to high driving load from its nets or wire and the clock signal that is continuously present across flip-flops, which are not required to change their state, contributing a large power consumption. In counter application, the clock signal that consumes on average 25 to 40% of total power is observed [20].

In a synchronous binary counter, a generally high-frequency clock signal is used. It is usually driving a large load for the reason that clock signals have to reach several flip-flops distributed throughout the synchronous counter. So, the clock signal has been a major cause of power consumption because of the high driving load and the switching frequency. Also, it does not carry any information content because the clock signal is predictable. It is only used for synchronization purposes in synchronous counters. Clock gating methods have been demonstrated to the power efficiency of distribution and generation of the clock signal. To optimize the switching power dissipation of the synchronous counter due to clock signal, clock gating techniques are appropriate methods to overcome the high power dissipation due to the elimination of unnecessary activities in the clock signal.

Typically, NAND or NOR gate is used as a gating function to turn off the clock signal, when the flip-flop is not required for an extended duration. Clock gating is the most appropriate method for switching power reduction associated with clock signals. But the enable\disable rate of gating signal should be slower as compared to clock frequency since it will cause the degradation in timing performance of counters. Otherwise, it is an efficient technique for power saving due to clock activity. Additional gate delay due to gating function is the major issue for designing synchronous counter with clock

gating networks. So, the overall speed of the counter will be degraded due to the gating signal appears in the critical delay path. The major design challenge is the generation of the enable or disable signals through clock gating network (CGN) with minimum complexity of control logic circuits.

There are several efficient techniques for binary counter design present in literature. A counter design using clock gating presented by Wu Q et al. [21]. A power-efficient Johnson counter with a clock gating network is proposed in [22]. However, [21-22] required extra hardware to implement clock gating network, interconnection and clock buffer-network complexity that increase with the size of the counters. A priority encoder based counter design for low power application was proposed in [23], it is based on compressing the numerous inputs into a single output. A pulse latch base ring counter design is presented in [24]. But the drawback associated with [23-24] required additional hardware in terms of the pulse generator and priority encoder, enforcing the restriction on the design of wide bit binary counters. For optimization of power, a quasi-synchronous counter design is presented in [25]. In this approach, the clock signal for flip flops is derived from the main source of clock signal i.e. isolating the flip-flops from unwanted transitions of clock signal for optimizing the power consumption. Adiabatic logic and pass transistor based counter design for low power dissipation is proposed in [26-27]. Katreepalli and Haniotakis proposed a power-efficient technique for synchronous counters design. It is reducing the power consumption due to clock distribution arrangements at each FFs [28]. However, the downside of this architecture is the increase complexity of the clock gating network (CGN). It can cause the degradation in timing performance of counter or master clock frequency limitation due to gating signals that appear in the critical delay path.

To design VLSI circuits, two possible solutions such as Application-specific integrated circuits (ASICs) and programmable logic device (PLD, FPGA) based design have been proposed [29]. The ASICs design has many advantages concerning other solutions, such as low power dissipation, high speed, low cost for mass production, better controlling characteristics of input-outputs and high compact ICs design. However, there are some disadvantages, such as costly production for low volume due to high investment in CAD tools, workstations, and production manpower, while FPGA can be implemented with any hardware design. Circuits implementation in FPGA can be implemented in a short period of time comparatively because it is not required fabrication processes such as physical layout process, mask making, low NRE costs, and short time to market. In this case, FPGAs have been progressively used as the final product platforms.

In this paper, the performance of a synchronous binary counter with a different clock gating network (CGN) is investigated. Three different clock gating networks have been used for the generation of enable or disable signals through clock gating network (CGN) with minimum complexity of control logic circuits. Thereafter, FPGA and ASIC synthesis have been done using Spartan-3E FPGA and 180-nm CMOS technology respectively. The remaining brief of work is organized as follows: Section II presents the proposed binary CGN network and design of binary counter for 4, 8, and 16-bit by utilizing the CGN network. Section III presents a design methodology for ASIC. Section IV presents a physical layout of proposed binary counter architecture. Section V presents the performance comparison between the 180-nm CMOS process and Spartan 3E FPGA. Finally, Section VI concludes the work.

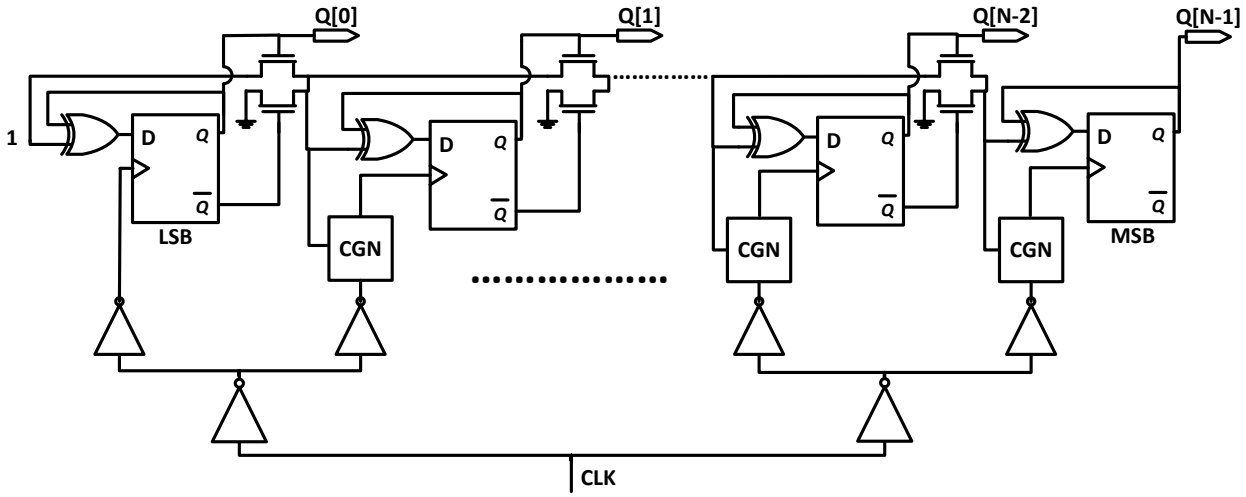
II. Design of Binary Counter with CGN Networks

To design high-performance synchronous circuits, it is necessary to use the clock distribution network. This network contains multiple hierarchy tree to feed the sequential elements. The clock distributed tree has been made by inserting buffers, which describe the chain of inverters design to drive a large capacitive load with minimum propagation delay [30]. To reduce the delay time due to driving a large load capacitance associated with several flip-flops in counter circuits, the buffer insertion is necessary to provide a large amount of pull-down and pull-up current to quickly charge or discharge a load capacitor. This technique handles a large capacitive load by using the buffer between a flip-flop (facing the large load) and the load itself (clock source) in a synchronous counter design. The clock distribution network is shown in Figure 1(a).

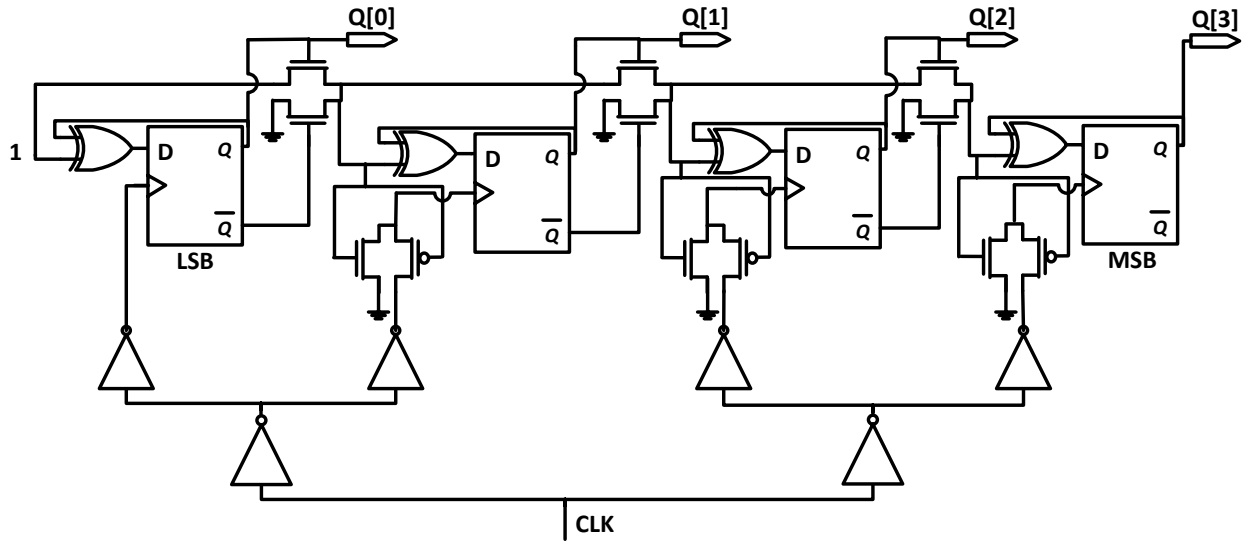
There are various methods to design a binary counter, in which the most widely used is the D-flip-flops as they are used to reduce logic gate complexity of counter circuits, convert the D-flip-flops into T- lip-flops using XOR gate that offers toggling at each clock pulse with less hardware complexity. The fundamental step to design a counter, is the 'n' number of flip-flops are required for n-bit counter design.

In conventional CGN network, NAND or NOR gates gating function are typically used to turn off the master clock feeding throughout the counter [28] [31]. The signal from the gating network should be disabled or enabled at a much slower rate as compared to the master clock frequency. To improve the performance, we proposed the three different CGN network by using the arrangement of NMOS and PMOS transistor to overcome the drawback of NAND or NOR gate based on gating techniques. By utilizing the CGN network, we proposed three architecture of binary counters i.e. SBC-1T, SBC-2T, and SBC-4T.

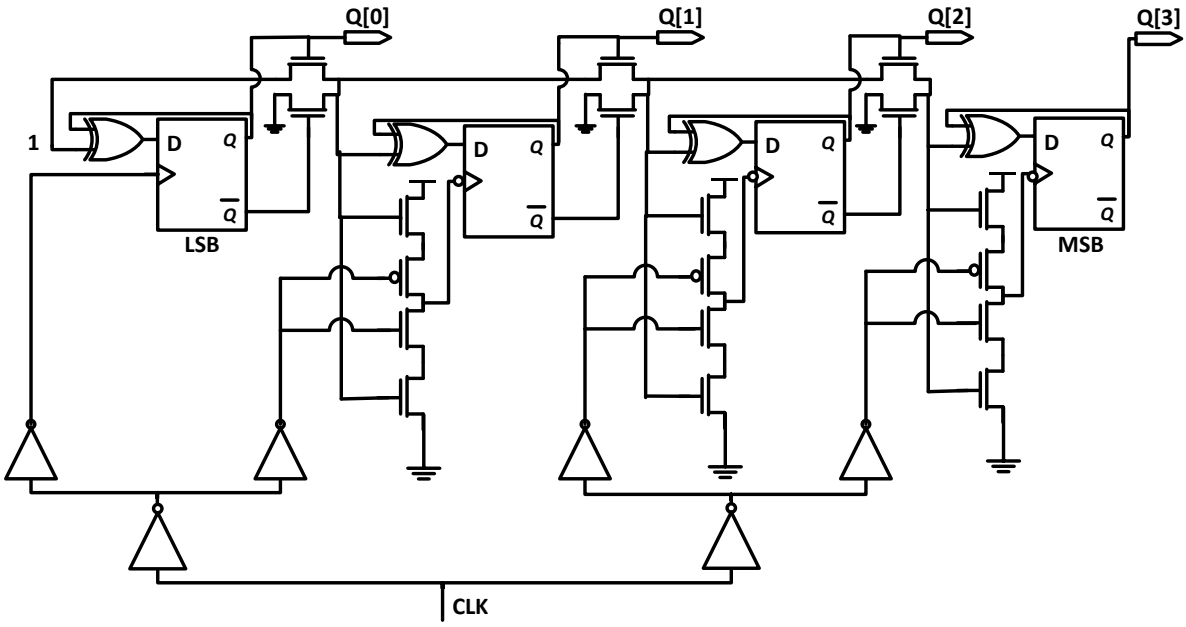
Figure 1(a) shows the general architecture of N-bit binary counter with CGN networks. This architecture, containing two parallel NMOS transistors acts as a highly efficient AND gate. Its gate terminal is controlled output of flip-flop. So, when the time single transistor is ON, there is no sneak path between and ground. Clock triggering at each flip-flop is controlled by a clock gating network (CGN) except the LSB and pass through the repeaters or buffers. Buffers or repeaters are used to drive the master clock throughout the counter circuits. Multiple levels in tree networks are necessary to avoid the slow rate of rise or fall time at the input of the CGN network and to decrease the noise by controlling the edge rate of the clock signal.



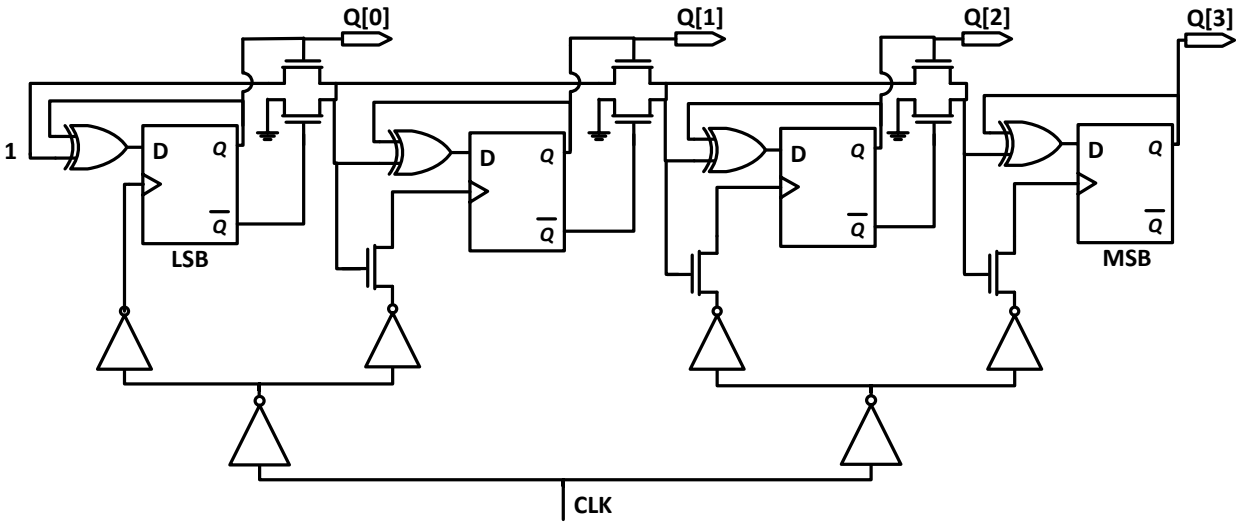
(a) Generalized structure of binary counter with clock gating network (CGN).



(b) 4-bit SBC-2T



(c) 4-bit SBC-4T



(d) 4-bit SBC-1T

Figure 1: Proposed four new clock gating based binary counter architecture

Furthermore, for higher bit synchronous counters, we can use the CGN network at each level inside the buffer network, to add optimization of power in buffer network. It is used to further reduce the level of the master clock, depending on the activity of FFs in a counter circuit.

Figure 1(b), 1(c) and 1(d) show the proposed synchronous binary counter with CGN networks i.e. synchronous binary counter with two transistor gating networks (SBC-2T), four transistor gating network (SBC-4T) and one transistor gating network (SBC-1T) respectively. We can see that the proposed synchronous binary counter design employs a new transistors arrangement, which acts as a CGN network. Unlike conventional synchronous counter design, here we used a proposed CGN network to drive all FFs.

In the SBC-2T counter of Figure 1(b), a combination of parallel NMOS and PMOS transistor acts as a CGN network. It activates only when the previous FFs output are high. A combination of both transistors acts as highly efficient AND gate, and it is activated when the previous flip-flop is active. Master clock input is connected through the source terminal of PMOS to pass the active state of the master clock. The advantage of this arrangement of transistor is that there is no sneak path between the supply and ground because at this time, only a single transistor is active.

Similarly, in the SBC-4T counter of Figure (c), the clock is directly connected to the first flip flop (without not gate). For other flip flops, clocks are passed through a combination of four transistors, which are working as a CGN network, In this condition, the outer transistors of CGN network are controlled by precedent flip-flop output. Here, it is activated only when the precedent flip-flops output is high. Inner transistors of CGN network are controlled by a master clock signal, so that when the precedent flip-flop's output is active, the CGN network passes the inverted value of the master clock and for rest of the cases, the output will be in a high impedance state. Therefore, the LSB FF is required to be positive edge triggered, while other FFs is to be negative edge triggered in order to attain synchronization in the overall architecture.

In SBC-1T counter of Figure 1(d), only one NMOS transistor act as a CGN network. The master clock is driven by this nMOS transistor which is activated only when the precedent flip-flops output is high.

III. Methodology for ASIC Design

This work was evaluated on the Mentor Graphics tool. A Semicustom (front-end) design flow adopted in this work is shown in Figure 2.

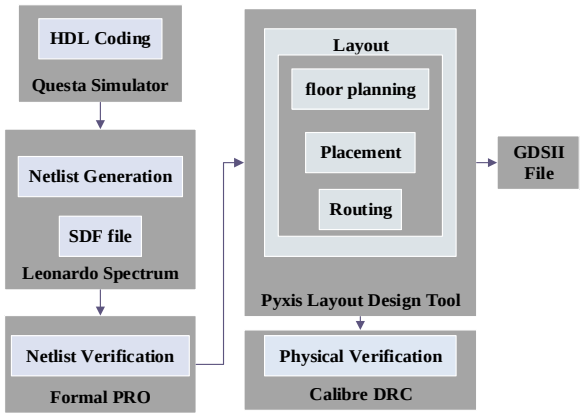


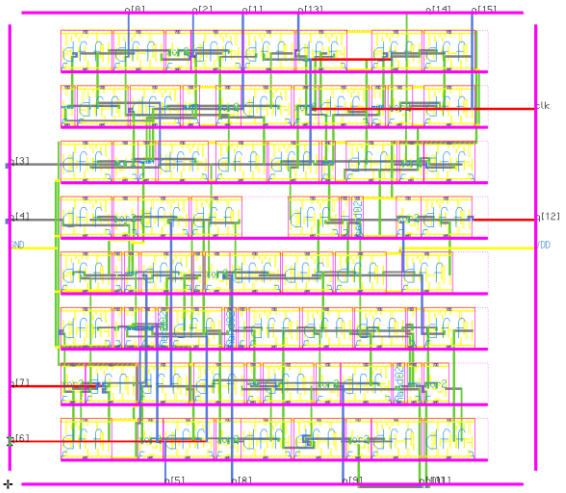
Figure 2: Design flow of the experiments

The summary of workflow details are as follows:

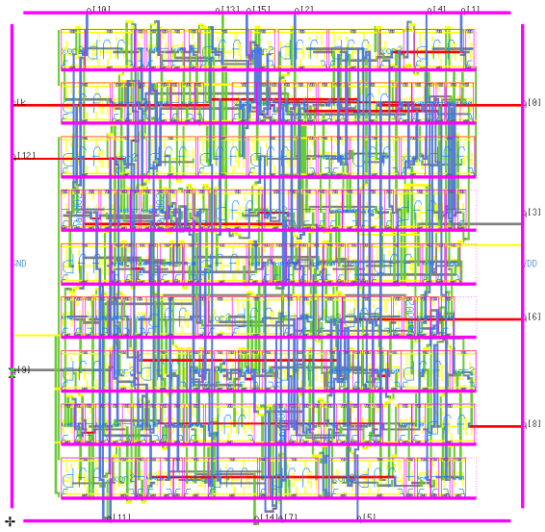
- HDL code in Verilog for the proposed algorithm is written using the Questa Simulator tool of mentor graphics. Functional Verification is carried out using the RTL (register transfer level) design.
- Synthesis on the RTL Code using Leonardo Spectrum Tool is carried out by generating Netlist and Standard Delay Format (SDF) file. Here, Netlist refers to textual description of the connection of gates. It is then used to produce the layout of the chip. SDF file is the interpretation and representation of timing data for use at the design process and it is used for dynamic and static time analysis. For this synthesis operation, select the technology file as TSMC 180-nm CMOS and specify the frequency.
- After synthesis on RTL, we perform the post-synthesis verification of netlist that can be done by Equivalence Checking or Formal PRO Tool, which operates and verifies the netlist, which is generated from Leonardo Spectrum Tool. For verification of netlist, one requires dot v (.v) and sdf file.

- To generate layout for the Netlist of HDL code, we used the Pyxis Design Tool. In this operation, first, we select the files to initiate layout operation such as Verilog Netlist, Process and Rule file. At this stage, the netlist of the gate level circuit is converted into a complete physical layout representation. For physical design, the following steps are necessary: floor planning for placement of numerous blocks, Input/output pads across the chip area depend on the designing constraints, physical elements placement within each block is done followed by detailed and global routing for connecting all the elements across the chip area.
- After layout, import the GDSII (GDS2) file from this tool, which is used by the fabrication foundry to fabricate the chip. The physical layout should be done based on silicon foundry design rules.
- At this stage, a physical verification is required using Calibre DRC (Design Rule Check) to ensure the layout phase.

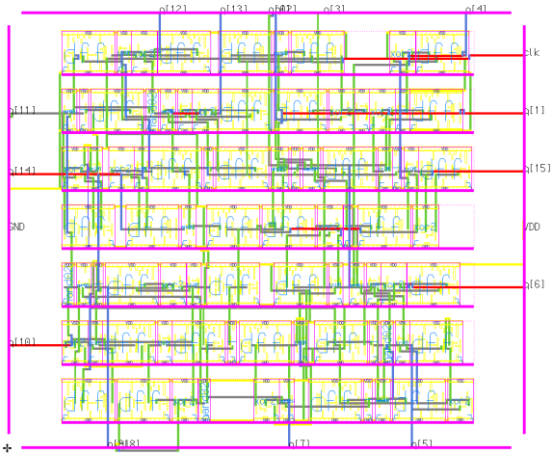
The Layout of binary counter of proposed Architecture using a 180-nm standard CMOS technology file (TSMC 180-nm) is shown in Figure 3.



(a) 4-bit SBC-2T



(b) 4-bit SBC-4T

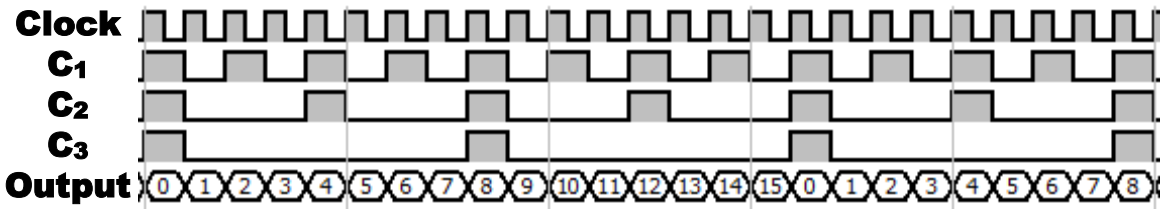


(c) 4-bit SBC-1T

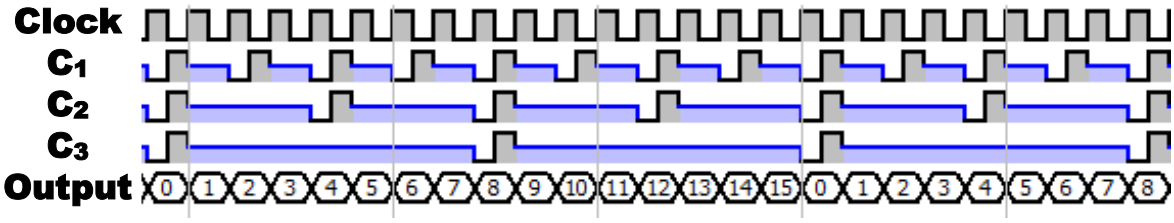
Figure 3: Physical layout of proposed counter based on 180-nm CMOS technology

IV. Result and Discussion

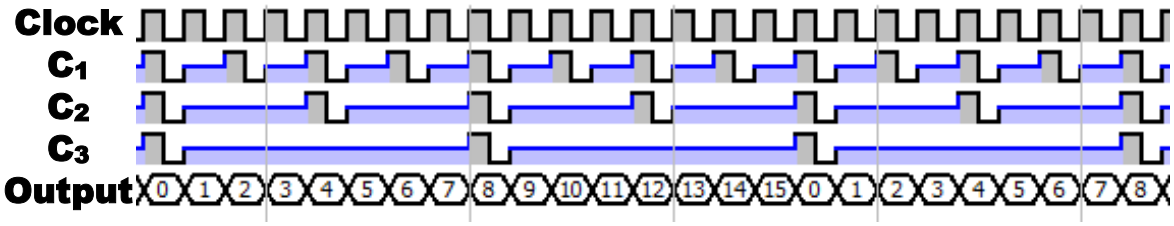
The proposed binary counters with CGN network for 4, 8, 16-bit size are coded in Verilog HDL. These results are synthesized using the TSMC 180-nm CMOS process in the Leonardo spectrum tool and Spartan-3E FPGA in the ISE design suite. The synthesis of the proposed design was done at 100 MHz frequency constraints. The simulated output based on the Verilog test bench for 4-bit proposed synchronous counters with the CGN network is shown in Figure 4. Performance parameters of proposed counters and existing literature of binary counter [28] are shown in Table 1 and 2 for ASIC and FPGA synthesis respectively.



(a) 4-bit SBC-2T



(b) 4-bit SBC-4T



(c) 4-bit SBC-1T

Figure 4: Clock signals and output waveform of proposed four new clock gating based binary counter

Table 1
Synthesis Report Based on 180 nm CMOS Technology with 100 MHz Operating Frequency

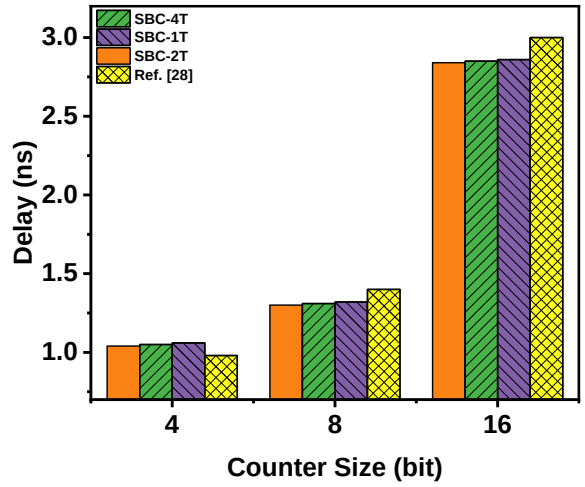
Binary Counter	4-bit				8-bit				16-bit			
	Maximum Operating frequency (MHz)	Delay (ns)	Slack Time (ns)	Area (no. of gates)	Maximum Operating frequency (MHz)	Delay (ns)	Slack Time (ns)	Area (no. of gates)	Maximum Operating frequency (MHz)	Delay (ns)	Slack Time (ns)	Area (no. of gates)
Ref. [28]	840.3	0.98	8.81	59	621.5	1.40	8.39	141	311.7	3.0	6.79	305
SBC-2T	800.9	1.04	8.75	57	660.9	1.30	8.49	129	328.0	2.84	6.95	274
SBC-4T	795.2	1.05	8.74	64	657.0	1.31	8.48	145	327.1	2.85	6.94	308
SBC-1T	788.2	1.06	8.73	47	652.1	1.32	8.47	105	325.9	2.86	6.93	222

Table 2
Synthesis Report Based On Spartan-3E FPGA with 100 MHz Operating Frequency

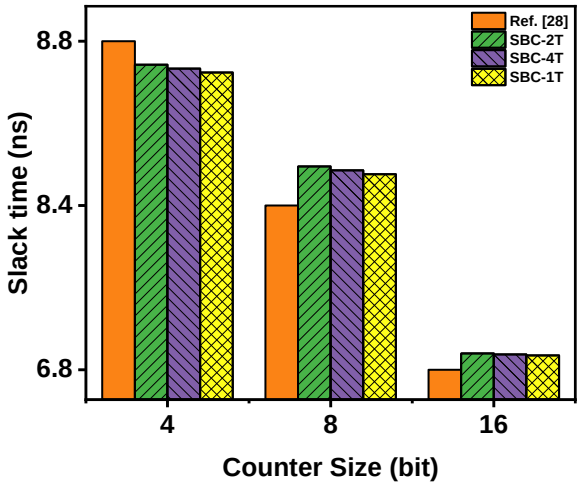
Binary Counter	4-bit					8-bit					16-bit				
	Maximum Operating frequency (MHz)	Delay (ns)	On chip power dissipation (mW)	PDP (10^{-12}J)	Area (occupied slices)	Maximum Operating frequency (MHz)	Delay (ns)	On chip power dissipation (mW)	PDP (10^{-12}J)	Area (occupied slices)	Maximum Operating frequency (MHz)	Delay (ns)	On chip power dissipation (mW)	PDP (10^{-12}J)	Area (occupied slices)
Ref. [28]	436..862	2.289	113.89	260.69	8	408.497	2.448	119.47	292.46	17	386.615	2.587	120.63	312.07	43
SBC-2T	509.697	1.962	114.34	224.34	8	474.732	2.106	120.68	254.15	18	427.004	2.342	121.80	285.26	41
SBC-4T	509.671	1.962	113.55	222.78	7	483.688	2.067	119.43	246.86	14	439.754	2.274	120.53	274.09	33
SBC-1T	509.671	1.962	113.85	223.37	7	462.963	2.16	119.78	258.72	15	429.655	2.327	121.05	281.68	35

A. Performance Analysis using 180 nm CMOS Technology

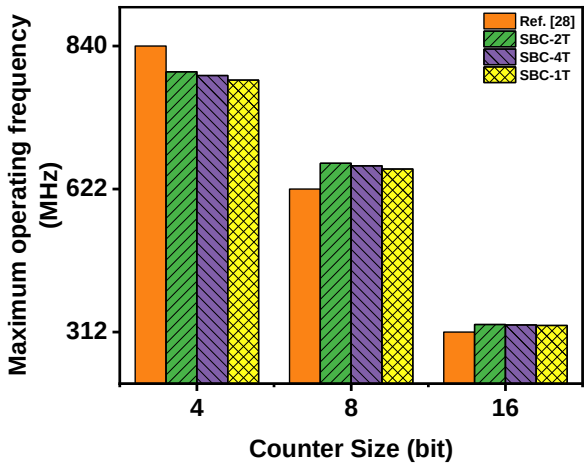
Table 1 shows the ASIC synthesis result of the proposed counters and existing binary counter [28] in terms of delay, slack time, maximum operating frequency and utilized area. In this analysis, we evaluated the static time analysis in which we found the maximum possible delay of the proposed three different architectures of the synchronous counter and existing binary counter [28]. From Table 1, it shows that the reduction in delay for synchronous counter with proposed methodology was 5.7%, 7.14%, 6.4% for SBC-1T, SBC-2T and SBC-4T counter respectively, when compared to conventional method. The next parameter is the slack time as a difference between the desired arrival time of a clock signal and its actual arrival time. Its consideration is important because one needs to understand how fast the counter is going to run and interact with the other modules. In this study, the slack time at 100 MHz frequency was calculated and it was found that the slack time has improved by 2.1%, 2.3%, 2.2% for SBC-1T, SBC-2T and SBC-4T counter respectively. It indicates whether a timing constraint is being violated or not. Typically, a user can specify an acceptable slack value, that is, a slack threshold. Here, we found the maximum possible operating frequency with acceptable slack time of counter and it increased by 6.2%, 4.7%, 5.3% for SBC-1T, SBC-2T and SBC-4T counter respectively. Thereafter, an analysis of the utilized area of a binary counter was conducted. Graphical representation of performance parameters such as delay, slack time, maximum operating frequency and area are shown in Figure 5(a), 5(b), 5(c) and 5(d) respectively.



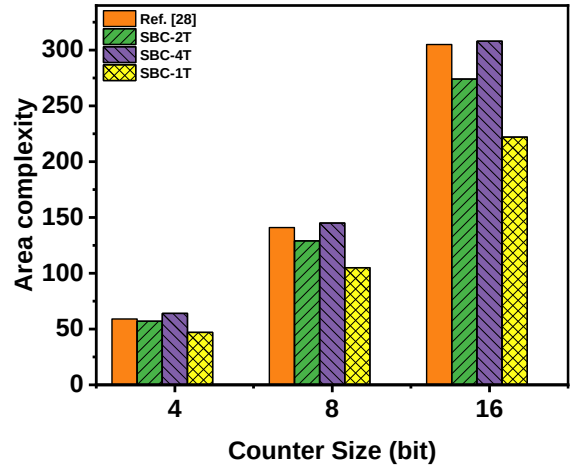
(a) Delay



(b) Slack time



(c) Maximum operating frequency



(d) Area complexity

Figure 5: Comparison analysis of clock gating based binary counter using 180 nm CMOS technology

B. Performance Analysis using Spartan-3E FPGA

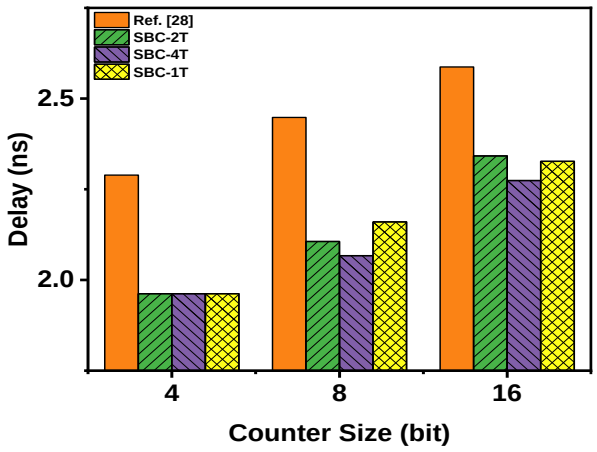
Table 2 shows the Spartan-3E FPGA synthesis result of the proposed counters and the existing literature of binary counter [28] in terms of delay, maximum operating frequency, on-chip power dissipation, power delay product (PDP) and utilized area in terms of lookup tables. The proposed CGN network has its main benefit in terms of high speed and low power consumption. In the existing literature [28], clock gating techniques were used for lower power consumption, in which its timing performance was degraded due to the conventional clock gating logic network. This analysis evaluated the maximum possible delay of proposed three different architectures of the synchronous counter and the existing literature of counter [28]. From Table 2, it is shown that the reduction in delay for synchronous counter with proposed methodology was 11.8%, 14.0%, 15.6% for SBC-1T, SBC-2T and SBC-4T counter respectively, when compared to conventional method. The improvement in terms of power consumption for the proposed synchronous counter design is almost the same as the existing work.

We evaluated the maximum operating frequency of the proposed synchronous counter and it was increased by 13.3%, 16.0%, 18.4% for SBC-1T, SBC-2T and SBC-4T counter respectively as compared with the conventional architecture. Further, the utilized area in terms of occupied slices of the proposed counter was analyzed. We found the occupied slices decreased by 18.6%, 4.6%, 2.3% for SBC-1T, SBC-2T and SBC-4T counter respectively, when compared to conventional. Finally, we achieved an improvement in PDP by 14.4%, 14.2% and 14.5% corresponding SBC-1T, -2T and -4T proposed architecture of binary counter. The graphical representation of performance parameters such as delay, maximum operating frequency, power dissipation, utilize the area and PDP are shown in Figure 6(a), 6(b), 6(c), 6(d) and 6(e) respectively.

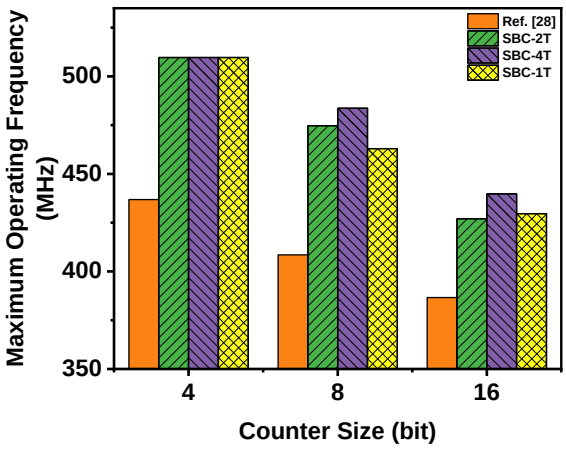
V. CONCLUSION

In this brief, we investigated the performance of a binary counter with a different clock gating network (CGN). Three different CGN network were used for the implementation of high speed and power-efficient synchronous binary counters i.e. 4bit SBC-1T, -2T and -4T to overcome the performance degradation. An improved speed of a circuit which is the degraded due to gating signal in a critical delay path resulted in saving the power consumption by reducing unnecessary activities of clock signal inside the counter circuit with minimum hardware overhead. The results of the proposed architecture were compared and contrasted with the results obtained for the previous clock gating based counter [28]. It

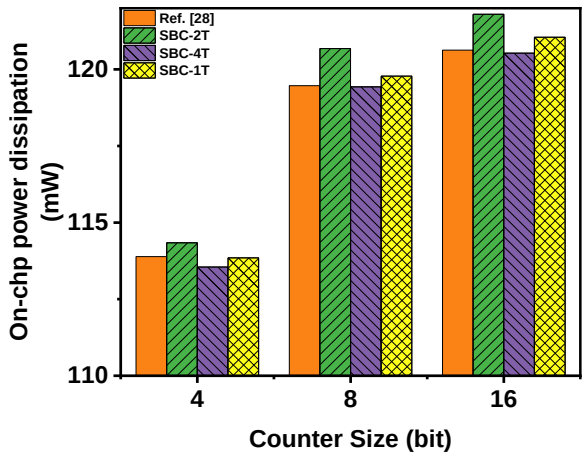
demonstrates that the proposed counting operation is faster with lower power dissipation than counter available in the literature [28]. It was also suggested that the proposed counter can be operated at a high-frequency clock signal compared to the conventional binary counter. Analysis has been done in this work to demonstrate the usage of the proposed CGN network-based synchronous counter circuit for different bit sizes. This work demonstrates that the proposed CGN network-based counter architecture can significantly reduce the delay by 15.6%, PDP by 14.5% and it can successfully be operated at 18.4% higher frequency compared to the earlier reported designs, which provides lower power consumption with the minimum utilized area.



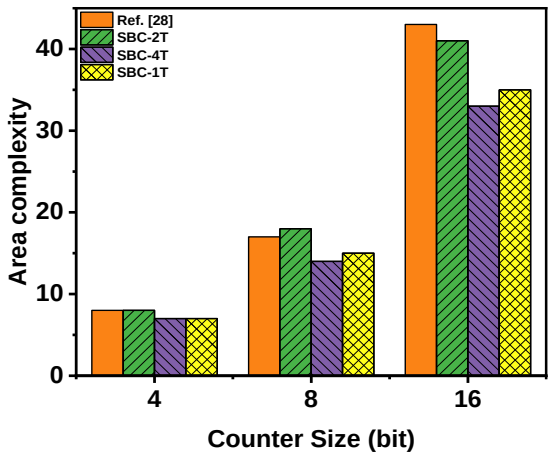
(a) Delay



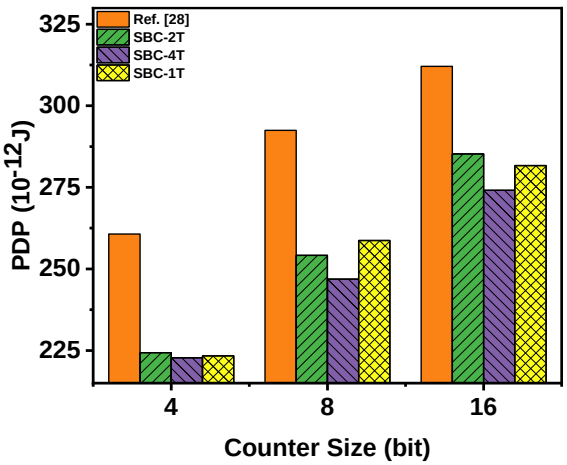
(b) Maximum operating frequency



(c) On-chip power dissipation



(d) Area complexity



(e) PDP

Figure 6: Comparison analysis of clock gating based binary counter based on Spartan-3E FPGA

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