A High Frequency Ring-VCO with Wide Tuning Range

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***Abstract*—In this paper, a high frequency ring-VCO using an improved differential delay-cell (DD-cell) is presented. The proposed DD-cell benefits from a bandwidth extension technique. Facilitated by the wide band cell, the oscillation frequency of the proposed VCO can be increased up to 15.45 GHz. The DD-cell has tunable loads, which is used to change the operating frequency of the proposed VCO between 6-15.45 GHz. The proposed VCO has been designed and simulated in CMOS 65nm process with 1V supply voltage and consumes about 4.38 mW of power when oscillating at 15.45 GHz and 3.7 mW for 8 GHz output signal. The FoM of the proposed ring-VCO is equal to 153.7 dBc/Hz.**

***Index Terms*—Differential Delay Cell; High Frequency; Ring-VCO; Wide Band.**

I. INTRODUCTION

The millimeter-wave transceivers are emerging as a promising high speed communication alternative [1-3]. The high frequency signal generation, which is performed by a PLL is an inevitable part of these transceivers [4-5]. The high frequency PLL is usually a power hungry block and can increase the power consumption of the transceiver to a value that hinders the practical realization of the transceiver into a mobile device. In the design of a high frequency PLL, the most challenging parts to realize are the high frequency VCO [6] and divider [7-9] as they account for big part of the total power consumption of the PLL block. When the frequency of operation of PLL is pushed to millimeter frequencies, the contribution of the VCO and divider to the total power consumption becomes more significant [9].

In the applications of moderate phase noise specification, the ring-VCO can be used with a small area occupied on the chip. However, most of the reported ring-VCO's in the literature are limited to a few GHz operational frequency [10][11][12][13][14][15][16][17][18]. Other designs, which have been able to achieve oscillation frequency above 10 GHz are using some frequency multiplication [19] or push-pull techniques [20], which will increase the power consumption of the circuit about 2-3 folds.

This paper introduced a simple DD-cell with wide bandwidth that is utilized inside a four-stage ring-VCO, which subsequently will easily be able to reach the operation frequencies beyond 10 GHz. This improvement, at the same does not have any power or area overhead on the circuit.

The paper is organized as follows; the Section II of the paper presents the proposed DD-cell. In Section III, the ring-VCO structure is briefly explained, and in Section IV simulation results of the proposed ring-VCO are presented. The paper is summarized with conclusions in Section V.

II. THE DIFFERENTIAL DELAY CELL (DD-CELL)

The circuit schematic of a traditional DD-cell is shown in Figure 1. It is in fact a differential amplifier with tunable loads; tail current is controlled by a bias voltage. This DD-cell is used in a feedback loop to realize a ring oscillator, which can be realized with even number of stages. A block diagram of this four-stage differential ring oscillator is shown in Figure 2. Each of the presented blocks in Figure 2 can be modeled by a single pole gain stage with a transfer function as in (1),

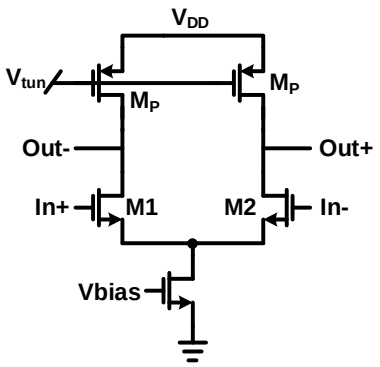


Figure 1: The traditional DD-cell

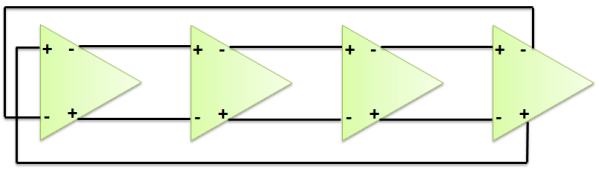


Figure 2: A typical 4-stage differential ring oscillator structure

$$H(s) = \frac{A_0}{1 + \frac{S}{\omega_{P1}}} \tag{1}$$

In this equation, A_0 is low frequency gain of each block. The free running frequency of the oscillator will be equal to $\omega_{P1,}$ which is the 3dB bandwidth of each gain block and is defined as:

$$\omega_{P1} = \frac{-1}{(ro_p || ro_n)\,(C_P + C_N)} \tag{2}$$

In this equation, r_{op} and r_{on} are small signal output resistance of the NMOS (M_1) and PMOS (M_P) transistors in

Figure 1, respectively. The C_P and C_N are the parasitic capacitances of the NMOS and PMOS transistors, which contribute to total output load capacitance. There is a loading capacitor from the next stage when the delay-cell is used in the VCO, which is negligible and neglected in this analysis. The smaller output resistance could increase the 3dB bandwidth of each gain block. However, the total output resistance, which is equal to $r_{op}||r_{on}$ is set by a minimum required gain for oscillation, so its value could not be reduced below a certain amount. The value of parasitic capacitances CN and CP is determined by the size of the transistors. The size of transistors is also set by a minimum required gain for oscillation if the value of power consumption is limited. Therefore, bandwidth of the gain block is limited by a minimum required gain for the oscillation.

The proposed DD-cell with larger bandwidth is shown in Figure 3. It uses two series resistors (R) at the output of the gain block. The function of these resistors is to decouple the capacitors of the NMOS and PMOS transistors and to insert a zero in the transfer function of the cell. In order to be able to analyse the proposed bandwidth extension technique, the small signal model of the circuit is utilized.

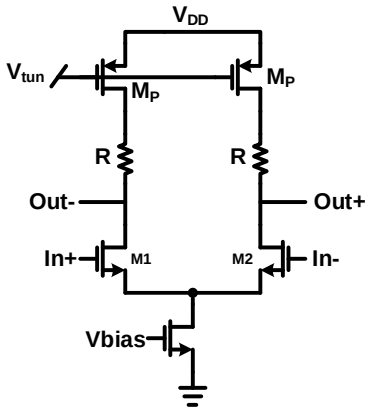


Figure 3: The circuit schematic of the proposed DD-cell

The circuit model of the proposed DD-cell is shown in Figure 4. The current source I_{sig} models the transconductance of the input transistors M1 or M2. The r_{on} and r_{op} resistors in this model, represent the output resistance of the input NMOS (M1/M2) and load PMOS transistors (M_P), respectively. The C_N and C_P capacitors are sum of all the parasitic drain capacitances associated with NMOS and PMOS transistors, which are merged to form a single capacitor. In this model, R is the inserted resistor for bandwidth extension of the circuit. Without R resistor, the circuit is the same as the one in Figure 1 and then the dominant pole will be equal to (2).

The transfer function (TF) of the impedance seen by the current source I_{sig} in Figure 4 is represented by (3). This TF has two poles and one zero, which were introduced by the insertion of the R resistor. By setting R=0, the poles of the TF will be merged and equal to the value in (2). The poles of the Z_{sig} in (3) are shown in (4), at the bottom of the page, and its zero frequency is equal to (5).

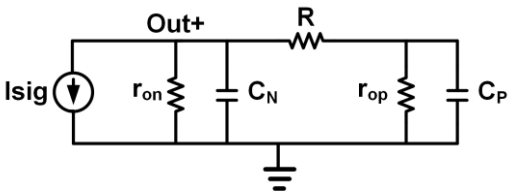


Figure 4: The small-signal model of the proposed DD-cell

$$Zsig = \frac{R\left(1 + r_{op}C_PS\right) + r_{op}}{Rr_{op}C_NC_PS^2 + \left(r_{op}C_P + r_{op}C_N + RC_N + \frac{Rr_{op}C_P}{r_{on}}\right)S + \frac{R + r_{op} + r_{on}}{r_{on}}} \quad (3)$$

$$Sz = -\left(\frac{1}{RC_P} + \frac{1}{r_{op}C_P}\right) \quad (5)$$

By inserting R resistors at the output of the proposed DD-cell, a pole and a zero are introduced to TF of the amplifier. According to (5), for small values of R, the zero frequency is moving to higher frequencies: This is also true for the second pole (P2) in the TF. On the other hand, the dominant pole (P1) of the amplifier is less affected by the variations of the R resistors. In order to benefit from the addition of zero frequency to extend the bandwidth of the DD-cell, the value of R resistors is chosen based on the fact that the zero frequency should be close to the first pole and away from the second pole to be effective in extending the amplifier bandwidth. Figure 5 shows the amplifier poles and the zero locations for different values of the R resistors.

The value of other parameters in TF has been selected based on the data obtained from circuit simulation. As shown in the figure, for values of R resistors, which are smaller than 150Ω, the zero is far from P1 and couldn't be useful for bandwidth extension. Additionally, for values larger than 300Ω, the zero frequency is almost cancelled by P2 and cannot reduce the TF roll off caused by the first pole and increase the bandwidth. For the very small values of the R resistor, the zero location is moving to higher frequencies and is less effective in decreasing the roll off. On the other hand, for very large values, the zero frequency is completely canceled by the second pole. In this paper, the value of the R resistors was chosen to be equal to 200Ω, which will be explained in detail in the continuation of the paper.

The bandwidth of the proposed DD-cell extracted from TF for the values of C_N parasitic capacitor in the range of 2-20 fF has been plotted and shown in Figure 6. It is also compared with the bandwidth of the original DD-cell. Both amplifiers have the same gain value in order to have a fair comparison. The results in this figure indicate that for these range of values for C_N capacitor which are the most encountered values for the parasitic capacitance of the input transistors in the targeted frequencies, the proposed cell has higher bandwidth in comparison to the original circuit.

$$S_{p1,p2} = \frac{1}{2}\frac{\left(-r_{op}C_Pr_{on} - r_{op}C_Nr_{on} - RC_Nr_{on} - Rr_{op}C_P \pm \sqrt{r_{op}^2C_P^2r_{on}^2 + 2r_{op}^2C_Pr_{on}^2C_N - 2r_{op}C_Pr_{on}^2RC_N + 2r_{op}^2C_P^2r_{on}R + r_{op}^2C_N^2r_{on}^2} - \right.}{\left. Rr_{op}C_NC_Pr_{on}\right.}$$
$$\sqrt{2r_{op}^2C_Nr_{on}RC_P + 2r_{op}C_N^2r_{on}^2R + R^2C_N^2r_{on}^2 - 2R^2C_Nr_{on}r_{op}C_P + R^2r_{op}^2C_P^2} \quad (4)$$

The frequency response of TF of the proposed and original cells are shown in Figure 7. As demonstrated in this figure, the proposed amplifier has higher bandwidth, this simulation has been performed for C_N=6.8fF; other circuit specifications are set based on simulation data. The demonstrated plots in Figure 7 confirms the advantage of the bandwidth extension technique used in the proposed circuit.

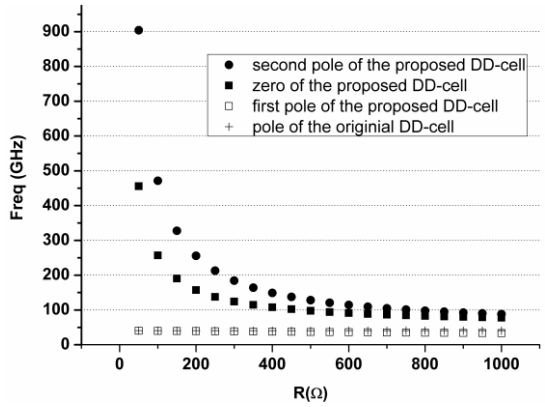


Figure 5: The poles and zero location for the proposed DD-cell

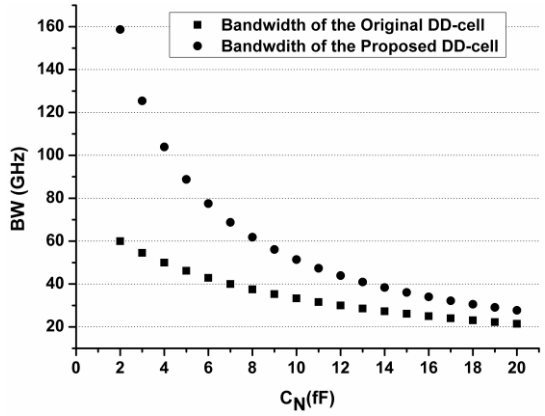


Figure 6: The comparison of the bandwidth for the original DD-cell and the proposed circuit for different values of the parasitic capacitor CN

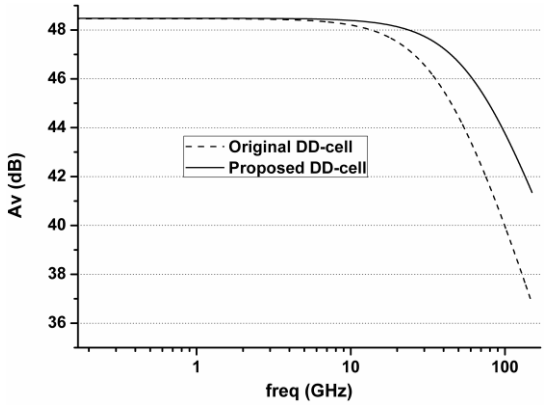


Figure 7: The comparison of the frequency response for TF of the circuit model of the proposed and original cells

As mentioned before, the value of R resistors that is chosen equal to 200Ω has the optimum bandwidth extension; here, this factor is further evaluated to confirm the selected value. The graphs in Figure 8 demonstrate the bandwidth improvement factor for different values of R resistor versus C_N parasitic capacitor ranging from 5-15 fF, which according to simulations are the most expected values for parasitic capacitance of the input NMOS transistors for targeted frequencies. As shown in this figure, the larger values of R resistor give a larger improvement for small values of C_N capacitors, however, this improvement decreases at higher C_N values. In order to have considerable improvement for bandwidth of the proposed DD-cell at wider range of values for the C_N capacitor and based on the results of the graphs in Figure 8, the value of R resistors in this paper is set to 200 Ω. The improvement obtained for the bandwidth in the actual circuit simulations is less than the predicted values in Figure 8. The results in Figure 8 are based on small signal model calculations; however, in the practical circuit, changing the value of R resistors also requires the necessary change in the value of C_N capacitors, which limits the improvement obtained for the bandwidth of the amplifier. For larger values of R resistors and to have the same bandwidth improvement, the equivalent resistor of the PMOS transistors should be reduced. This is not feasible because it will reduce the frequency span of the VCO.

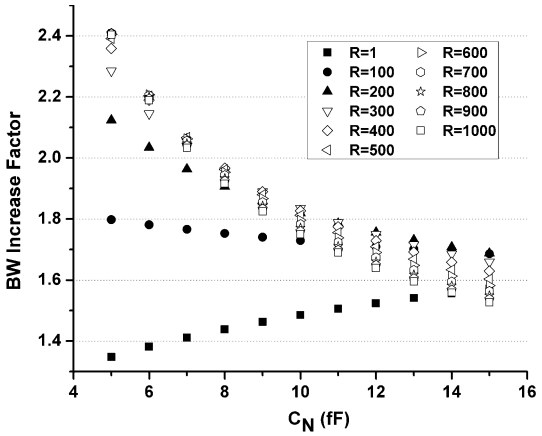


Figure 8: The bandwidth improvement factor for different values of R resistors versus expected range of values for the C_N parasitic capacitor

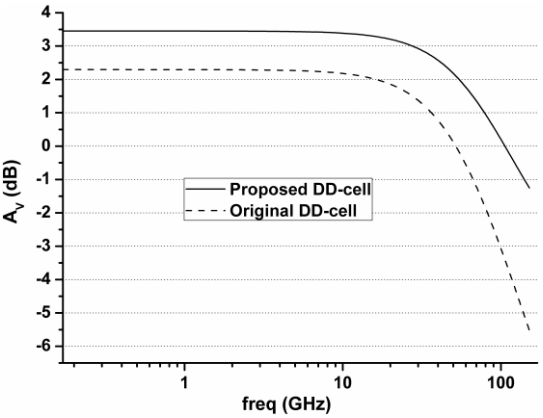


Figure 9: The simulated frequency response for the proposed DD-cell and the original circuit

In order to validate the improvement in bandwidth, which was explained above, two circuits in Figures 1 and 3 are designed and simulated in schematic level using the knowledge gathered from the analysis of the proposed circuit. The frequency response for these two circuits are demonstrated in Figure 9. The dashed line represents the result for the original circuit and the solid line stands for the proposed cell. These results in Figure 9 confirm the predicted improvement in the amplifier bandwidth. The bandwidth of

the circuit in Figure 1 is about 40 GHz while the proposed circuit has bandwidth of about 55 GHz. It should be mentioned that two circuits have been designed with the same power consumption and it also has the same gain value. But, the proposed circuit has higher bandwidth and slightly higher gain value for the same amount of power consumption.

III. The Ring-VCO

The structure of the designed ring-VCO is shown in Figure 2, which is constructed by using four DD-cells in a feedback loop. Assuming TF presented in (2) for each DD-cell, then the ring-VCO will have the TF as in (6):

$$H(s) = \frac{{A_0}^4}{\left(1 + \frac{S}{\omega_{P1}}\right)^4} \quad (6)$$

The minimum gain for oscillation of each DD-cell can easily be found that is equal to $A_0 = \sqrt{2}$ and the oscillation frequency regarding the required 45° phase shift for each DD-cell will be equal to $\omega_{osc} = \omega_{P1}$. Therefore, the free running frequency of the proposed VCO will be equal to ω_{P1} that is the 3dB bandwidth of each individual cell. Therefore, as explained in previous section, increasing this 3dB bandwidth using the proposed technique will increase the maximum oscillation frequency of the final VCO.

The proposed DD-cell can increase the maximum operating frequency of the VCO in comparison to the traditional one. On the other hand, for the same operating frequency as the VCO constructed using the traditional DD-cell, the proposed circuit can achieve low power consumption that is very critical in designs targeting the wireless portable applications.

IV. Simulation Results

The proposed ring-VCO and DD-cell are designed and simulated in CMOS 65nm process and compared with the ring-VCO designed using the traditional DD-cell. The simulations are performed for both the proposed and traditional ring-VCO to have a fair comparison. The device size and value used in the simulations are presented in Table 1. The results here are from post-layout simulations for both of the proposed and the traditional ring-VCO. The size of the input transistors (M1 and M2) in the proposed DD-cell and in the DD-cell of Figure 1 is set to 6µm to achieve maximum operation frequency. The DD-cell in Figure1 was optimized to achieve the maximum operating frequency, by choosing the minimum tuning voltage and smaller size for the load transistors. Then, maximum operating frequency of the proposed ring-VCO and the traditional one and the tuning ranges of them are evaluated.

The simulations result for this evaluation is shown in Figure 10. The results indicate that for the selected size of the input devices, the maximum operating frequency of the proposed ring-VCO is 15.45 GHz, which is about two times better than the original ring-VCO. The power consumption of the proposed ring-VCO at the oscillation frequency of 8GHz is about 3.7 mW, which is about 20% lower than the original ring-VCO, which further indicates its superior functionality. The locking range of the proposed ring-VCO as demonstrated in Figure 10 is about 88%, which is higher than the traditional ring-VCO with locking range of about 78%.

Table 1
The Summary of the Device Size and Value Used in the Simulations

Device Size	Traditional DD-Cell in Figure 1	Proposed DD-Cell in Figure 3
M1 & M2 (W/L) (µm)	(6/0.06)	(6/0.06)
MP (W/L) (µm)	(6/0.06)	(8/0.06)
Bias Transistor (W/L) (µm)	(32/0.06	(32/0.06)
R (Ω)	NA	200

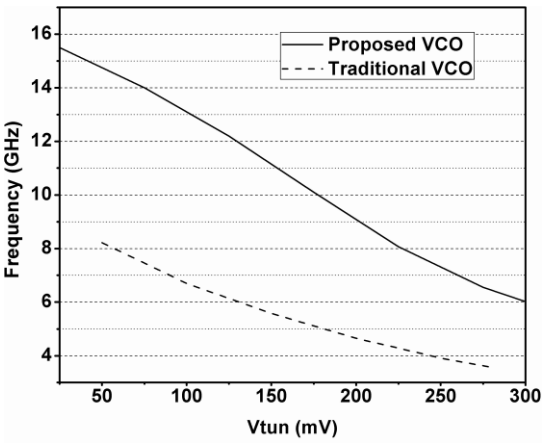


Figure 10: The tuning range of the proposed and traditional ring-VCO

The phase noise of the proposed ring-VCO at output frequency of 8GHz is shown in Figure 11, and it is compared to the traditional ring VCO. As shown in this figure, the proposed ring-VCO has better phase noise with less power consumption. At the offset frequency of about 1 MHz, the phase noise of the proposed ring-VCO is about 5dB less than the traditional one.

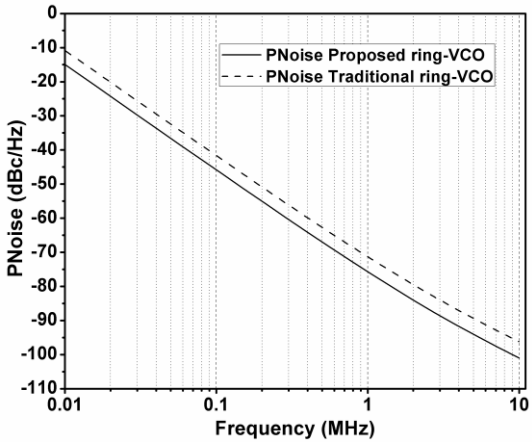
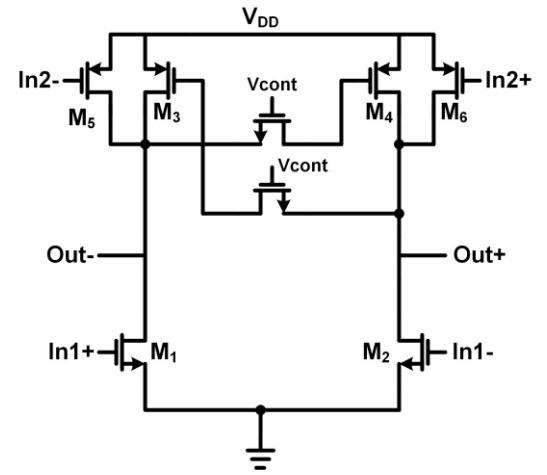


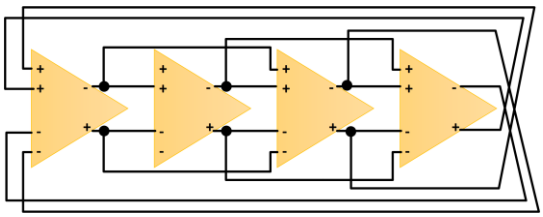
Figure 11: Phase noise of the proposed and traditional ring-VCO at output frequency of 8GHz

To demonstrate the phase noise performance of the proposed circuit in the targeted process technology, a Park-Kim ring-VCO [21] is also designed and simulated in the same process to be compared with the proposed circuit. The Park-Kim delay cell is shown in Figure 12(a) and the ring-VCO based on this cell is depicted in Figure 12(b). The result of this simulation and comparison is shown in Figure 13. The Park-Kim ring-VCO is running at output frequency of about 7.4 GHz and the results are from the schematic simulation,

whereas the prosed circuit output frequency is reduced down to 8GHz for this comparison and the results are from the post-layout simulation. As shown in this figure, the proposed circuit has better phase noise in comparison to the Park-Kim ring-VCO at the offset frequencies above 200 kHz that is the targeted bandwidth in most of the modern communication systems. The Park-Kim ring-VCO is one of the best performing VCOs regarding the highest operating frequency and the phase noise value.



(a)



(b)

Figure 12: (a) The delay cell introduced in [21], and (b) the low phase noise VCO based on this delay cell

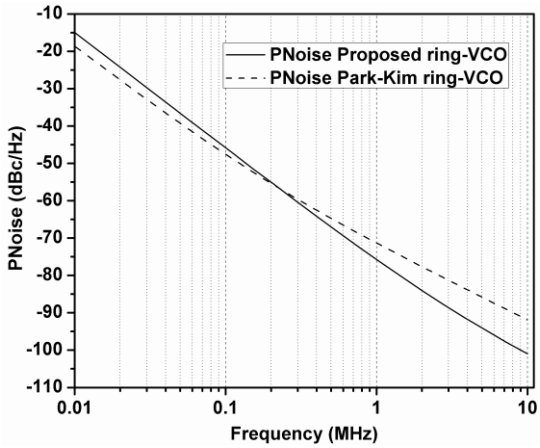


Figure 13: The comparison of the phase noise for the VCO in [21] and the one presented here

The layout of the proposed ring-VCO is shown in Figure 14; its area, including only the active core is about 115×95 μm^2. The summary of the post-layout simulations for the proposed ring- VCO is shown in Table 2, and it is compared with some of the recently reported works [10][11][14] from the literatures. The FOM in (7) is used to compare these designs. In this equation, $PN(f_{off})$ is the phase noise at the offset frequency of f_{off}, f_0 is the oscillation frequency and P_{VCO} denotes the power consumption of the VCO.

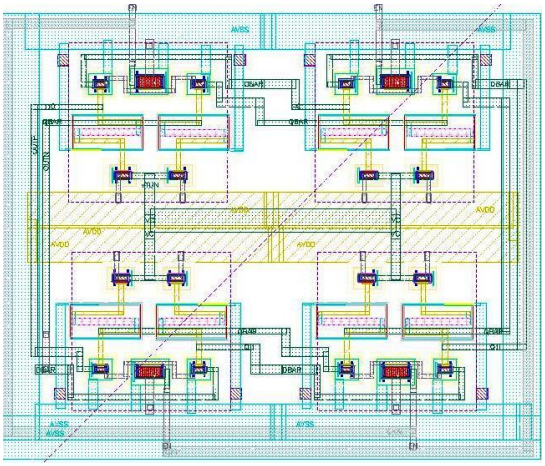


Figure 14: The layout of the proposed ring-VCO

$$FOM = 20\log\left(\frac{f_0}{f_{off}}\right) - 10\log\left(\frac{P_{VCO}}{1\ mW}\right) - PN(f_{off}) \qquad (7)$$

The proposed ring-VCO has lower FOM in comparison to [10] and [14], which is due to its higher phase noise value. The proposed ring- VCO here is aiming at higher operating frequencies, while having the same power consumption and the phase noise. The presented design here with high output oscillation frequency has lower power consumption and phase noise in comparison to the traditional circuit and the Park-Kim ring-VCO that are designed and simulated here in the same process and conditions.

The higher phase noise value for the proposed circuit in comparison to [10] and [14] that is presented in Table 2 is dominated by the process technology limitation, which then has reduced the FOM value for the proposed ring-VCO as compared to the design in literatures. However, the FOM value is much better in comparison to the traditional and Park-Kim [21] ring-VCO.

V. CONCLUSIONS

In this paper, a high frequency ring-VCO was introduced, which is based on an improved DD-cell. The proposed DD-cell has larger frequency bandwidth and higher gain value while consuming the same power in comparison to the traditional DD-cell. The traditional and the proposed ring-VCO have been designed and simulated in CMOS 65nm process. The simulation results show that the proposed VCO has about two-fold higher maximum operational frequency in comparison to the original VCO and has 20% less power consumption when both VCO's are operating at the same output frequency of about 8 GHz. The proposed VCO has 10% higher tuning range in comparison to the original VCO. In order to evaluate the phase noise performance of the proposed VCO, its phase noise was compared with the Park-Kim VCO [21] that is also designed here in the same process. The Park-Kim VCO is one of the state-of-art designs concerning the phase noise performance of the VCO. The proposed VCO has about 5dB better phase noise at offset frequency of 1MHz with respect to the 8GHz output carrier.

Table 2
The Comparison of the Proposed VCO with Other Designs from the Literatures

	[10][a]	[11][b]	[14][a]	Park-Kim VCO [21][c]	Traditional-VCO[d]	Proposed-VCO[d]
Technology (nm)	65	65	65	65	65	65
Supply (V)	0.6	0.7	1	1	1	1
Power (mW)	0.45	0.36	10	4.59-5.82	2.72-4.54	2.95 – 4.38
Maximum Frequency (GHz)	0.49	0.909	0.645	7.4	8.22	15.5
Tuning Range (%)	24	42	70	130	78	88
Phase Noise @ 1MHz offset frequency (dBc/Hz)	-94.84	-90	-110	-71.78	-71.9	-76.3
FoM (dBc/Hz)	162.1	153.6	156	141.5	143.6	153.7

Note: [a]measurement, [b]simulation (schematic), [c]redesigned and simulated here, [d]simulation (post-layout)

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