RF Performance Enhancement of Gallium Oxide MOSFET using p-type NiO Pocket near Source and Drain Regions

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***Abstract*— The paper puts forward an impact of using p-type NiO pocket near the channel/drain and channel/source interface regions on the RF performance of the gallium oxide MOSFET. This arrangement results in smaller electric field near the respective junctions and helps to compensate for the leakages that arises from the increased value of parasitic components. The key figures of merits used in the analysis are transconductance (g_m), intrinsic capacitances (gate to drain capacitance C_{gd} and gate to source capacitance C_{gs}), output conductance (g_d), cut-off frequency (f_T), transconductance frequency product (TFP), gain frequency product (GFP) and the gain transconductance frequency product (GTFP). The analysis was carried out by using Atlas 2D device simulator.**

Index Terms— Gallium Oxide MOSFET; Leakage Currents; RF Figure of Merits; RFICs; Wide Band Gap Semiconductors.

I. INTRODUCTION

The increasing demand for high power RF applications leads to the need for semiconductor technology to have low losses associated with them [1]. Known as the silicon technology (which is the widely used semiconductor technology), it has reached its theoretical limit for such applications due to its narrow band gap (~ 1.1 eV). In high power RF applications based on silicon technology, it is observed that as the die size increases (to decrease the specific on resistance for low power losses), the input capacitance also increases and results in increased switching losses and offsets the reduction in the conduction losses, which is achieved by decreased value of specific on resistance [2]. Henceforth, to overcome these limitations wide band gap (WBG), semiconductor technology is reported by the various researchers [3] and even several devices based on WBG semiconductor technology has already been proposed [4]-[7] out of which gallium oxide (Ga_2O_3) MOS technology is mostly preferred due to its several advantages like high breakdown voltage, low power losses, low leakages and most important it indicates a path for the efficient integration of monolithic and heterogeneous devices in high power switching applications [8].

For RF applications, several researches already have been proposed. *K. P. Pradhan et al.* discussed the impact of high-k gate dielectrics on analog and RF performance of the nanoscale MOSFET and concluded that gate stacking using silicon nitride as high-k dielectric material exhibit better performance in comparison to the other dielectric materials, and hence suitable for the design of analog and RF circuits. [9] *N. Mohan Kumar et al.* reported the influence of channel and gate engineering on the analog and RF performance of MOSFETs, in which the gain of the device increases with the use of halo channel doping and by using dual metal (molybdenum and aluminum) interconnects for gate terminal [10]. *Angsuman Sarkar et al.* put forward the effect of gate engineering in double-gate MOSFETs on its analog and RF performance. The use of triple metal gate results in the shifting of peak horizontal electric field toward the source side, which improves the carrier transport efficiency, and hence improves the RF performance of the device [11]. *Yadava and Chauhan* put forward that the introduction of thin layer of graphene or black phosphorous results in improved large signal RF performance of the gallium oxide MOSFET [4]. *Green et al.* studied that the RF performance of gallium oxide MOSFET with recessed gate structure and found that its performance can be further improved by using highly doped ohmic cap layers [5].

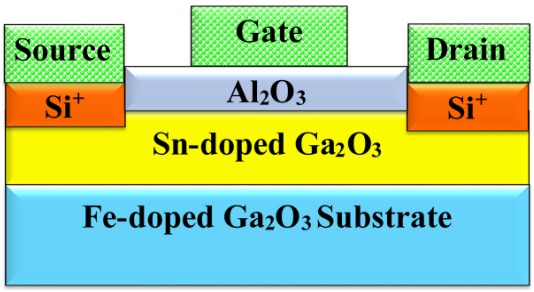
In high power electronics applications, the current driving capability of the devices is required to be high, and for this purpose p-type type conductivity is required [12]. However, in gallium oxide semiconductor technology p-type conductivity is almost negligible and it is due to the inherent behavior of oxides that forms donor type oxygen. Further, if dopant atom is added, it leads to the introduction of deep accepter levels with ionization energies larger than 1 eV, which exacerbates the p-type conductivity even more [13]. Therefore, to achieve p-type conductivity in Ga_2O_3, heterostructure of p-type oxide-based semiconductors are used (Ir_2O_3, NiO_x) with the disadvantage of lattice and band structure mismatch [14]. *Kokuban et al.* fabricated the NiO/Ga_2O_3 heterojunction diode, in which the p-type NiO layer was made to grow on Ga_2O_3 substrate. The oxide based fabricated device shows good rectifying characteristics with the ratio greater than 1×10^8 at ± 3 V [15]. The first normally-off MOSFET with p-type Ir_2O_3 channel region is reported by FLOSFIA Inc. [16], which is considered to be ground breaking work to pave the need for future power devices. However, the technology is still in the developing stage.

This paper, henceforth, investigates the performance of proposed p-type NiO pocket-based gallium oxide MOSFET. The key figures of merits used in the analysis are transconductance (g_m), intrinsic capacitances (gate to drain capacitance C_{gd} and gate to source capacitance C_{gs}), output

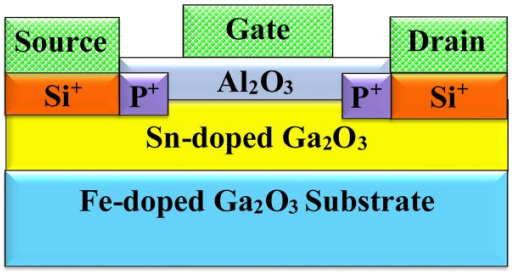
conductance (g_d), cut-off frequency (f_T), transconductance frequency product (TFP), gain frequency product (GFP) and the gain transconductance frequency product (GTFP).

II. DEVICE DESCRIPTION

The structure of the conventional and the designed p-type NiO pocket-based gallium oxide MOSFETs is shown in Figure 1(a) and Figure 1(b) respectively. The use of p-type NiO pocket near the channel/drain and channel/source interface regions leads to minute increase in the potential at the respective interfaces of the designed MOSFET compared to the conventional gallium oxide MOSFET. It is due to the abrupt change in doping profile of the channel/drain and channel/source interface regions. This arrangement results in smaller electric field near the respective junctions and helps to compensate for the leakages that arise from the increased value of parasitic components. The channel of the device is a uniformly doped (7×10^{17} cm^{-3}) 0.3 µm thick n-type region grown over a semi-insulating single crystal Ga_2O_3 substrate. A p-type NiO (1.61×10^{17} cm^{-3}) pocket regions with optimum length of 10 nm are used on both sides of the channel. The multiple Si^+ implantation is used to define source and drain electrode regions of 150 nm shallow box profile. These regions are n-type uniformly doped regions (3×10^{19} cm^{-3}). The source and drain regions are 20 µm apart from each other over which a gate dielectric insulator Al_2O_3 was made to grow followed by deposition of Ti/Pt/Au metal gate of 2 µm in length on the top.



(a)



(b)

Figure 1 (a) Conventional gallium oxide MOSFET and (b) NiO pocked based gallium oxide MOSFET.

III. RESULTS AND DISCUSSIONS

The important figures of merit used to investigate the RF of the device are transition frequency or cutoff frequency (f_T), transconductance frequency product (TFP), gain frequency product (GFP), gain transconductance frequency product (GTFP) and the intrinsic capacitances (gate to drain capacitance C_{gd} and gate to source capacitance C_{gs}), which are obtained by AC small signal analysis after performing the DC analyses. The analysis is carried out by using Atlas 2D device simulator [17]. The transfer characteristics of the devices are shown in Figure 2, in which the use of p-type NiO pocket near the channel/drain and channel/source interface regions results in lower rate of increase in the drain current in comparison to the conventional gallium oxide MOSFET as the gate to source voltage increases. The lower rate of increase in the value of the drain current is due to the increased carrier to carrier scattering in the channel region. The On/Off current ratio is of the order of ~ 10^{10} with steeper subthreshold slope. It implies that the design device has fast switching speed with low leakage current i.e. in the range of pico-Amperes. Figure 3 represents the output characteristics of the devices and it is observed that for p-type NiO pocket-based gallium oxide (NiO-GO) MOSFET, the value of drain current is lower and is due to the afore stated phenomenon.

The intrinsic capacitances are obtained by performing AC analysis at the frequency of 1 MHz at gate to source DC voltage swept from 0 V to 1.5 V. From Figure 4, it is observed that the value of C_{gs} is smaller for NiO-GO MOSFET in comparison to the conventional (Conv.-GO) MOSFET. The capacitive coupling between the drain and the gate electrode regions opposes the decreasing of C_{gd} in the NiO-GO MOSFET and due to which its value is comparable to the Conv.-GO MOSFET. Since a p-i-n diode is formed near the drain region, the leakage current associated with device has direct correlation with these intrinsic capacitances. For a larger value of drain to gate voltage, there is significant amount of charges generated in the channel region and results in increased leakage current associated with the device. The rate of the generation of these charges is directly proportional to the electric field in the channel region and it increases with the increase in the field.

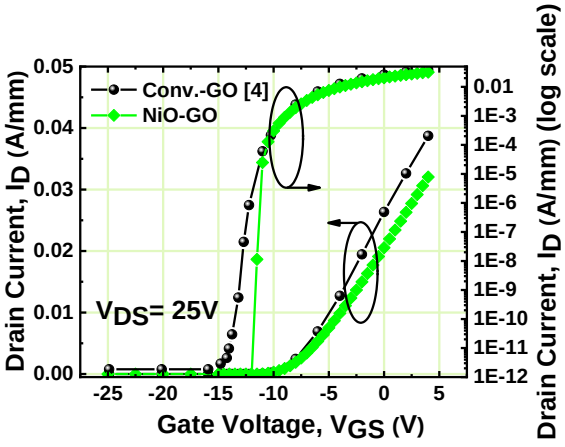


Figure 2 Drain current versus gate to source voltage.

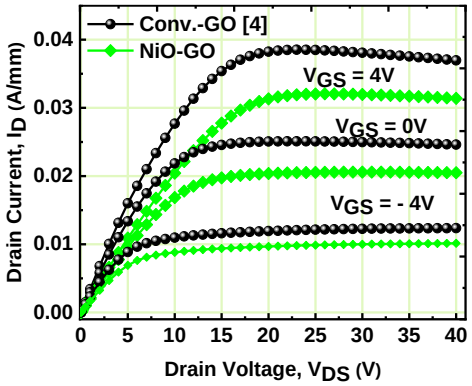


Figure 3 Drain current versus drain to source voltage.

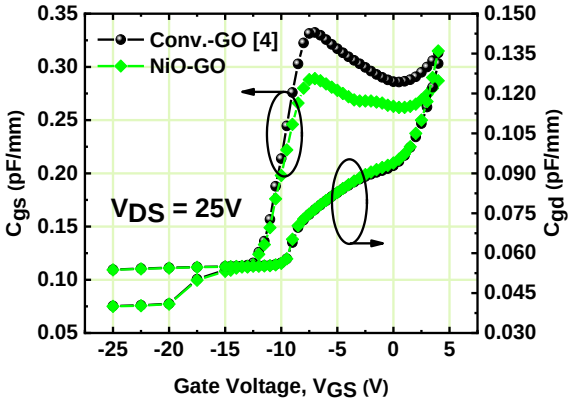


Figure 4 Intrinsic capacitances versus gate to source voltage.

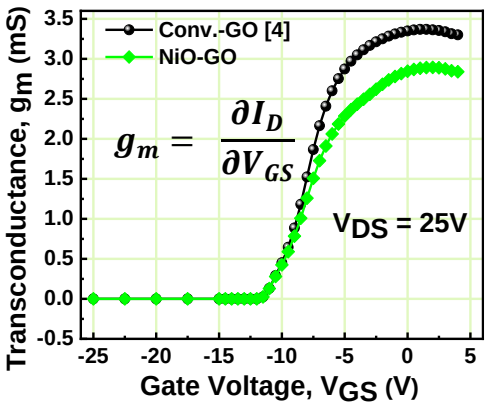


Figure 5 Transconductance versus gate to source voltage.

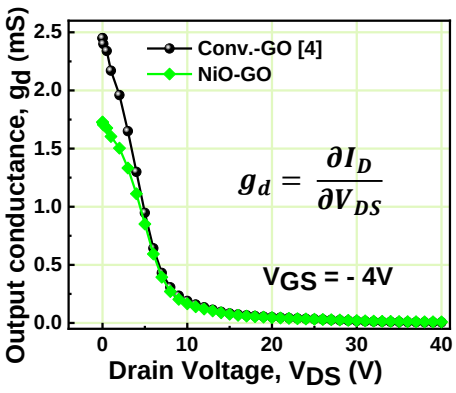


Figure 6 Outputconductance versus drain to source voltage.

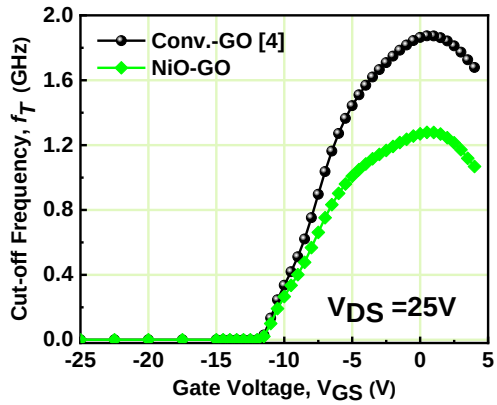


Figure 7 Cut-off frequency versus. gate to source voltage.

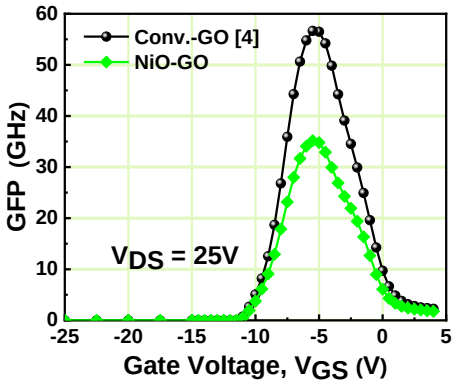


Figure 8 GFP versus gate to source voltage.

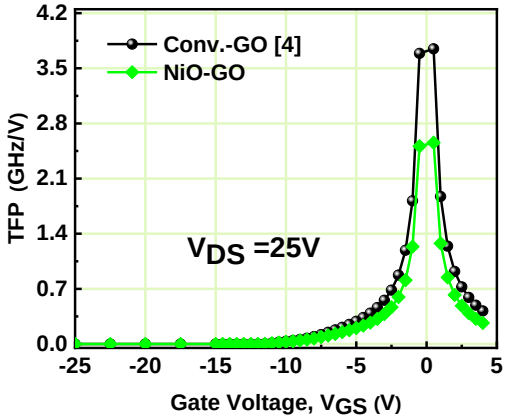


Figure 9 TFP versus gate to source voltage.

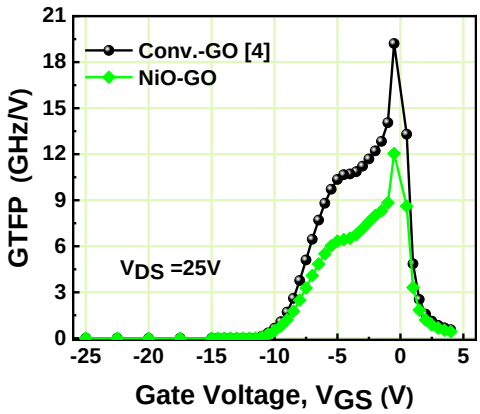


Figure 10 TFP versus gate to source voltage.

The transconductance (g_m) is the important RF parameter and is used to determine the gain of the amplifier. In Figure 5, the plot of g_m with respect to gate to source voltage is shown. The value of g_m, which is formulated in eq. (1) decreases with the use of p-type NiO pocket in the device. The increased carrier-to-carrier scattering near the channel interfaces results in a decreased value of I_D , which results in a decreased g_m. In analog applications to achieve high output gain, lower output conductance (g_d) is needed (see eq. (2)). Figure 6 represents the characteristic of g_d versus drain to source voltage at V_{GS} equal to - 4 V. Lower value of g_d is obtained for NiO-GO MOSFET in comparison to the Conv.-GO and indicates that the device is suitable for high gain applications. The components, which results in high g_d includes channel length modulation and DIBL, and the uses of p-type NiO pocket in the device shows good control over these adverse effects owing to low g_d.

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \quad (1)$$

$$g_d = \frac{\partial I_D}{\partial V_{DS}} \quad (2)$$

$$f_T \approx \frac{g_m}{2\pi(C_{gs}+C_{gd})} \quad (3)$$

The transition frequency or cut-off frequency f_T is known to be the important figure of merit (FOM) for RF performance evaluation. It is the frequency point, which marks the transition of the frequency from the amplification to the attenuation. The approximate value of f_T is formulated using eq. (3). In order to obtain more accurate value of f_T, the AC analysis over a wide range of frequency is performed using 2D device simulator. Then, an advanced RF parameter extraction tool (using two-port network) is used with applied frequency (f_0) (see eq. (4)). From Figure 7, it is observed that for NiO-GO MOSFET, the value of f_T is lower. This condition is due to the decreased value of g_m.

$$f_T = f_0 \cdot |H_{21}| \quad (4)$$

$$TFP = \left(\frac{g_m}{I_D}\right) \times f_T \quad (5)$$

$$GFP = \left(\frac{g_m}{g_d}\right) \times f_T \quad (6)$$

$$GTFP = \left(\frac{g_m}{g_d}\right) \times \left(\frac{g_m}{I_D}\right) \times f_T = A_V \times TFP \quad (7)$$

In Figure 8 and Figure 9, the variation of TFP and GFP versus gate to source voltage are shown and can be formulated by using eq. (5) and eq. (6) respectively. In designing moderate to high speed RF circuits, it is necessary to find the tradeoff between power and bandwidth, and this can be obtained by utilizing TFP. The GFP is known to be the important FOM for RF applications, especially for RF amplifiers. In Figure 8 and Figure 9, it is observed that the increased value of both TFP and GFP is smaller when p-type NiO pocket is used in the device. This condition is due to the decreased value of g_m. The gain transconductance frequency product (GTFP), shown in Figure 10 is another important RF FOM. It is utilized to find the tradeoff between switching speed, transconductance and intrinsic gain. The higher the GTFP, the higher will be the gain and the lower will be the speed of operation and vice versa (see eq. (7)). The highest value of GTFP is achieved at the V_{GS} = - 0.5 V for all the designed devices.

Table 1
Comparison of key RF foms

MOSFET	C_{gs} (pF)	C_{gd} (pF)	f_T (GHz)	GFP (GHz)	TFP (GHz/V)	GTFP (GHz/V)
Conv.-GO [4]	0.33	0.13	1.87	56.4	3.6	19.2
NiO-GO (This work)	0.29	0.13	1.27	35	2.5	12.0

Table I represents the comparison of the maximum value of some key RF FOMs of the designed device compared with the conventional device [4]. The value of C_{gs} is 0.87 times lower due to the use of p-type NiO pocket region, while the value of C_{gd} is almost equal to that of the Conv.-GO MOSFET, and this is due to the capacitive coupling between drain and gate electrodes. In NiO-GO MOSFET, the f_T is 0.68 times, while the GTFP is 0.63 times smaller than the Conv.-GO MOSFET. The GFP is 0.62 times and the TFP is 0.69 times inferior than the Conv.-GO MOSFET. The above results indicate that the proposed NiO-GO MOSFET shows better RF performance with low leakages.

IV. CONCLUSION

The p-type NiO pocket near the channel/drain and channel/source interface regions are used to reduce the leakages associated with the device. The value of C_{gs} is 0.87 times lower due to the use of p-type NiO pocket region, while the value of C_{gd} is almost equal to that of the Conv.-GO MOSFET. This condition is due to the capacitive coupling between drain and gate electrodes. In NiO-GO MOSFET, the f_T is 0.68 times, while GTFP is 0.63 times smaller than the Conv.-GO MOSFET. The GFP is 0.62 times and the TFP is 0.69 times inferior than the Conv.-GO MOSFET. The above results indicate that the proposed NiO-GO MOSFET shows better RF performance with low leakages, and it can be further improved by developing the technology, which can introduce p-type conductivity in the gallium oxide semiconductors.

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