Low Phase Noise Wide Tuning Range LC Oscillator for RF Application using Varactor Bank

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***Abstract*— This paper presents the design of a QVCO (Quadrature voltage controlled oscillator) with high tuning range and low phase noise for Radio Frequency applications. The proposed VCO has been designed to produce quadrature signal by using cross coupled topology. Extra pair of MOSFETS are added to improve the quality factor of the LC tank, which helps to improve the phase noise. The tuning range of VCO ranges from 3.8 GHz to 4.52 GHz, which is nearly 20%. Additionally, the obtained phase noise is -120.31 dBc/Hz at 1MHz offset frequency. The observed power dissipation is 13.21 mW.**

***Index Terms*— Dual Pair Cross Coupled; Phase Noise; Power dissipation; Quadrature LC VCO; Tuning Range.**

I. INTRODUCTION

Oscillator is now becoming the basic requirement for almost every electronic system today, and this leads to the need for the production of periodic output signal. The various uses of the VCOs such as, in clock generators frequency synchronizers and in the communication systems have resulted in the requirements for tuning the frequency. Furthermore, tuning range and phase noise play a vital role when tuning the frequency is required during high radio frequency in the field of wireless communication. Thus, it is necessary to keep the tuning range as high as possible at low phase noise. In this paper, the proposed a design of the LC VCO for RF applications. Since LC VCO provides low phase noise, it is equally difficult to achieve better tuning range with LC VCO. Considering the existence of tradeoff between phase noise and tuning range, it is a challenge to maintain both of them accordingly. Although the ring oscillator for better tuning range is preferred, the ring oscillator degrades the phase noise. Since we are interested in low phase noise, the LC VCO is a better option compared with the ring VCO. In this context Taking into consideration the tradeoff between phase noise and tuning range, we posit that the use of the cross coupled CMOS topology with biasing of PMOS in LC VCO improves the phase noise [1]. In the proposed design, we adopted the varactor bank to achieve the tuning range of 20%, although the usage of the varactor bank caused some parasitic to the circuit.

II. QUADRATURE CIRCUIT

In low or zero-IF transceivers, the quadrature signal is required for modulation and demodulation. It is required to generate the quadrature signal with minimum phase noise. This can be achieved by the quadrature LC VCO. Further, the quadrature VCO can be designed either by using ring topology or LC tank topology. Generally, oscillators designed by using ring topology, have good tuning range but lower phase noise. Similarly, the VCOs designed by using LC tank topology has good phase noise but suffers from low tuning range. There is a demand for low phase noise in RFIC, therefore LC topology is used in the proposed design [2].

A. Quadrature Signal Generation

Various literatures provided explanation on the generation of the quadrature signal. It has been documented that the use of the RC-CR network as a delay element [3,4] can generate the signal; however, it has a drawback of requiring much power for its buffers. The phase error is also high for these networks. Ring oscillator can also be used for the generation of quadrature signal; however, as discussed earlier, it suffers from bad phase noise [5].

Another method to generate quadrature signal is by cross coupling two different dual band LC VCO in a manner such that they produce quadrature signals that have equal phase difference in between them. The dual band LC VCO generates two signals across the different ends of the inductor. Hence, cross coupling of two dual band LC VCO generates quadrature signal. The quadrature VCO has better phase noise than the single band as well as dual band VCO. As such, they are used for low power [6] and low phase noise applications.

B. Quadrature Topology

The oscillator with negative Transconductance can produce different signal at the outputs. To produce differential signal, we placed CMOS parallel to each other and then cross coupled them since the negative resistance occurs at the drains of the CMOSs [7]. In the proposed LC oscillator (figure 1), the respective components used in both pairs of LC oscillator are identical; therefore, the differential signal produces at the end of both inductors will have the same frequency of oscillation with different phases only.

III. PROPOSED CIRCUIT

The proposed design adopted similar method to generate the quadrature signal by connecting two different dual band LC VCO in a cross coupled manner. The proposed design is shown in Figure 1. The circuit has two dual band LC VCO circuit, cross coupled to each other. The first pair (p1, p2) was to produce negative resistance, which minimizes the losses of the oscillations and the other pair (p3, p4) was cross coupled to improve the quality factor Q of the LC tank circuit and to minimize the parasitic losses introduced in the circuit. Both the CMOS pairs are connected parallel to each other, which effectively increases the capacitance introduced by MOS, which decreases the quality factor of the capacitance. This

improves the phase noise. In pull down network, pairs of NMOS are cross coupled and connected across the inductor, which helps to maintain smooth sinusoidal oscillation. Figure 1 shows the proposed design of quadrature LC VCO without varactor bank.

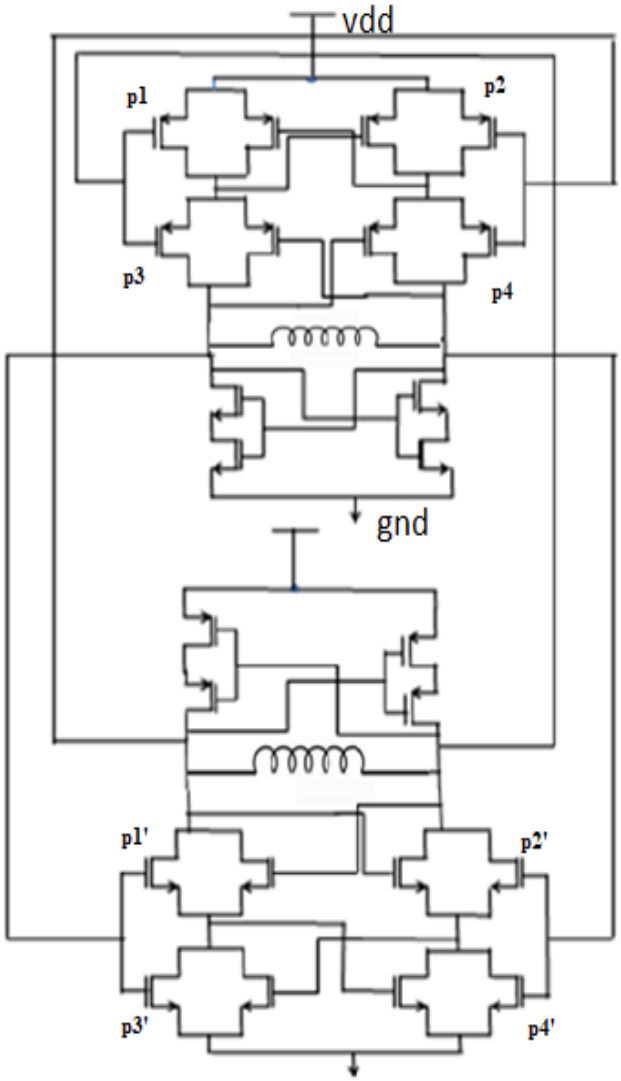

Figure 1: Dual Pair Cross Coupled VCO.

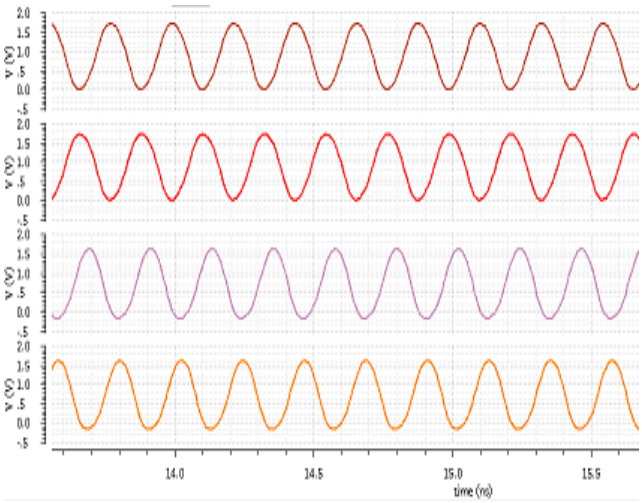

Figure 2: Generation of Quadrature Signal.

As we can see from Figure 2, oscillation will occur at both ends of the inductor. The signal at the first end will be in the anti-phase with the signal at the other end. Therefore, a total of four signals will present across both inductors. Hence, quadrature signal generation takes place, as shown in Figure 2.

IV. VARACTOR BANK

A varactor bank is basically a variable capacitor whose value depends upon applied tuning voltage. The capacitance vs area ratio for the MOS type varactor is much higher than the PN varactor. Therefore, it provides better tuning range [8]. Additionally, MOS varactor can be scaled as per existing technology.

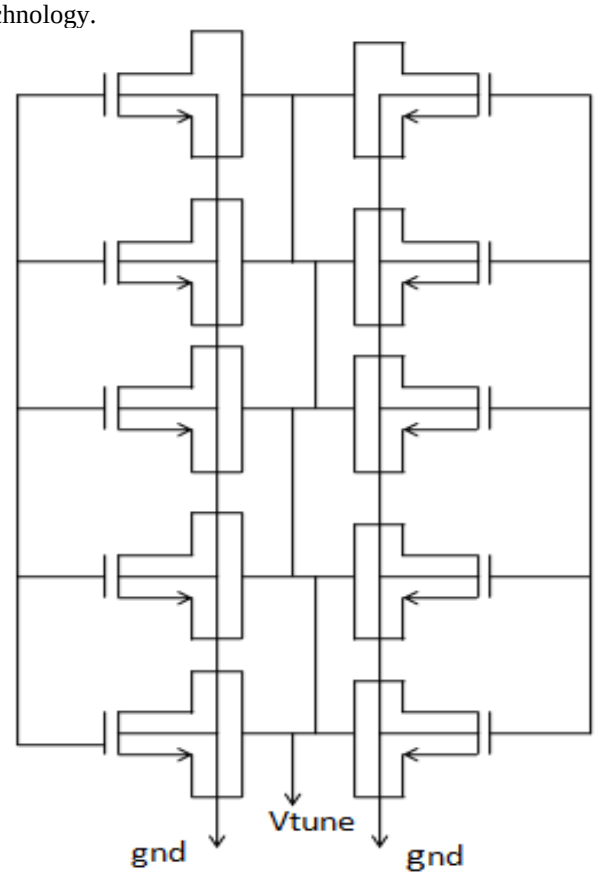

Figure 3: Varactor Bank.

Figure 3 shows the varactor bank, which is a variable capacitor designed from MOS. When we apply the tunable voltage across the varactor bank, its capacitance changes according to the tuning of the applied voltage. The varactor bank can be designed by NMOS as well as PMOS. According to the applied voltage, it can operate in various modes like accumulation, depletion or inversion. Bodies of the MOSFETs are either grounded or connected to the vdd depending on NMOS or PMOS, whatever used for the designing. In deep submicron, a diode varactor provides the low capacitance ratio, which is shown by the MOS varactor. Therefore, it is used as the variable capacitor in LC VCO. The designing of the MOS varactor is done by connecting the source terminal of the MOS with the drain terminal, as shown in Figure 3. In the case of NMOS varactor, the body is grounded while other terminals are connected to the vdd. Similarly, in the case of the PMOS varactor, all of the terminals are connected to the vdd. Here, the shown MOS

varactor is designed by NMOS. The inductor L along with varactor produces approximate oscillation of frequency, f_o as shown below [9]:

$$fo = \frac{1}{2\pi\sqrt{L\,(Cv + C)}} \quad (1)$$

where: fo = oscillation frequency
L = inductor
C = capacitor
C_v = varactor capacitance

V. DESIGN CONSTRAINT

The proposed design aims to minimize the phase noise by keeping the tuning range as good as possible. Some other parameters, such as power dissipation, tuning range and area, are also taken into account.

In non-ideal condition, there are always some losses occur. In Figure 4, let the losses are denoted through R [10].

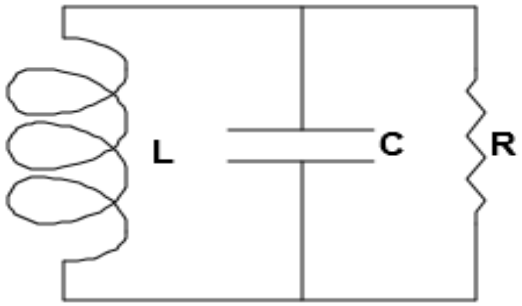

Figure 4: Tank Circuit with losses R.

This parasitic resistance, R provides losses in the circuit. These losses degrade the performance of the oscillator. Hence, to minimize these losses, we need to cancel out this R by taking it in parallel with another R of the same value, but negative in nature. This is called negative resistance, which will cancel out the circuit losses and sustain the oscillation in the circuit. Figure 5 shows the negative resistance, which is in parallel with R [11]:

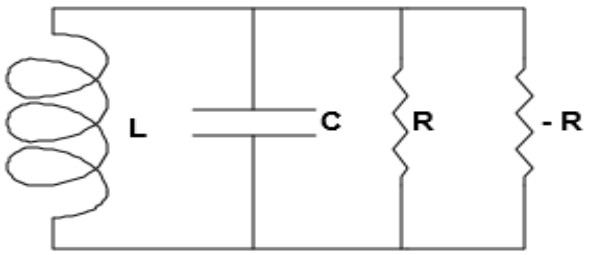

Figure 5: Negative Resistance Parallel to R.

This negative resistance (-R), is produced on the drain of the cross coupled (differential pair) MOS, connected in parallel with the LC tank. The occurrence of the negative resistance is given as -2/Gm, which can be seen in Figure 6.

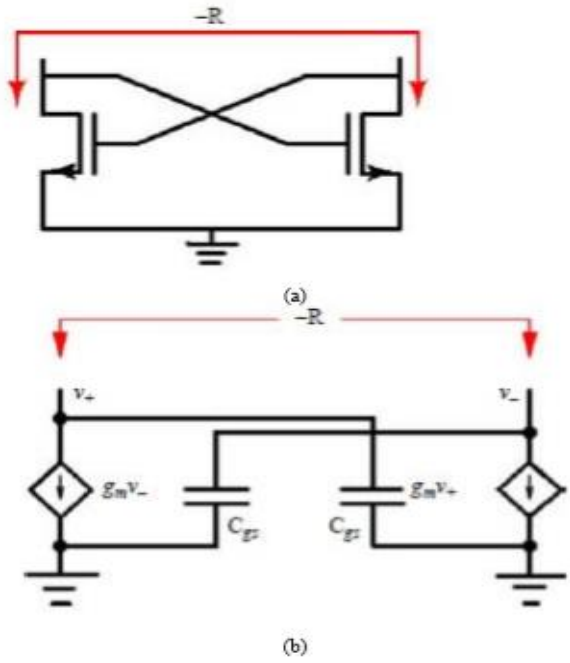

Figure 6: Generation of the Negative R.

Figure 6 shows the cross coupling of MOS transistors, which is responsible for the generation of the negative resistance. Whereas, Figure 6(b) is the small signal equivalent of the Figure 6(a). Therefore, the negative resistance can be given as [12]:

$$R = V/I = \left(V_{gs_2} - V_{gs_1}\right)/(-gmV_{gs_2} = -2/gm\,) \quad (2)$$

where: R = negative resistance
V = voltage
I = drain current
Vgs_1 , Vgs_2 = gate to source at both ends

The quality factor also affects the phase noise of the circuit. Let the equivalent quality factor of the circuit is Q, given as:

$$1/Q = 1/Q_c + 1/Q_L \quad (3)$$

where: Q = quality factor of the tank circuit.
Q_c = quality factor of the capacitor.
Q_L= quality factor of the inductor.

As the Qc is much larger, 1/Qc almost tends to zero. Therefore, we can consider QL only. The QL is given as:

$$Q_L = \omega L/R \quad (4)$$

where: Q_L= quality factor of the inductor.
R = series resistance of inductor.
ω = oscillation frequency.
L = inductance value.

To understand the working of the differential cross coupled pair of NMOS, we need to understand the basics of the NMOS[16]. When NMOS pair is in the saturation region, the drain current is given as:

$$Ids = \frac{\mu nC_{ox}}{2}\left(\frac{w}{l}\right)\left(V_{g_s - Vt}\right) \quad (5)$$

where: Ids = drain to source current.
μ_n = mobility of the charge carriers.
C_{ox} = gate oxide.
w = depletion width.
l = depletion region length.
V_{gs} = gate to source voltage.
V_t = threshold voltage.

From the low frequency model of MOSFET, we can calculate the Transconductance gm, which is given as [16]:

$$Gm = \frac{\partial Ids}{\partial Vgs}\left(\frac{w}{l}\right)(Vgs - Vt)\mu nCox \quad (6)$$

where: G_m = Transconductance.
All other parameter has been explained earlier.

The proposed topology contains NMOS as well as PMOS cross coupled pairs. The current flowing from both is also equal. Therefore, the negative resistance of the circuit is given as:

$$R = -\frac{2}{\text{Gmn} + \text{Gmp}} \quad (7)$$

where: R = negative resistance.
Gmn = Transconductance of NMOS.
Gmp = Transconductance of PMOS.

The tuning range of the VCO is the range of the frequency in which VCO can be tuned. This can be done by changing the capacitance value of the tank circuit. The capacitance value of the tank circuit is varied with the applied tuning voltage. let ωo be the centre frequency given by ωo= 1/√LC hence tuning range is given by:

$$TR = (\omega_{max} - \omega_{min})/\omega_o \quad (8)$$

where: TR = tuning range.
ω_{max} = maximum frequency of oscillation.
ω_{min} = minimum frequency of oscillation.
ω_o = frequency of the oscillation.

Now the phase noise is determined through the leeson's formula as:

$$L\{\Delta\omega\} = 10log\left[\frac{2FKT}{Psig}\{1 + \left(\frac{\omega o}{2Q\Delta\omega}\right)^2\}\left(1 + \frac{\Delta\omega_{\frac{1}{f^3}}}{|\Delta\omega|}\right)\right] \quad (9)$$

where: $L\{\Delta\omega\}$ = phase noise
F = empirical factor
K = boltzmann constant
T = temperature in kelvin
P_{sig} = power dissipation
ω_o = center oscillation frequency
$\Delta\omega$ = offset frequency
Q = quality factor of the tank circuit
$\Delta\omega_{\frac{1}{f^3}}$ = flicker or corner frequency

If we calculate phase noise from Leeson's equation, then it comes around -125dBc/Hz, which is little more than the simulated result (-120dBc/Hz).

Figure 7 shows the complete proposed circuit of the Quadrature LC circuit, which has dual pair or cross coupled MOS which effectively decreases the parasitic introduced by MOS itself.

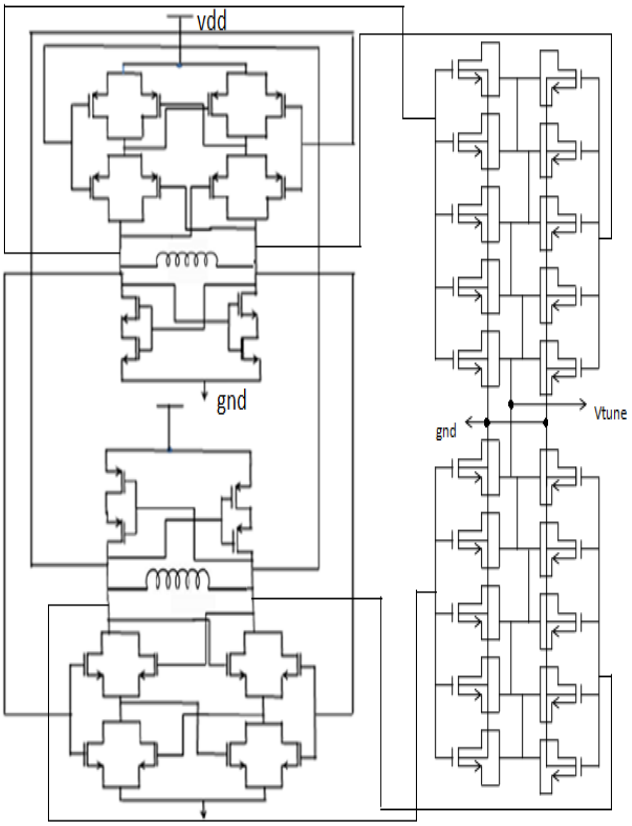

Figure 7: Proposed Circuit Design of the Dual Pair Cross Coupled LC VCO.

The Varactor bank designed by NMOS works as a variable capacitor, which is connected in parallel with the inductor. There are two dual band LC Oscillators, as shown in the circuit diagram. They are cross coupled to each other to produce Quadrature signal. Two pairs of the varactor bank are connected to each of the dual band oscillators. Both varactor pair share the common tuning voltage. By changing this tuning voltage, the varactor capacitance changes.

VI. SIMULATION CURVE AND TABLES

All curves shown in Figure 8 to Figure 10 are simulated using 180nm gpdk technology. Figure 8 shows the curve of the tunable range of the frequency. When applied tuning voltage is tuned from 0 to 1.8V, the frequency changes from 3.8GHz to 4.52GHz, which is nearly 20%.

Figure 9 shows the phase noise curve. The observed phase noise at 1MHz that offsets the frequency comes out to be -120dBc/Hz. The mathematical equation for the phase noise is given in equation 9, which is known as the leeson's equation.

The simulation curve in Figure 10 shows the power dissipation of the proposed circuit. The power has been calculated using the equation shown below:

$$P_{diss} = V.I_{DS} \quad (10)$$

where: $P_{diss.}$ = power dissipation
V = supply voltage
I_{DS} = drain to source current

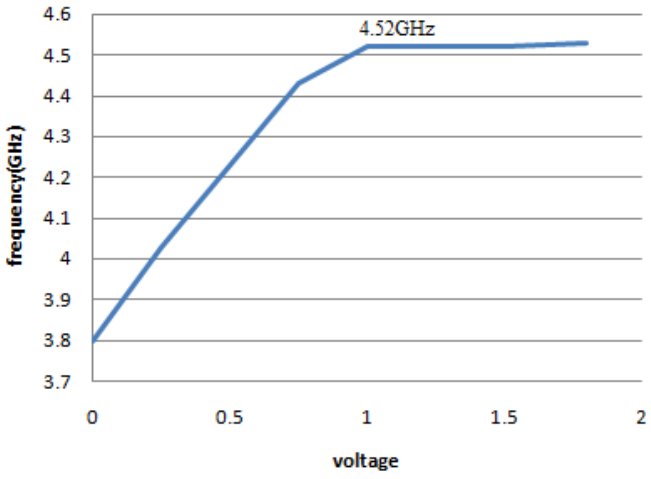

Figure 8: Tuning range curve for proposed VCO.

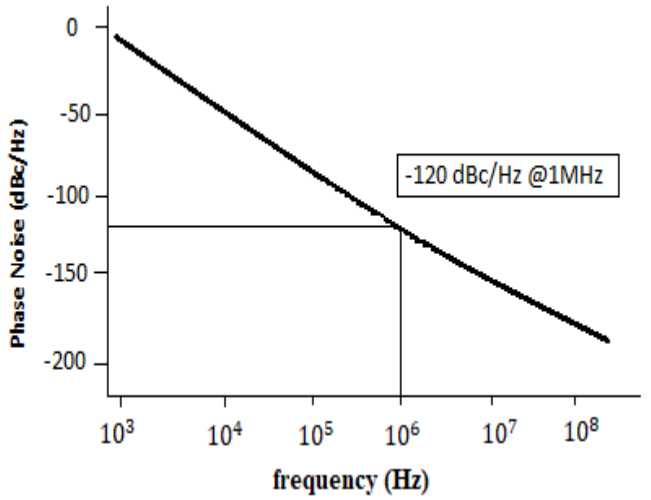

Figure 9: Phase noise curve for the proposed circuit.

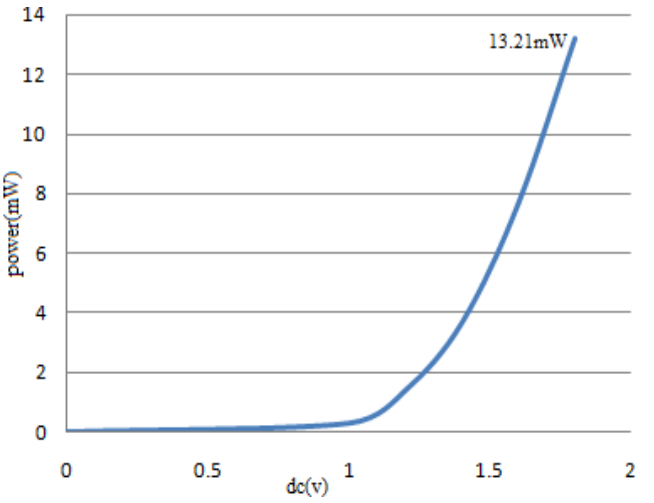

Figure 10: Power dissipation curve for the proposed circuit.

Table 1 shows the results of the proposed circuit and compares it with other works. All the research works shown in the table has been done by using the same technology. Table 2 shows the values of the components that we used in the design.

Table 1
Comparison table with results.

	Phase noise	Tuning range	Tuning voltage	power	Tech. used
This work	-120.3 dBc/Hz@1MHz	20%	0 - 1.8 V	13.21 mW	180nm
[7]	-114 dBc/Hz@1MHz	30%	0 - 2 V	8 mW	180nm
[10]	-116.3 dBc/Hz@1MHz	42%	-	6 mW	180nm
[14]	-117.6 dBc/Hz@1MHz	6.4%	0 - 1.8 V	9 mW	180nm
[15]	-115 dBc/Hz@1MHz	15%	0 - 1.8 V	7.2 mW	180nm
[12]	-107.779 dBc/Hz@1MHz	10.6%	0 - 1.8 V	9.8 mW	180nm

Table 2
Parameters values used in the circuit.

Circuit parameters	Values
Width(PMOS, NMOS)	32 u
Length(PMOS, NMOS)	180 nm
Fingers	1
Multiplier	5

Note-: All parameter values are same for (as shown in table 2) varactor bank also, with only one change. The parameter value for multiplier in varactor bank is 5.

VII. LAYOUT DESIGNING

The layout of the proposed design is shown in Figure 11. Metal1 and metal2 are used for the connections.

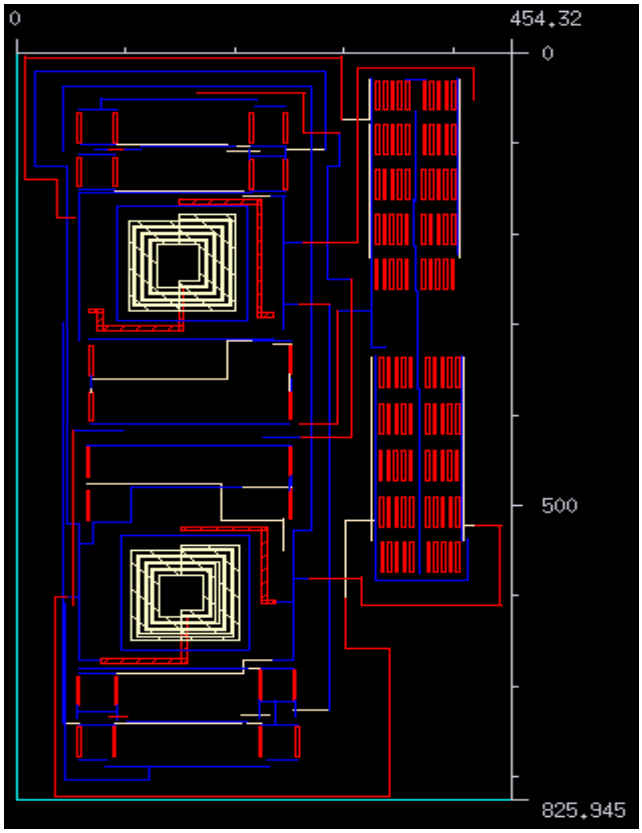

Figure 11: Layout design for proposed circuit.

VIII. CONCLUSION

The proposed design provides the quadrature oscillations with low phase noise of -120dBc/Hz at 1MHz of offset frequency and wide tuning range of 20 percent. This design uses the Varactor Bank circuit designed by MOS rather than the variable capacitor. Adding an extra pair with the LC tank circuit improves the quality factor and reduces the parasitic resistance of the tank circuit.

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