Wideband Inductorless Low-Noise Amplifier Using Three Feedback Paths

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***Abstract*- This paper presents the design of a wideband inductorless low noise amplifier (LNA) in 0.18 μm CMOS technology for multiband wireless communication standards. The LNA is a fully differential common-gate structure. It uses three feedback paths, for choosing arbitrary value of LNA transconductance which leads to a LNA with higher gain and lower noise figure (NF) over the previously reported amplifiers. Post-layout simulation results show a gain of 20.4 dB with a 3-dB bandwidth of 2.84GHZ, with a 2.62dB NF while dissipating 2.97mW. The IIP3 is -1.67dBm.**

***Index Terms*- Inductorless, Low Noise Amplifier (LNA), Multistandard, Wideband.**

I. INTRODUCTION

Nowadays, GSM, DECT, and GPS which are diverse wireless standards have been developed. It would be straightforward to integrate different wireless receivers together on a chip in order to satisfy the particular demands for each and every application; however, the required power consumption and chip area will be large. As a result, it is desirable to have a multi-standard receiver to meet all the mentioned standards. A wideband receiver is one of the possible solutions for multiband multi-standards receiver.

The Low Noise Amplifier (LNA) is nominated the first gain stage of a wideband receiver. It must meet several specifications simultaneously, which makes the design challenging. LNA should achieve good impedance matching, high, and flat gain, low noise figure (NF) across a wide frequency band,good linearity, and low area and power consumption.

With the help of several methods, wideband input matching for wideband amplifier can be achieved; such as using the distributed amplifier [1], [2], the filter-type amplifier [3], and the resistive shunt feedback amplifier [4], [5]. However these methods may suffer from various disadvantages such as high power consumption, large chip area, and inadequate NF.

One of the wideband LNA topologies that have been widely investigated is the common-gate low-noise amplifier (CGLNA) [7], [8]. A common-gate structure has better wideband input impedance matching than a common-source structure. Beside the simple input matching architecture (1/gm=Rs), the CGLNA Also offers good linearity, stability, low power consumption, and robustness to PVT variation. However, its main drawback is the relatively high noise figure (NF) [6]. This is due to the tradeoff between the noise factor (F) and input impedance matching requirement (Zin=Rs).

In this paper, a gm-boosting scheme has been applied to a CGLNA to break the traditional link between the input matching and noise figure, and leads to a simultaneous reduction in noise and power dissipation in order to retain the advantages of the CG configuration and overcome its deficiencies. The use of three feedbacks improves the gain compared to all of the other CGLNA topologies. The whole structure is designed without the use of any bulky inductors, thus requires a less area. The presented LNA covers frequency bands for digital video broadcasting (DVB) at 450-850MHZ,global system for mobile communication(GSM) at 900MHZ,global positioning system(GPS) at 1.21 and 1.5 GHZ and cellular radios at 850-1900MHZ which provides a practical solution for multi-standard application. This paper is organized as follows. Section II reviews the gm-boosting technique by using negative feedback and section III discusses a new positive feedback with nmos transistor are discussed. The proposed circuit is presented in section IV then Section V presents post-layout simulation results and finally, section VI presents the conclusion and outline of this paper.

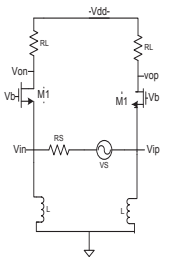

Figure 1: Differential CGLNA

II. CIRCUIT DESCRIPTION

From Figure 1, which shows the differential CGLNA, gain and input impedance can be obtained as below:

$$Av = gm_1 R_L \quad (1)$$

$$R_{in} = \frac{2}{gm_1} \quad (2)$$

where gm_1 is the transconductance of M1. By assuming matching condition as $R_{in} = 2R_s = 100\Omega$, the noise factor is given by

$$F = 1 + \frac{\gamma}{a} + \frac{4R_s}{R_L} \quad (3)$$

In Equation 3, γ is the channel thermal noise coefficient $(1 < \gamma < 2)$, and $a = g_m / g_{do}$, g_{d0}, is zero-bias drain conductance. By following the above equation, input matching condition force gm_1 to be equal to 20mS. In this condition, we cannot increase arbitrarily gm_1 for noise reduction. Therefore, gain can be increased through a gm-boosting technique which is suggested in Figure 2(a). Wherein inverting amplification, A, is introduced between the source and gate terminal of M1, so that gm_1 is boosted to $gm_1(1+A)$ and input impedance matching is given by:

$$\frac{1}{gm_1(1+A_{NEG})} = R_s = 50\Omega \quad (4)$$

This configuration leads to smaller bias current, less channel noise from the input transistor M1,and consequently smaller noise contribution and power consumption. F which is given by

$$F = 1 + \frac{\gamma}{(1+A_{NEG})\alpha} + \frac{aR_s}{R_L} \quad (5)$$

A capacitor-cross-coupling (CCC) is one of the possible ways to achieve passive inverting gain in this technique [6], [7], as shown in Figure 2(b), A is approximately given by the capacitor voltage division ratio

$$A = \frac{c_2}{c_2 + c_{gs1}} = \frac{1}{1 + c_{gs1}/c_{gs1}} \quad (6)$$

In Equation 6, c_{gs1} is the gate-source capacitance of M1. For $C_1 >> C_{gs1}$, $A \cong 1$ and F simplifies from Equation 5 to 7:

$$F = 1 + \frac{\gamma}{2a} + \frac{4R_s}{R_.} \quad (7)$$

And

$$Av = 2gm_1R_L \quad (8)$$

$$R_{in} = 2R_s = \frac{2}{2gm_1} = \frac{1}{gm_1} \quad (9)$$

In this case, F is reduced and the effective transconductance is increase with a concomitant decrease in power dissipation.

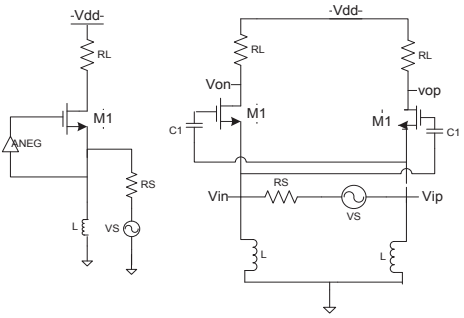

Figure 2: gm-boosting Technique

III. BASIC IDEA

The use of capacitors does not increase PDC but A is set to 1 for minimum NF, gm_1 is restricted to 10 mS for input matching, reducing the gain in order to achieve high gain and low NF. A positive feedback can be inserted along with the negative feedback. But in the previous research pmos transistor is always used (Figure 3) [8], [9]. The idea in this paper is to use nmos type instead of pmos type (Figure 4), because of following reasons:

1-pmos transistor should have larger size than nmos type to reach the same transconductance that leads to increase parasitic capacitor which causes to decrease bandwidth. Consequently, in proposed structure the larger bandwidth is obtained in previous works.

2-as shown in Figure 4, since by placing nmos transistor at the input, indeed it uses current reuse technique which leads to reduce power consumption.

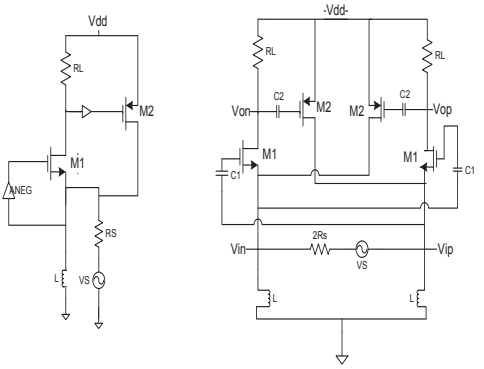

Figure 3: Positive feedback in previous works

This feedback has the effect of increasing the input impedance:

$$R_{in} = 2R_s = \frac{2}{2gm_1(1 - R_L\beta gm_2)} \quad (10)$$

This feedback affects the input impedance and does not influence the value of transconductance coefficient. Assuming

$A_{pos} = R_L \beta\, gm_2$, which varies from 0 to 1 for stability and A_{pos} can be 0 to 1 for an arbitrary choice of gm_1 to achieve an input matching condition. So the impedance matching does not set transistor biasing current and the current is variable to reduce noise. For example, suppose that:

$$A_{NEG} = 1, \quad A_{pos} = 0.5, \quad R_s = 50 \tag{11}$$

According to above, $gm_1 = 20ms$ thus, the gain increases. Considering the thermal channel noise under input matching condition, the f is given by:

$$F = 1 + \frac{1 - A_{pos}\gamma}{1 + A_{NEG}a} + gm_2 R_2 \frac{\gamma}{a} + \frac{R_s}{R_L}(2 - A_{pos})^2 \tag{12}$$

According to Equation 10 and 11, we have:

$$Av = 2gm_1 R_L \tag{13}$$

$$R_{in} = 2R_s = \frac{2}{gm_2} \tag{14}$$

$$F = 1 + \frac{\gamma}{4a} + gm_2 R_s \frac{\gamma}{a} + \frac{9R_s}{4R_L} \tag{15}$$

The third term in Equation 15 represents the noise due to M2 and can be decreased by using small gm_2 .thus the combination of negative and the positive feedback have more power consumption that can decrease noise when compared to negative feedback alone with higher gain.

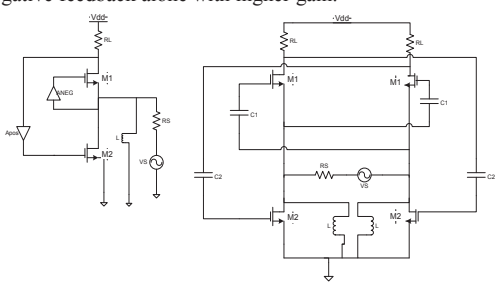

Figure 4: Proposed positive feedback

IV. PROPOSED LNA

Now, instead of bulky inductor that uses more area, we use current sources (M3) that are capacitive coupled $C_3 >> C_{gs3}$ (Figure 5) [10], [11].

The capacitively coupled M3 creates another positive current feedback. Besides small occupation area another freedom degree of input matching condition is provided.

So, there will be more flexibility in choosing the best value of the LNA transconductance which achieve minimum NF.

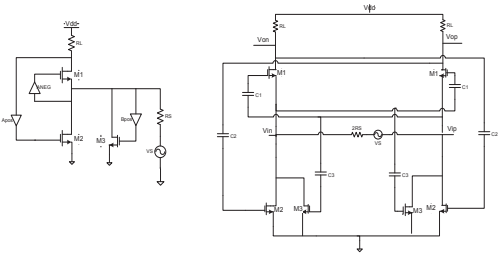

Fig.5. Proposed LNA

A. Input impedance

$$R_{in} = 2R_s = \frac{2}{2gm_1(1 - R_L \beta gm_2)Cgm_3} \tag{16}$$

Assuming $A_{pos} = R_L \beta\, gm_2, \beta_{pos} = \frac{Cgm_2}{2gm_2}$,

and $A_{NEG} = 1$, so we have:

$$R_{in} = 2R_s = \frac{2}{2gm_1(1 - A_{pos} - \beta_{pos})} \tag{17}$$

Thus, the input matching condition is given by

$$2gm_1 R_s(1 - A_{pos} - \beta_{pos}) = 1 \tag{18}$$

From Equation 18, two degrees of freedom, A_{pos} and β_{pos} , exist that allow arbitrary choice of gm_1 achieving high gain and low NF.

B. Noise analysis

For noise analyses, we draw noise current sources that due to the thermal noise of the transistors, load, and source resistance as shown in Fig.6 and replace the capacitors by short circuit since they are much larger than the capacitance of input transistors M1 and M3.

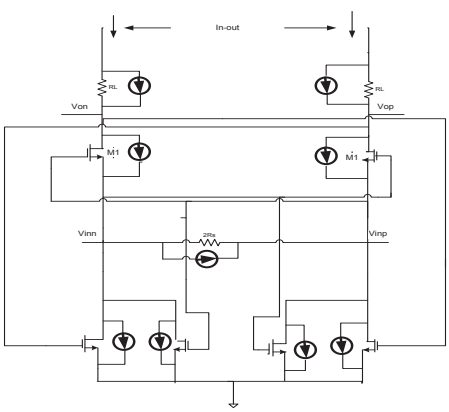

Figure 6: Schematic of the proposed LNA showing noise sources

The output differential current due to each noise source is given by:

Thermal noise due to the source resistance:

$$\overline{\iota^2_{ns-out}} = AkTR_s gm_1^2 \Delta f \quad (19)$$

Thermal noise due to the M1:

$$\overline{\iota^2_{n1-out}} = 4kT\frac{\gamma_2}{a} gm_1 (gm_1 R_S - 1)^2 \Delta f \quad (20)$$

Thermal noise due to the M2:

$$\overline{\iota^2_{n2-out}} = 4kT\frac{\gamma_2}{a} gm_2 (gm_1 R_S)^2 \Delta f \quad (21)$$

Thermal noise due to the M3:

$$\overline{\iota^2_{n3-out}} = 4kT\frac{\gamma_3}{a} gm_3 (gm_1 R_S)^2 \Delta f \quad (22)$$

Assuming $\gamma_1 = \gamma_2 = \gamma_3 = \gamma$, the noise factor is given by:

$$F = \frac{\overline{\iota^2_{ntotal-out}}}{\overline{\iota^2_{ns-out}}} = 1 + \frac{\gamma}{a}\frac{(gm_1 R_d - 1)^2}{gm_1 R_s} + \frac{\gamma}{a} gm_2 R_2 \frac{\gamma}{a} + gm_2 R_s + \frac{R_s}{R_L}(1 + \frac{1}{2gm_1 R_s})^2 \quad (23)$$

Under the input matching condition:

$$2gm_1 R_s (1 - A_{pos} - \beta_{pos}) = 1 \rightarrow$$

$$2gm_1 R_s (1 - A_{pos} - \frac{gm_3}{2gm_1}) = 1 \rightarrow$$

$$gm_3 R_s = 2gm_1 R_s - 1 - 2gm_1 R_s A_{pos} \quad (24)$$

And assuming $\eta = gm_1 R_s$, the F is reduced to:

$$F = 1 + \frac{\gamma}{a}\frac{(\eta - 1)^2}{\eta} + 2\frac{\gamma}{a}(1 - A_{pos})\mu - \frac{\gamma}{a}(1 - \frac{R_s}{R_L} A_{pos}) + \frac{R_s}{R_L}(1 + \frac{1}{2\eta})^2 \quad (25)$$

To determine optimum value for designing, we will estimate the amount of η

$$\frac{dF}{d\eta} = 0$$

$$\eta_{opt} = \frac{1}{\sqrt{3 - 2A_{pos}}} \quad (26)$$

The third term in Equation 25 plays an important role in noise reduction and we can say that the combination of three feedbacks contributes to noise cancellation.

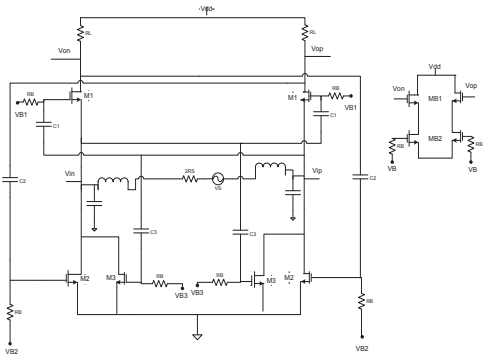

Figure 7: Schematic of the entire LNA with the output buffer

V. RESULTS

The LNA has been implemented in TSMC 0.18-um CMOS technology. The total schematic of the LNA with the output buffer, pad capacitor, and bonding wire inductor is shown in Figure 7. A buffer is used at the LNA output to drive the 50-Ω load of the measuring equipment. The core LNA consumes 1.65mA from 1.8 V supply. The layout of the design has been done in cadence in order to obtain the practical results. The layout is shown in Figure 8. Figure 9-15 show the post layout simulated S-parameters, voltage gain, NF, and IIP3, respectively. The S_{11} is lower than -10dB until 2GHZ (Figure 9). Figure 10 and 11 also show the measured output return loss and reverse isolation: S_{22} is below -10dB up to 2GHZ, while S_{12} is below -23dB across the band. The voltage gain is 20.35dB with a 3-dB bandwidth of 2.83 GHZ (Figure 13).The minimum NF is 2.62 dB at 913 MHZ (Figure 14).Two-tone testing is performed with 100MHZ spacing for third-order inter-modulation distortion which is shown in Fig.15.the measured IIP3 is -1.67 dBm.

Table 1 show the performance summary of this work and compares with previous published wideband LNAs. The FOM defined in [12] is adopted.

$$FOM = \frac{BW(GHZ).GV(Lin).PIIP3(mW)}{P_{DC}(mW).(F_{Lin} - 1)} \quad (27)$$

where:

$$Av(dB) = 20\log GV_{Lin} \quad (28)$$

$$IIP3(dB) = 10\log\frac{PIIP3}{1(mW)} \quad (29)$$

$$NF = 10\log F_{Lin} \quad (30)$$

As shown in this table, the FOM of this work is better than other works, because it has low noise, low power consumption, high linearity, and high bandwidth simultaneously.

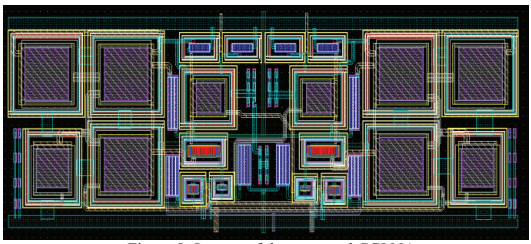

Figure 8: Layout of the proposed CGLNA

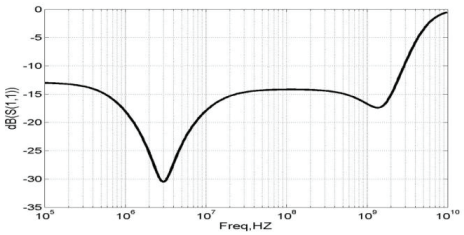

Figure 9: Simulated S11 of proposed CGLNA

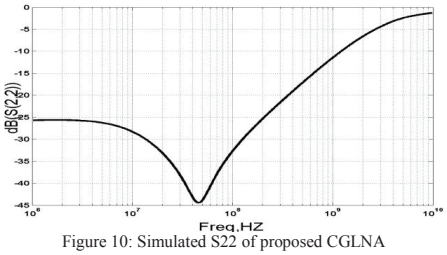

Figure 10: Simulated S22 of proposed CGLNA

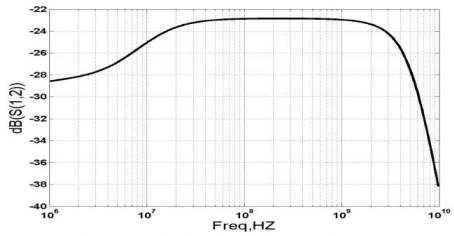

Figure 11: Simulated S12 of proposed CGLNA

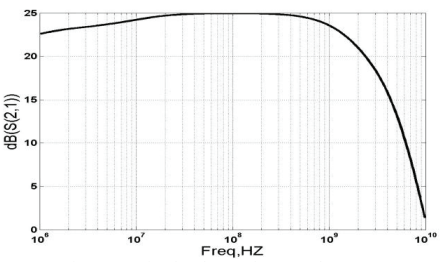

Figure 12: Simulated S21 of proposed CGLNA

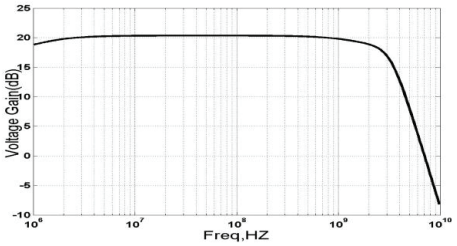

Figure 13: Simulated gain of proposed CGLNA

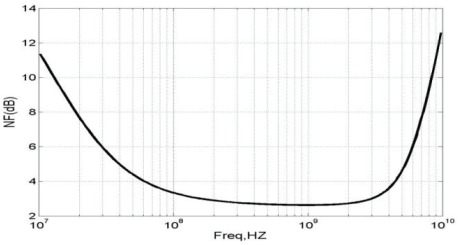

Figure 14: Simulated NF of proposed CGLNA

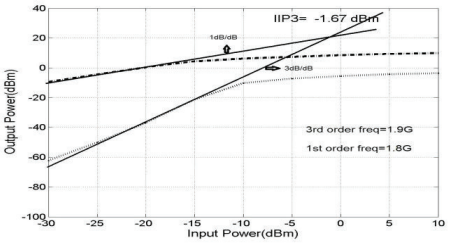

Figure 15: Simulated IIP3 of proposed CGLNA

VI. Conclusion

In this paper, a wideband inductorless LNA for multiband multistandard receiver is proposed. It uses three feedback paths for choice gm value arbitrarily for input matching and end to tradeoff between noise and input power matching. Post-layout simulation results show a voltage gain of 20.5dB with a 3-dB bandwidth of 3.19GHZ. A minimum NF of 2.3dB and an IIP3 of -2.17dBm while dissipating 1.65mA from 1.8V supply.

Table I
Comparison with recently published LNA

Ref.	(dB) Gain	BW (GHZ)	NF (dB)	IIP3 (dBm)	P_{DC} (mW)	Tech cmos	FOM
[13]	16.9	1.05−3.05	2.57	−0.7	12.6	um 0.18	1.178
[8]	21	0.3−0.92	3.5	−3.2	3.6	um 0.18	0.71
[14]	20.5	0.02−1.18	3	2.7	32.4	um 0.18	0.71
[15]	13.7	0.002−1.6	2.4	0	35	um 0.25	0.31
[16]	16	0.4−1	3.5	−17	16.8	90 nm	0.003
[17]	21	0.002−2.3	1.7	−1.5	18	90 nm	2.13
[7]	20	0.1−2.7	4	−12	1.32	um 0.13	0.78
[18]	19	0.2−3.8	2.8	−4.2	5.7	um 0.13	2.37
[19]	18	0.1−5	4	−8	20	um 0.13	0.19
[20]	13	0.1-1.6	2.1	5.5	20.8	65nm	1.83
[21]	12.6	0.1-7	5.5	-9	0.75	90 nm	1.9
[10]	23	0.1−1.77	1.85	−2.85	2.8	90 nm	8.1
This work(post-lay)	20.4	−2.84 0.005	2.62	−1.67	2.97	um 0.18	8.33

REFERENCES

[1] K. Entesari, A. R. Tavakoli, and A. Helmy, "CMOS distributed amplifiers with extended flat bandwidth and improved input matching using gate line with coupled inductors,"IEEE Trans. Microw. Theory Tech., vol. 57, no. 12, pp. 2862–2871, Dec. 2009.

[2] R. Liu, C. Lin, K. Deng, and H. Wang, "A 0.5–14-GHz 10.6-dB CMOS cascode dstributed amplifier," inProc. Symp. VLSI Circuits Dig. Tech. Papers, pp. 139–140, June 2003.

[3] A. Bevilacqua and A. M. Niknejad, "An ultra-wideband CMOS low-noise amplifier for 3.1 to 10.6 GHz wireless receiver,"IEEE J. Solid-State Circuits, vol. 39, no. 12, pp. 2259–2268, Dec. 2004.

[4] C.-W. Kim, M.-S. Kang, P. T. Anh, H.-T. Kim, and S.-G. Lee, "An ultra-wideband CMOS low noise amplifier for 3–5 GHz UWB system," IEEE, J. Solid-State Circuits, vol. 40, no. 2, pp. 544–547, Feb. 2005.

[5] T. Chang, J. Chen, L. A. Rigge, and J. Lin, "ESD-protected wide-band CMOS LNAs using modified resistive feedback techniques with chip-on-board packaging,"IEEE Trans. Microw. Theory Tech., vol. 56, no. 8, pp. 1817–1826, Aug. 2008.

[6] W. Zhuo, X. Li, S. Shekhar, S. H. K. Embabi, J. P. de Gyvez, D. J. Allstot, and E. Sanchez-Sinencio, "A capacitor cross-coupled common-gate low-noise amplifier,"IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 52, no. 12, pp. 875–879, Dec. 2005.

[7] F. Belmes, F. Hameau, M. Fournier,"A low power Inductorless LNA with Double Gm Enhancement in 130 nm CMOS".in IEEE Journal of Sollid-state Circuits,May.vol.47,no.5,pp.1094-1103, 2012.

[8] S. Woo, W. Kim, C. Lee, K. Lim, and J. Laskar, "A 3.6 mW differential common-gate CMOS LNA with positive-negative feedback," inIEEE Int. Solid-State Circuits Conf. Tech. Dig. pp. 218–219, Feb. 2009.

[9] A. Saleh, M. Ortmanns, and Y. Manoli, "A Low-Power Differential Common-Gate LNA," IEEE, pp. 137-140, 2008.

[10] E. Sobhy, A. Helmy, S. Hoyos, K. Entesari, E. Sinencio," A 2.8-mW Sub-2-dB Noise-Figure Inductorless Wideband CMOS LNA Employing Multiple Feedback",Ieee Transactions on Microwave Theory And Techniques,December.Vol.59,No.12,pp.3154-3160, 2011.

[11] A. Amer, E. Hegazi, and H. Ragai, "A low-power wideband CMOS LNA for WiMAX,"IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 54, no. 1, pp. 4–8, Jan. 2007.

[12] M. Okushima, J. Borremans, D. Linten, and G. Groeseneken, "A DC-to-22 GHz 8.4 mW compact dual-feedback wideband LNA," in Proc. IEEE Radio Frequency Integrated Circuits Symp, pp. 295–298, Jun. 2009.

[13] K. Jusung, D. Hoyos, and J. Silva-Martinez, "Wideband common-gateCMOS LNA employing dual negative feedback with simultaneousnoise, gain, and bandwidth optimization," IEEE Trans. Microw.Theory Tech. , Sep., vol. 58, no. 9, pp. 2340–2351, 2010.

[14] S. Seong-Sik, I. Dong-Gu, K. Hong-Teuk, and L. Kwyro, "A highlylinear wideband CMOS low-noise amplifier based on current ampli-fication for digital TV tuner applications,"IEEEMicrow. WirelessCompon. Lett. , Feb, vol. 18, no. 2, pp. 118–120, 2008.

[15] F. Bruccoleri, E. Klumperink, and B. Nauta,"Wide-band CMOSlow noise amplifier exploiting thermal-noise canceling," IEEE J.Solid-State Circuits, Feb.vol. 39, no. 2, pp. 275–282, 2004.

[16] M. Vidojkovic, M. Sanduleanu, J. van der Tang, P. Baltus, and A. van Roermund, "A 1.2 V, inductorless, broadband LNA in 90 nm CMOS LP," inIEEE RFIC Symp. Dig., pp. 53–56, 2007.

[17] M. Nozahi,Helmi.A,Sinencio.E, K.Entesari," An Inductor-Less Noise-Cancelling Broadband Low Noise Amplifier With Composite Transistor Pair in 90 nm CMOS Technology",IEEE Journal Of Solid-State Circuits ,May, Vol.46,NO.5,pp.1111-1122, 2011.

[18] H. Wang, L. Zhang, and Z. Yu,"A wideband inductorless LNA with local feedback and noise cancelling for low-power low-voltage applications,"IEEE Trans. Circuits Syst. I, Reg. Papers, Aug, vol. 57, no. 8, pp.1993–2005,2010.

[19] D. Im, I. Nam, J-Y. Choi, B-K. Kim, and K. Lee, "A CMOS active feedback wideband single-to-differential LNA using inductive shunt-peaking for SAW-less SDR receivers," in IEEE A-SSCC Tech. Dig., Nov, pp. 1–4,2010.

[20] Chung. T, Lee. H, Jeong. D, Yoon. J, Kim. B, "A Wideband CMOS Noise-Cancelling Low-Noise Amplifier With High Linearity," in IEEE Microwave and wireless components letters, June, pp.1-3, 2015.

[21] Parvizi. M, Allidina. K, El-Gamal. M, "A sub-mW ultra Low-Voltage wideband Low-Noise amplifier design technique," in IEEE, vol. 23, no. 6, pp. 1111-1112. 2015.