Design Characterization and Verification of Channel Bandwidth Selectivity and Linearity Performance of I/Q Baseband Receiver SoC

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***Abstract*— This paper presents the methodologies used to characterize and verify critical parameters of a differential In-phase/Quadrature (I/Q) baseband channel of an integrated circuits system, consisting of amplifiers and filters in a single chip radio transceiver. It is a highly compact circuit of novel Software Defined Radio (SDR), System-on-Chip (SoC) to support Multi-Band and Multi-Mode operation. The architecture is designed to fulfill the critical requirements of very low power consumption, high linearity, very low noise floor, optimized chip size and high reliability for wideband radio networks transceiver applications. Integrating the entire wireless transceiver system into a single chip can greatly minimize its size, simplify assembly process, and decrease manufacturing costs. However, the characterization and verification processes of such customized SoC is very much daunting and time consuming. This paper discusses an industrial standard procedure to verify such requirements in complex design and development stages. In general, the required receiver baseband path consists of amplifiers and filters line-up to perform 75dB Inter-Modulation Distortion (IMD) suppression or blocking capability. Detailed parameters subjected to characterization are shown and verified to the specification of SDR transceiver SoC . The SoC architecture has low noise amplifier (LNA), local oscillator, down conversion mixer, post mixer amplifier, and baseband path. The baseband path includes several receiver components, such as amplifiers and low pass filters (LPFs) producing low BW selectivity errors, high linearity, and low baseband noise. Finally, the critical parameters of the amplifier and filter blocks are measured and verified to satisfy the required design specifications.**

***Index Terms*— Characterization, Multi-Band, Multi-Mode, SoC, Baseband, Transceiver, RFIC.**

I. Introduction

Single chip radio system integrates transmitter, receiver, amplifier, power management components and other baseband logic circuits into one single chip. The realization of a single chip radio is greatly motivated by deep sub-micron CMOS technology capability in terms of size and low power consumptions. High level of integration increases the reliability of the final product. The following contents of this paper discuss the characterization analyses of the receiver baseband path, from the overall architecture design into its detailed critical parameters verification perspective. The transceiver SoC IC is designed to support analog VHF/UHF/ 700/800/1000MHz FM, and Linear QAM.

II. Overall System Design

The receiver chain contains RF input line-up to meet direct conversion and super heterodyne receiver requirements from 49MHz to 1GHz. The RF channel contains a low noise amplifier (LNA), variable gain amplifier (VGA), and quadrature sampling demodulator. The output of the demodulator interfaces to a complete baseband section, containing highly linear post mixer amplifier (mixer AB AMP.), four poles of selectivity feature, IF amplifier stages, and sigma delta Analog-to-Digital Converter (ΣΔ ADC), and post-ΣΔ ADC digital formatting section. The baseband bandwidth selectivity is compensated for temperature and provides tolerances with variable RC track compensation. This SoC incorporates a passive 1-Pole after the first Mixer AB AMP to provide additional selectivity. The output stage is a Synchronous Serial Interface (SSI) with programmable rates to accommodate multiple protocols.

The receiver RF path interface impedance is the differential 50 ohms with a DC common mode voltage of approximately 1.80V. The output of the analog signal path is sampled and digitized using high-resolution ΣΔ ADC. The digitized signal enters a digital portion of the receiver consisting of decimation filters, digital filters, digital formatting and serial data port of SSI. Any unique circuitry to a specific mode of operation is to be powered down during the disable mode to conserve power. The receiver path consists of a RF-to-analog baseband and a small digital sub-block with the RC ramp-tune compensation for the 1-Pole filter. The designed analog baseband sub-systems are LNA, a down mixer, a low noise post mixer amplifier, a 1-Pole filter with a tracked, programmable corner frequency, and a baseband amplifier with step programmable gain. The output of the analog signal path is routed to an external baseband IC for DSP. A down mixer is a baseband path that provides tunable selectivity for enhanced dynamic range and a high precision ΣΔ ADC. The output of the ΣΔ ADC is post-processed and formatted for SSI interface to the DSP. The overall description of the SoC receiver function is delineated below [1]:

1. The receiver front end topology has a distributed filter-LNA-filter-LNA configuration to provide sufficient front end selectivity to meet out-of-band blocking to

ensure sufficient reverse isolation to LO spurious emissions at the antenna feral and to reduce individual LNA gain requirements to enhance linearity.

2. The SoC Transceiver is designed to support 75dB IM suppression performance in Direct Conversion Radio (DCR) mode with system blocking performance of 100dB at 1MHz to offset relative to usable sensitivity.
3. There is an internal, on chip FGU for the first LO. The first LO VCO is an external block; therefore, the LO into the DCR must be 2x, 4x, or 8x based on the desired RF frequency to mitigate self-quieting.
4. The RF input is the differential, with an external 1:1 transformer providing a single ended-to-differential transformation. The transformer also serves to provide a ground return path for the LNA differential input pins.

III. BASEBAND ANALOG INTERFACE DEFINITION

The receiver baseband input incorporates the ability to "switch in" a Wide Band (WB) pole. The corner of the WB pole is set by an external differential switch capacitor with 1.6kohm differential source impedance from the down mixer and a pair of 500ohm series resistors. The WB pole is intended to enhance far-out blocking performance and should be set nominally to 150kHz, -3dB corner for most narrow band protocols, or an external capacitance of approximately 620pF differential. The physical receiver line-up path architecture interconnectivity and its overall requirements are shown in the Figure 1.

IV. BASEBAND 1-POLE LPF

The 1-Pole low pass filter (LPF) corner frequency will be programmable in 9.5% steps. This intermediate frequency (IF) filter works together with the baseband 2-Pole filter to produce a composite 3-pole response. The desired -3dB corner frequencies are characterized for the possible bandwidth settings of the 1-Pole filter. The resistor values are selected to minimize the noise contribution of the filter, while maintaining a reasonable capacitance value. The resistors selection BW5 [Hex] is the MSB of the serial-peripheral-interface (SPI) bits field BW [5:0] and it will also be used to select between bandwidth range 1 and range 2 of the filter. In range 1, the differential filter capacitor is 400pF. As for range 2, a portion of the differential filter capacitor is to be switched out to realize wider bandwidths.

Generally, the use of a different capacitor range will necessitate another filter tune. The baseband filter bandwidths shall be within +/-6% of the expected bandwidth and +/-12% tolerance from schematic to parasitics extracted layout. The filter resistor is composed of a tapped resistor string. The bandwidth tuning and corner frequency tracking are accomplished by selecting the appropriate tap on the resistor string as illustrated in Figure 2. The specifications consider maximum noise of a resistor with 20% higher than the nominal. This is due to the process of tolerances and the nominal resistor value for the given bandwidth setting. Bandwidth setting 1 corresponds to the second programmable bandwidth and does not refer to the tracking range [2].

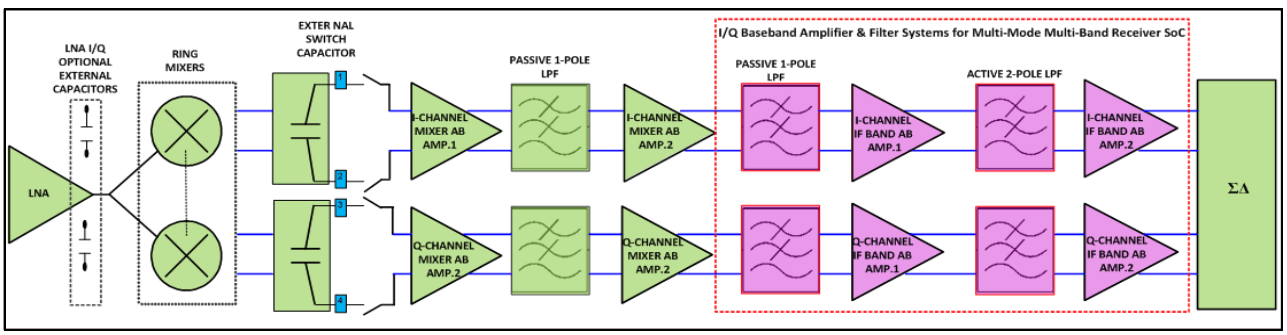

Figure 1: I/Q Baseband Receiver Path of SoC

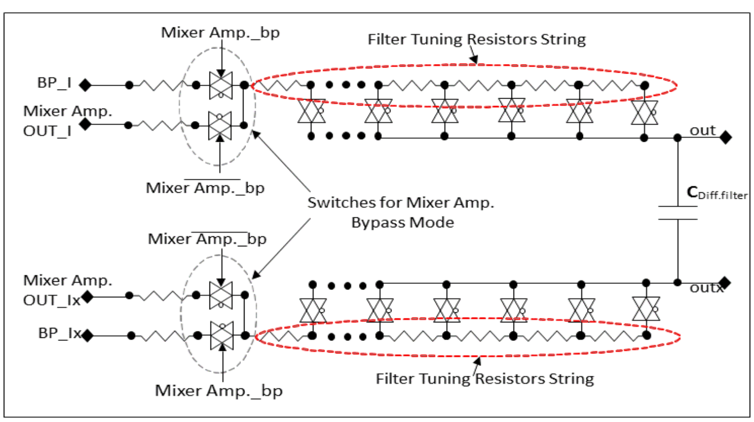

Figure 2: Differential 1-Pole Filter Interface

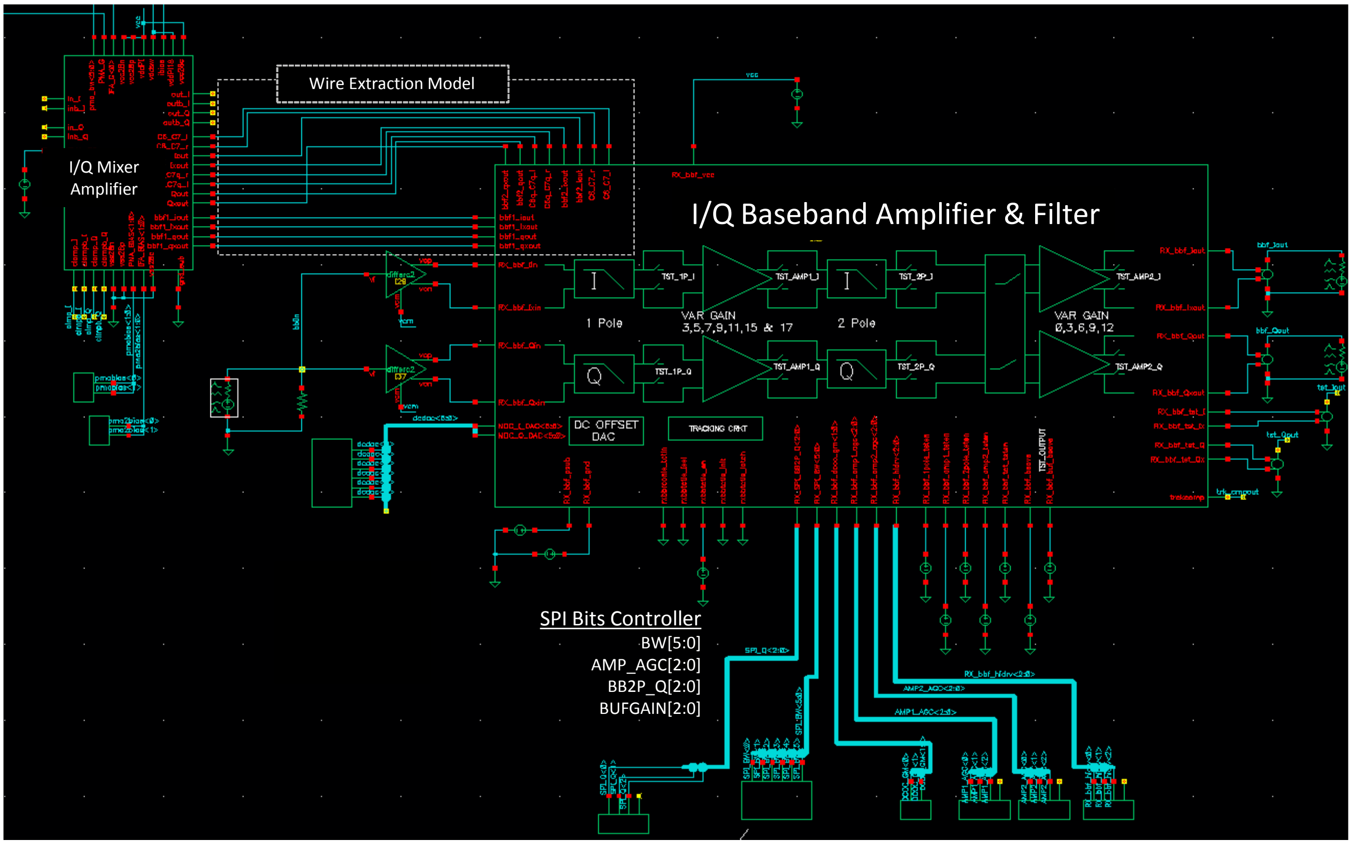

Figure 3: Schematic Testbench Setup of I/Q Baseband Path (Amplifier and Filter)

V. Baseband AB Amp.1

Baseband Amp.1 is a variable gain amplifier (VGA) with low input referred noise and 8 programmable 2dB gain steps. VGA architecture is implemented to maximize the dynamic range performance of the overall system. The SPI bits AMP_VGA [2:0] determines the gain of the amplifier. A critical condition to be considered is to match the gain steps between the I/Q path to avoid changing receiver sideband suppression when baseband gain is changed. The required amplifier is designed to have 8 gain programmable tuning steps from 3 dB to 17 dB in 2 dB increments.

VI. Baseband 2-Pole LPF

The active 2-Pole RC filter stage has a unity gain and incorporates a tapped series resistor for setting the filter bandwidth. The -3dB corner is slaved to the tracking oscillator designed to provide a clean bandwidth adjustment when a frequency error greater than half a programming step is detected. The nominal Q value for this filter in DCR mode is 1.0. For the specified Q, there will be about 1.25 dB overshoot in the response. This is required to give a flat composite filter response when cascaded with the baseband 1-Pole filter.

VII. Baseband AB Amp.2

The second baseband amplifier is cascaded between baseband 2-Pole LPF and ΣΔ ADC. This amplifier has five gain settings in 3dB voltage steps of 0, 3, 6, 9 and 12 dB. The control SPI bits BUFGAIN [2:0] controls the gain. It acts as a buffer required to drive the ΣΔ ADC input settling times, depending on the baseband radio mode of operation [3].

VIII. Design Measurements And Verification of 1-Pole and 2-Pole LPF

A complete top hierarchy layout with the extracted parasitics is simulated by injecting the 1Vpeak AC signals into each differential I/Q input pins as shown in Figure 3. Then, a test bench following a rigorous characterization plan is conducted to analyze the circuits' -3dB corner BW behavior that covers all BW settings, IC fabricator's process mismatches, wafer corner process variations, supply voltage changes, and temperature variances (PVT) from -40°C to 100°C.

A. Bandwidth Corner Requirement

The -3dB corner of LPFs is measured at differential I/Q signals of 1-Pole and 2-Pole for all BW[5:0] settings to determine clean channel cut-off and pass-band clearance [4]. The -3dB bandwidth measurement is then repeated to verify composite's bandwidth corner at the output of 2-Pole LPF. Table 1 shows the results of -3dB corner frequency of the baseband passive 1-Pole and active 2-Pole LPF together with its composite output over 36 bandwidth settings. It is observed that all -3dB corner outputs for BW[5:0] Hex settings fall within the expected specifications as shown in Figure 4(a) and 4(b) for better visualization. The Q of the 2-Pole filter is well controlled by the SPI bit settings BB2P Q[2:0]. Obviously, with the 2-Pole filter, Q is set to a nominal value of 1.0 shown in Figure 5. The composite filter response of the baseband 1-Pole and baseband 2-Pole LPF stage has a flat pass band response and linear phase across the pass band as shown in Figure 6 [5].

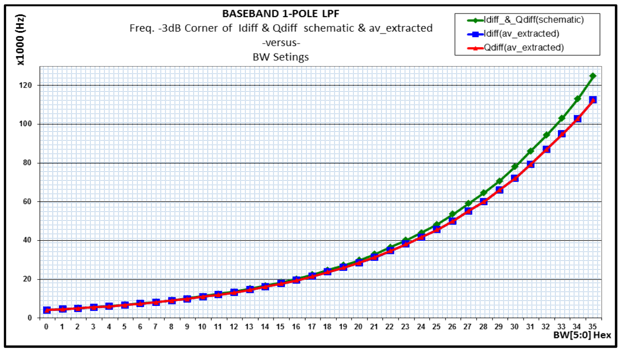

Figure 4(a): -3dB Corner of 1-Pole LPF

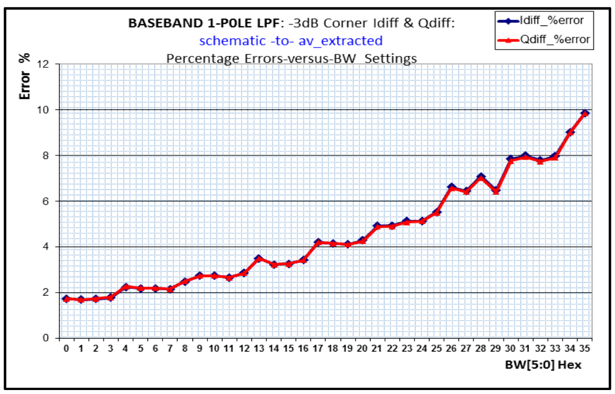

Figure 4(b): -3dB Corner of 1-Pole LPF;
(Schematic-to-Layout % Errors)

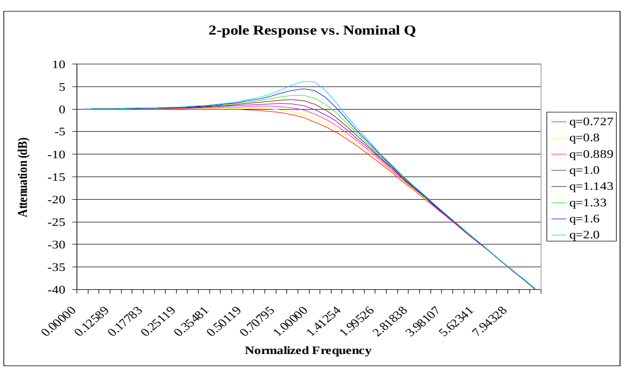

Figure 5: Normalized Amplitude Response of 2-Pole LPF

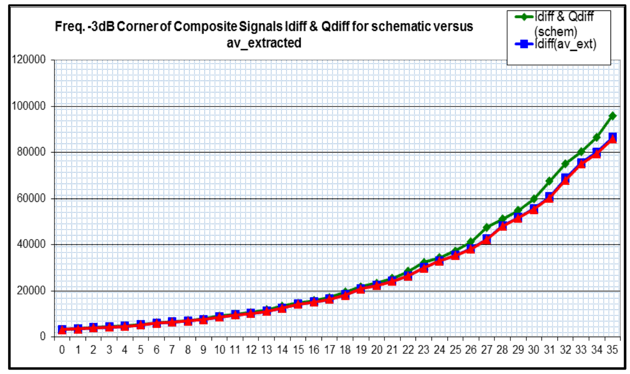

Figure 6: -3dB Corner of Composite Signals

Table 1
-3dB Corner Baseband 1-Pole and 2-Pole LPF

BW SETS		1-POLE LPF Extracted Model		2-POLE LPF Individual Block AV_EXTRACTED		1-POLE & 2-POLE LPF Composite AV_EXTRACTED	
		I_diff	Q_diff				
BW (Dec)	BW [5:0] (Hex)	3dB BW Hz	3dB BW Hz	I_ diff 3dB BW Hz	Q_ diff 3dB BW Hz	I_ diff 1.25dB BW Hz	Q_ diff 1.25dB BW Hz
0	0	4147	4147	5303	5303	3183	3182
1	1	4600	4600	5759	5759	3564	3562
2	2	5065	5064	6489	6491	4061	4060
3	3	5557	5556	7230	7231	4353	4351
4	4	6105	6104	7871	7872	4703	4700
5	5	6786	6785	8529	8531	5211	5207
6	6	7481	7480	9494	9498	6024	6017
7	7	8217	8217	10680	10680	6466	6462
8	8	9003	9002	11670	11670	6956	6952
9	9	10000	10000	12630	12640	7640	7634
10	0A	11030	11030	13840	13850	8708	8696
11	0B	12120	12120	15720	15730	9589	9581
12	0C	13270	13270	17270	17270	10290	10280
13	0D	14670	14670	18690	18700	11190	11180
14	0E	16250	16250	20360	20370	12620	12600
15	0F	17850	17850	23050	23070	14210	14200
16	10	19540	19540	25490	25510	15210	15200
17	11	21490	21490	27650	27670	16450	16420
18	12	23790	23790	29970	30000	18240	18200
19	13	26160	26160	33500	33550	20970	20940
20	14	28630	28640	37360	37400	22430	22390
21	15	31390	31400	40820	40860	24180	24130
22	16	34780	34790	44120	44180	26510	26440
23	17	38180	38200	48410	48540	30020	29890
24	18	41830	41830	54760	54850	33090	33000
25	19	45690	45700	59900	59990	35380	35280
26	1A	50140	50160	64630	64730	38260	38120
27	1B	55310	55320	69900	70060	42530	42300
28	1C	60170	60210	78500	78750	48260	48090
29	1D	66210	66260	87590	87790	51840	51620
30	1E	72180	72240	94970	95180	55670	55400
31	1F	79420	79460	102400	102700	60780	60360
32	20	87180	87220	113000	113600	68770	68020
33	21	94990	95050	126000	126500	75420	74960
34	22	103000	103000	136900	137400	80150	79590
35	23	112600	112600	148900	148900	86520	85810

This SoC transceiver IC is designed on 0.18micron BiCMOS technology, where it is very crucial to prioritize a characterization plan for PVT and process mismatches. The following Figure 7(a) and 7(b) show the results of -3dB bandwidth corner sets for BW=10kHz emulating nominal operation of differential I/Q pass band for the worst case combinations of PVT. The operating conditions are characterized to cover the wafer fabrication process corner of sigma between +3 to -3 for 100 runs of Monte Carlo simulations, voltage variances between 2.90V to 2.65V, and temperature changes from -50°C to 100°C. The plots show clearly the fact that differential signals for 1-Pole LPF and its composites of 2-Pole LPF are well maintained within very low errors (< 4%) as shown in Table 2.

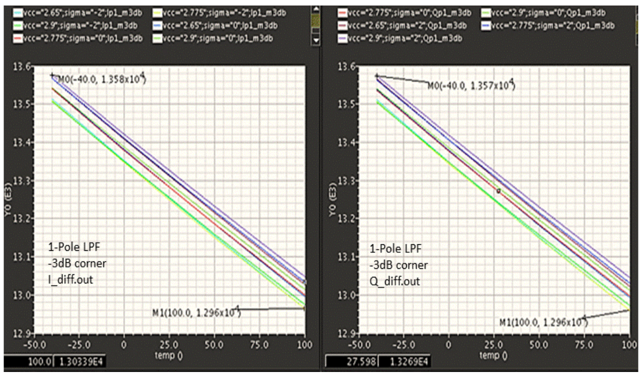

Figure 7(a): -3dB Corner to Pass Band PVT Swept of 1-Pole LPF

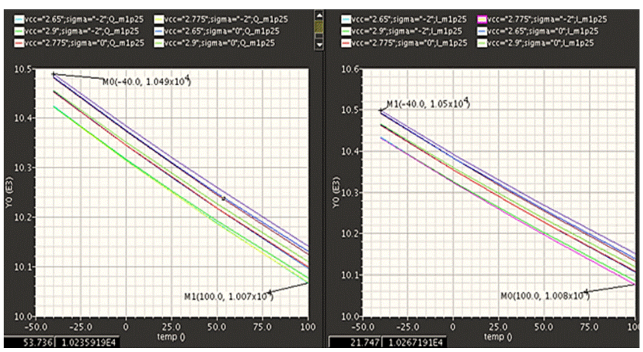

Figure 7(b): -3dB Corner to Pass Band PVT Swept of Composite Signals

Table 2
-3dB Corner Baseband 1-Pole and 2-Pole LPF

Composite LPF PVT Summary (schematic sim)						Schematic—to-av_extracted % errors	
		kHz	sigma	Temp	Vcc	1-Pole PVT	% Errors
I_ Diff	Max. freq.	10880	2	-40	2.90	I_Diff max. freq.	3.069
Q_ Diff	Max. freq.	10880	2	-40	2.90	Q_Diff max. freq.	3.242
I_ Diff	Min. freq	10390	-2	100	2.65	I_Diff min. freq.	2.878
Q_ Diff	Min. freq	10390	-2	100	2.65	Q_Diff min. freq.	2.878
Composite LPF PVT Summary (av_extracted sim)							
		Hz	Sigma	Temp	Vcc	Composite LPF PVT	% errors
I_ Diff	Max. freq.	10490	2	-40	2.90	I_Diff max. freq.	3.718
Q_ Diff	Max. freq.	10500	2	-40	2.90	Q_Diff max. freq.	3.619
I_ Diff	Min. freq.	10070	-2	100	2.65	I_Diff min. freq.	3.178
Q_ Diff	Min. freq.	10080	-2	100	2.65	Q_Diff min. freq.	3.075

1-POLE M.Carlo

	Parameter	Run No.	Freq. Corn.	Parameter	Run No.	Freq. Corn.
			Schematic			
MIN	Ip1_m3db_27	69	13640	Qp1_m3db_27	38	13648
			av_extracted			
MIN	Ip1_m3db_27	69	13270	Qp1_m3db_27	38	13270
	%errors		2.7882			2.848
			Schematic			
MAX	Ip1_m3db_27	87	13673	Qp1_m3db_27	59	13676
			av_extracted			
MAX	Ip1_m3db_27	87	13275	Qp1_m3db_27	59	13270
	%errors		2.9981			3.059

COMPOSITE M.CARLO

	Parameter	Run No.	Freq. Corn.	Parameter	Run No.	Freq. Corn.
			Schematic			
MIN	I_m1p25_27	69	10618	Q_m1p25_27	25	10621
			av_extracted			
MIN	I_m1p25_27	69	10286	Q_m1p25_27	25	10280
	%errors		3.2277			3.317
			Schematic			
MAX	I_m1p25_27	2	10638	Q_m1p25_27	29	10636
			av_extracted			
MAX	I_m1p25_27	2	10284	Q_m1p25_27	29	10274
	%errors		3.4422			3.523

IX. DESIGN MEASUREMENTS AND VERIFICATION OF CLASS AB AMP.1 AND AMP.2

The I/Q baseband AMP.1 is a class AB amplifier with eight programmable 2dB variable gain steps from 3, 5, 7, 9, 11, 13, 15, and 17dB respectively. The baseband class AB AMP.2 however, is designed to have five programmable 3dB gain steps of variable gain that vary from 0, 3, 6, 9 and 12 dB, functioning as a baseband output buffer to drive the ΣΔ ADC. Class AB amplifier and buffer topologies are selected to minimize current drain under DC and AC signal conditions, while maintaining channel linearity of I/Q receiver path. To minimize flicker noise corner and "far-out" noise, the sources of transconductance FETs stages are tied to the ground in order to eliminate tail current sources. Variation of the amplifier output common-mode voltage is critical, since it affects currents, gain, noise, and linearity.

A. *Linearity Requirement*

Linearity is one of the critical parameters that limit system dynamic range in receiver path. As an amplifier approaches compresses operation, non-linear behaviors become more apparent, including increased harmonic content. Linearity is measured based on signal immunity to intermodulation (IM) interference test. The parameters considered are the second order and third order input referred as the intercept points (IIP2 and IIP3) of 2-tone input signals in dBV_{RMS}.

IMD measurements start with injecting a 2-tone sinusoidal signal into an amplifier. A perfectly linear amplifier would produce an output signal that includes two tones at the exact same frequencies as the input signal with amplified output power. However, an actual amplifier will produce additional harmonics content at frequencies other than the two input tones at the output. Second order harmonics occur at multiples of the fundamental tones such as $2f_1$ and $2f_2$, and the third order harmonics can be observed at $3f_1$ and $3f_2$. In addition, the system will produce second-order and third-order distortion products at every combination of the first-order and second-order products, $|f_2-f_1|$ and $|f_1+f_2|$. The signal content due to third-order distortion occurs directly adjacent to the two input tones at $|2f_1-f_2|$ and $|2f_2-f_1|$. The IMD measurements verify the power ratio between the power level of output fundamental tones (f_1, f_2) and 3rd-order distortion products ($2f_1-f_2$, $2f_2-f_1$).

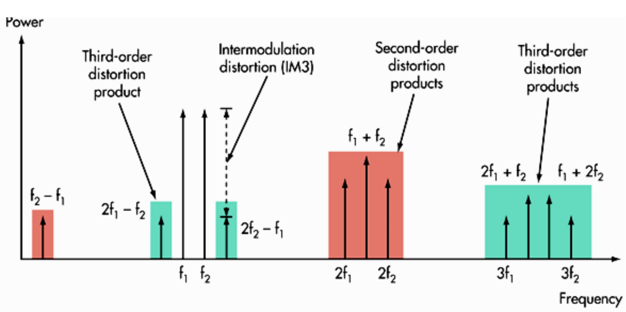

Figure 8: Nonlinear Devices Produce Harmonics Tones

Theoretically,

$$IIP_3 = \frac{(IMD)}{2} + Output\ Power \quad (1)$$

$$IP_n = P + \frac{\Delta P}{n-1} \quad (2)$$

$$IIP_2 = P_{i1} + (P_{o2} - P_{o12}) \quad (3)$$

$$IIP_2 = P_{i2} + (P_{o1} - P_{o12}) \quad (4)$$

$$IIP_3 = P_{i1} + (P_{o2} - P_{o12})/2 \quad (5)$$

$$IIP_3 = P_{i2} + (P_{o1} - P_{o21})/2 \quad (6)$$

The IP_n is the n^{th}-order intercept point, P is the fundamental frequency input power in dBV_{RMS}, and ΔP is the difference between the desired output signal to the undesired n^{th}-order output product in dBV_{RMS}. In order to measure IIP2, p_{i1} and p_{i2} represent the fundamental input power level of the tones at f_1 and f_2, p_{o1} and p_{o2} represent the output power for the tones at f_1 and f_2, and p_{o12} is the IM output power for the tone at $|f_2 \pm f_1|$. However, IIP3 is calculated with p_{o12} and p_{o21} represent IM output power for the tones measured at $|2f_1-f_2|$ and $|2f_2-f_1|$ [6].

The linearity characterization plan is to measure system IM suppression capability for all variable gains at the nominal operating frequency mode. The SPI bit is set accordingly to perform the linearity measurements for various gain and frequency settings. The system is set for 13.66 kHz operating mode with input power of 2-tone is -16dBm at f_{1IN}=26kHz and f_{2IN}=50kHz injected at all differential I/Q input pins of the baseband path. The maximum input harmonics number is set for 7 tones for wider spectrum observation. The second and third order intermodulation distortion products i.e., IMD2 and IMD3 are measured at 24kHz and 2kHz to verify its IIP2, and IIP3. Table 3 summarizes high linearity measured numbers that correspond to Figure 9 and 10 for better observation of the stability variations of IIP2 and IIP3. Similar procedures are performed to verify linearity performance at various frequency sets [7, 8]. Figure 11(a) to 11(c) show samples of measured and verified IIP2 and IIP3 of the output signals.

Table 3
Linearity Data of IIP2 and IIP3;
AMP_VGA=[000],[001],[010],[011],[100],[101],[110],[111]
=bbfamp1gain=17,15,13,11,9,7,5,3dB; bandwidth=[Mode:12]=13660Hz

bbfamp1gain=dec[7]=3dB bbfamp2gain=0 bndwdth=12=13660Hz	dBV	note	bbfamp1gain=dec[6]=5dB bbfamp2gain=0 bndwdth=12=13660Hz	dBV	note
IIP3_i	28.10	good	IIP3_i	28.11	good
IIP3_ix	28.09	good	IIP3_ix	28.11	good
IIP3_q	28.10	good	IIP3_q	28.11	good
IIP3_qx	28.09	good	IIP3_qx	28.11	good
IIP3_idiff	28.09	good	IIP3_idiff	28.11	good
IIP3_qdiff	28.09	good	IIP3_qdiff	28.11	good
IIP2_i	48.95	good	IIP2_i	50.93	good
IIP2_ix	48.95	good	IIP2_ix	50.92	good
IIP2_q	48.95	good	IIP2_q	50.93	good
IIP2_qx	48.95	good	IIP2_qx	50.92	good
IIP2_idiff	119.5	good	IIP2_idiff	117.5	good
IIP2_qdiff	119.5	good	IIP2_qdiff	117.5	good
bbfamp1gain=dec[5]=7dB bbfamp2gain=0 bndwdth=12=13660Hz	**dBV**	**note**	**bbfamp1gain=dec[4]=9dB bbfamp2gain=0 bndwdth=12=13660Hz**	**dBV**	**note**
IIP3_i	28.15	good	IIP3_i	28.22	good
IIP3_ix	28.14	good	IIP3_ix	28.2	good
IIP3_q	28.15	good	IIP3_q	28.22	good
IIP3_qx	28.14	good	IIP3_qx	28.2	good
IIP3_idiff	28.14	good	IIP3_idiff	28.21	good
IIP3_qdiff	28.14	good	IIP3_qdiff	28.21	good
IIP2_i	52.86	good	IIP2_i	54.78	good
IIP2_ix	52.85	good	IIP2_ix	54.76	good
IIP2_q	52.86	good	IIP2_q	54.76	good
IIP2_qx	52.85	good	IIP2_qx	54.78	good
IIP2_idiff	115.5	good	IIP2_idiff	113.5	good
IIP2_qdiff	115.5	good	IIP2_qdiff	113.5	good
bbfamp1gain=dec[3]=11dB bbfamp2gain=0 bndwdth=12=13660Hz	**dBV**	**note**	**bbfamp1gain=dec[2]=13dB bbfamp2gain=0 bndwdth=12=13660Hz**	**dBV**	**note**
IIP3_i	28.37	good	IIP3_i	28.65	good
IIP3_ix	28.33	good	IIP3_ix	28.6	good
IIP3_q	28.37	good	IIP3_q	28.65	good
IIP3_qx	28.33	good	IIP3_qx	28.6	good
IIP3_idiff	28.35	good	IIP3_idiff	28.63	good
IIP3_qdiff	28.35	good	IIP3_qdiff	28.63	good
IIP2_i	56.64	good	IIP2_i	58.43	good
IIP2_ix	56.61	good	IIP2_ix	58.38	good
IIP2_q	56.64	good	IIP2_q	58.43	good
IIP2_qx	56.61	good	IIP2_qx	58.38	good
IIP2_idiff	111.5	good	IIP2_idiff	109.6	good
IIP2_qdiff	111.5	good	IIP2_qdiff	109.6	good
bbfamp1gain=dec[1]=15dB bbfamp2gain=0 bndwdth=12=13660Hz	**dBV**	**note**	**bbfamp1gain=dec[0]=17dB bbfamp2gain=0 bndwdth=12=13660Hz**	**dBV**	**note**
IIP3_i	29.2	good	IIP3_i	29.86	good
IIP3_ix	29.13	good	IIP3_ix	29.83	good
IIP3_q	29.2	good	IIP3_q	29.86	good
IIP3_qx	29.13	good	IIP3_qx	29.83	good
IIP3_idiff	29.16	good	IIP3_idiff	29.85	good
IIP3_qdiff	29.16	good	IIP3_qdiff	29.85	good
IIP2_i	60.09	good	IIP2_i	61.61	good
IIP2_ix	60.03	good	IIP2_ix	61.51	good
IIP2_q	60.09	good	IIP2_q	61.61	good
IIP2_qx	60.03	good	IIP2_qx	61.51	good
IIP2_idiff	107.7	good	IIP2_idiff	105.9	good
IIP2_qdiff	107.7	good	IIP2_qdiff	105.9	good

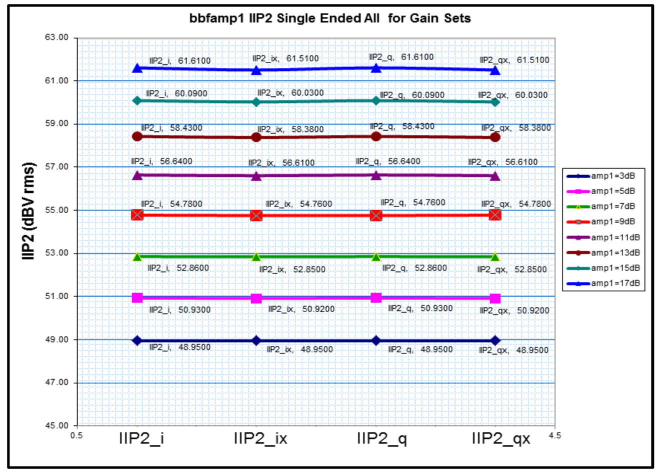

Figure 9: IIP2 Variations for Different AB. AMP.1 Gain Settings

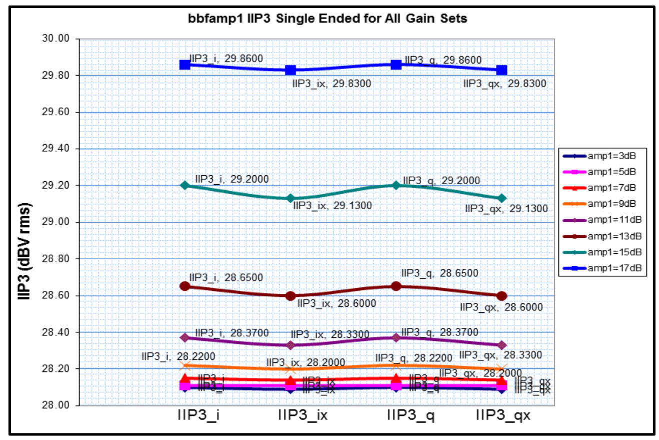

Figure 10: IIP3 Variations for Different AB. AMP.1 Gain Settings

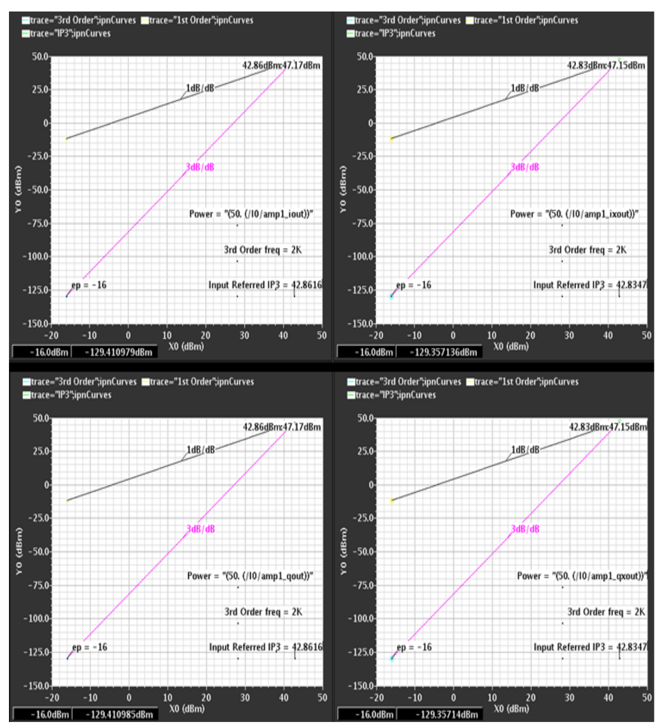

Figure 11(a): IIP3 Plots of I/Q Single Ended Output Signals

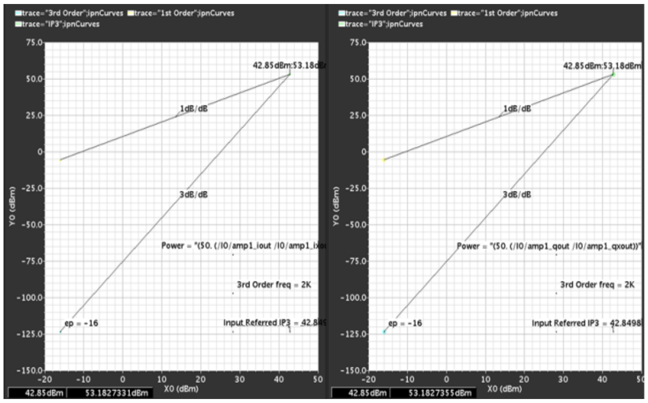

Figure 11(b): IIP3 Plots of I/Q Differential Output Signals

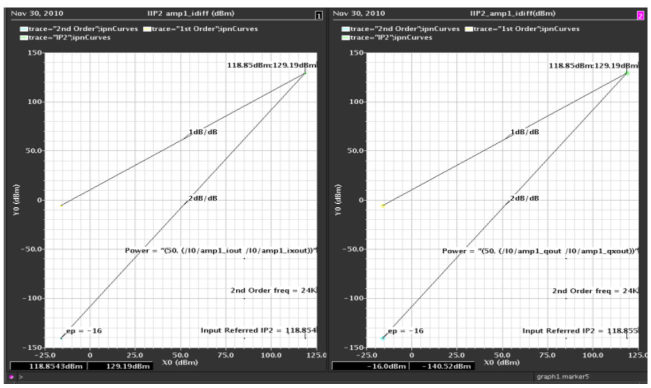

Figure 11(c): IIP2 Plots of I/Q Differential Output Signals

Similar procedures are repeated to measure IIP2 and IIP3 of AB AMP.2 at minimum (MIN) and maximum (MAX) gain settings, as shown in Table 4 for both IIP2 and IIP3 [8,9].

Table 4
AB AMP.2 Summary of IIP2 and IIP3

AMP2 Gain=Max		i/p dBm=-16
bbfamp1gain=[7]=3dB=min gain		
bbfamp2gain=[7]=12dB=max gain		
bandwidth=35=124900Hz		
	dBV	note
IIP3_i	17.9900	good
IIP3_ix	17.9900	good
IIP3_q	17.9900	good
IIP3_qx	17.9900	good
IIP3_idiff	17.9900	good
IIP3_qdiff	17.9900	good
IIP2_i	48.9500	good
IIP2_ix	48.9500	good
IIP2_q	48.9500	good
IIP2_qx	48.9500	good
IIP2_idiff	116.4000	good
IIP2_qdiff	116.0000	good

AMP2 Gain=MIN		i/p dBm=-16
bbfamp1gain=[7]=3dB=min gain		
bbfamp2gain=[0]=0dB=min gain		
bandwidth=35=124900Hz		
	dBV	note
IIP3_i	18.5600	good
IIP3_ix	18.5700	good
IIP3_q	18.5600	good
IIP3_qx	18.5700	good
IIP3_idiff	18.5700	good
IIP3_qdiff	18.5700	good
IIP2_i	36.7700	good
IIP2_ix	36.7800	good
IIP2_q	36.7700	good
IIP2_qx	36.7800	good
IIP2_idiff	106.3000	good
IIP2_qdiff	107.0000	good

B. Baseband Average Input Referred Noise RMS and Spot Noise Requirements Linearity Requirement

The baseband noise defines the lower bound for receiver system dynamic range and therefore the range is available for different modulations. This impacts the required noise and signal-handling performance, SNR. The average input referred noise RMS (IRN) is measured and calculated by using an integrating function to the input voltage referred noise power level, $V_{NIN()}^2$ from 0.1kHz to 10kHz which can be translated into numerical function as shown below.

$$IRN_{RMS} = \sqrt{\left(\int_{100}^{10000} \frac{\left(V_{NIN()}\right)^2}{(10000-100)}\right)} \tag{7}$$

$$IRN_{RMS} = sqrt((integ((V_{NIN()})^2{}_{[100\rightarrow10000]} / (10000 - 100))) \tag{8}$$

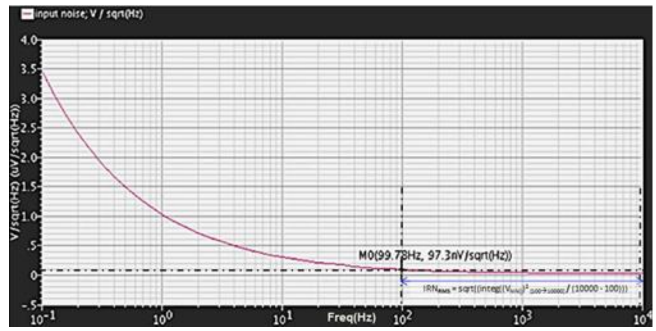

Figure 12: Total Measured IRN of I/Q Baseband Amplifier & Filter

The input referred noise is verified for each of 1-Pole, 2-Pole, AB AMP.1, and AB AMP.2 from 0.1kHz to 10kHz offset frequencies, temperature swept from 25°C to 105°C, with nominal operating BW setting. The total baseband spot noise is 85.268nV√Hz and input referred noise is 66.82 nV√Hz. The overall summary of average input referred noise within the acceptable level is shown in Table 5.

Table 5
Summary of Average Input Referred Noise RMS and Spot Noise Analysis

1-POLE Temperature	RMS Noise Average 0.1Hz-->10KHz NoiseAve nV/rtHz (RMS noise)
27degC	25.18
105degC	28.39
2-POLE Temperature	**RMS Noise Average 0.1Hz-->10KHz NoiseAve nV/rtHz (RMS noise)**
27degC	78.00
105degC	80.00
AB AMP.1 Temperature	**RMS Noise Average 0.1Hz-->10KHz NoiseAve nV/rtHz (RMS noise)**
27degC	13.00
105degC	15.00
AB AMP.2 Temperature	**RMS Noise Average 0.1Hz-->10KHz NoiseAve nV/rtHz (RMS noise)**
27degC	13.00
105degC	20.00
I/Q BBAND AMP & FILTER Temperature	**RMS Noise Average 0.1Hz-->10KHz NoiseAve nV/rtHz (RMS noise)**
27degC	60.75
105degC	61.51

The final layout of transceiver SoC has undergone such rigorous characterization routines, confirming a successful fabrication using BiCMOS-SiGe 0.18 micron technology. Figure 13 shows an overview layout of the RF transceiver SoC in QFN package. All measurements and verifications satisfy critical requirements targeted for multi-mode and multi-band SDR/DCR, compliance with TIA/EIA-TSB-84A standard as shown in Table 6 to 10 [10].

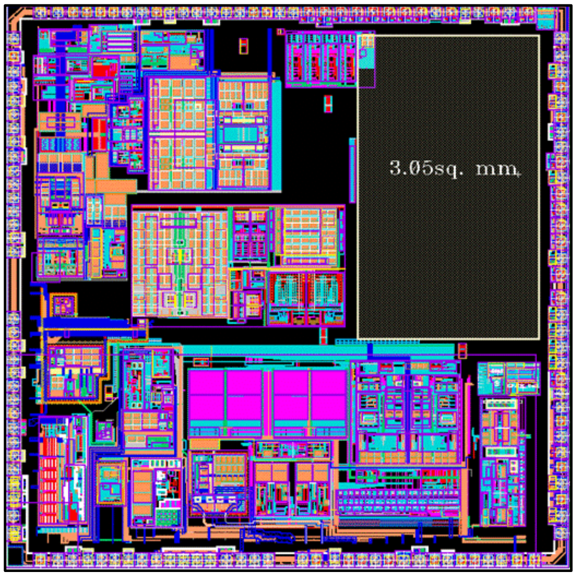

Figure 13(a): SoC Die Size = 13.25mm^2

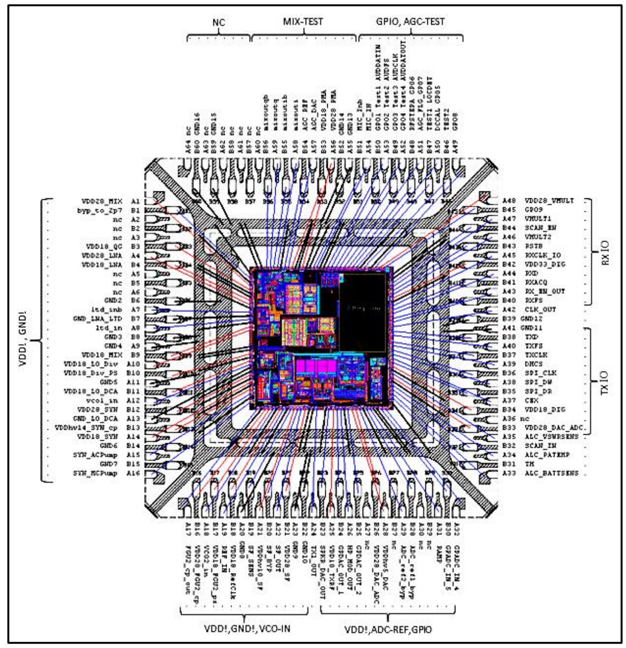

Figure 13(b): Architecture of the Verified RF Transceiver SoC in Dual Row QFN Package

Table 6
Overall Receiver Path Specifications

Receiver Path Stage	Transformer	Multiband LNA	Ring Mixer	Mixer AB Amp. 1	2-Pole LPF	Output Buffer
Typical GAIN (db)	-0.75	21dBv	-1.0	20	0	8
Type NF (db)	0.75	2.2	1.2nV/rtHz	5.5nV/rtHz	27nV/rtHz	15 nV/rtHz
IIP3 (dBm/dBV)	100	0	+18.0	+28 dBV	+40	+20 dBV
IIP2 (dBm/dBV)	1000	1000	+70dBm	+55 dBV	+95	+55 dBV
Common Mode voltage	0.65V	0.90	0.90	0.90	0.90	1.8V

Table 7
Overall 1-Pole Filter Specifications

Parameter	Conditions	Requirement Min.	Typ.	Max.	Units
Supply Voltage		2.65	2.775	3.15	V
Differential Input				1000	mVpk
Differential Output				1000	mVpk
Average Input Referred RMS Noise	BW Setting #9, 40k diff R(@105ºC)		26	29	nVrms/rtHz

Table 8
Overall 2-Pole Filter Specifications

Parameter	Conditions	Requirement Min.	Typ.	Max.	Units
Supply Voltage		2.65	2.775	3.15	V
Simulation Temperature		-40		100	º C
Operating Temperature		-30		85	º C
Gain variations for Q	Gain variations in circuit for setting Q	-20		20	%
I/Q Bandwidth Matching		-2.5		2.5	%
Filter Q Matching	Matching I/Q channels for all BW setting	-1.5		1.5	%
Filter Gain	Measured at f0/4	-0.4		0	dB
Filter Gain Accuracy	All Bandwidth Settings	-0.2		0.2	dB
I/Q Gain Matching	All Bandwidth Settings	-0.1		0.1	dB
Average Input Referred Stage RMS Noise	Bandwidth setting #9 (averaged from 0.1 Hz to f_0 of filter at 105°C)			80	nVrms/rtHz
Differential Input Signal	Off-channel signal > 2*corner freq. (2*f_0)			1000	mVpk
Differential Output Signal				500	mVpk

Table 9
AB AMPLIFIER.1 Specifications

Parameter	Requirement				
	Conditions	Min.	Typ.	Max.	Units
Supply Voltage		2.65	2.775	3.15	V
Simulation Temperature		-40		100	º C
Operating Temperature		-30		85	º C
Voltage Gain	AMP_AGC= 000		17		dB
	AMP_AGC= 001		15		dB
	AMP_AGC= 010		13		dB
	AMP_AGC= 011		11		dB
	AMP_AGC= 100		9		dB
	AMP_AGC= 101		7		dB
	AMP_AGC= 110		5		dB
	AMP_AGC= 111		3		dB
IIP2	Single Ended- Max Gain	45	75		dBVrms
	Differential- Max gain	65			
IIP3	Any gain settings	25			dBVrms
Gain Accuracy	For gains 3dB to 11dB	-0.2		0.2	dB
	For gains 13dB to 17dB	-0.2		0.2	dB
Differential Input Signal Range	Minimum gain			707	mVpk
Differential Output Signal Range				1000	mVpk

Table 10
AB AMPLIFIER.2 Specifications

Parameter	Requirement				
	Conditions	Min.	Typ.	Max.	Units
Supply Voltage		2.65	2.775	2.9	V
Simulation Temperature		-40		100	º C
Operating Temperature		-30		85	º C
Common Mode Output Voltage	Nominal conditions, 2.775V Supply		1		V
Voltage Gain	BUFGAIN[2:0]=111		12		dB
	BUFGAIN[2:0]=110		12		dB
	BUFGAIN[2:0]=101		12		dB
	BUFGAIN[2:0]=100		12		dB
	BUFGAIN[2:0]=011		9		dB
	BUFGAIN[2:0]=010		6		dB
	BUFGAIN[2:0]=001		3		dB
	BUFGAIN[2:0]=000		0		dB
IIP2	Max Gain	15	20		dBVrms
IIP3	Max Gain	8			dBVrms
Average Input Referred RMS Noise	Average from 0.1Hz to 10kHz		13	20	nVrms/rtHz
Gain Accuracy		-0.2		0.2	dB
Differential Input Signal Range	Minimum gain settings			500	mVpk
Differential Output Signal Range	All gain settings	1000			mVpk

X. CONCLUSION

This paper presented an efficient technique with comprehensive characterization of I/Q baseband path for BW selectivity and linearity performance. It is implemented by utilizing SPI Bits Controller for BW channel selectivity, amplifier gain, and linearity options to perform baseband tuning of the SoC having an on-board multiplexer for digital switching purposes by external MCU and DSP for SDR applications. This technique expedites the rigorous verification processes by maintaining data correlation and ease of measurements because it can be programmed automatically, as opposed to the most common approach by manual verifications for industrial standard validation and benchmarking. The SoC is successfully tested for its capability to perform digital multi-gain and multi-band tuning range with all critical parameters discussed in the measurements section. The architecture of the SoC has been verified by different sets of simulation tools for correlation analyses, such as transient versus harmonic balance. Post layout optimization and design trade-off are well covered where both simulation and measurement results demonstrate good robustness against PVT variations.

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