Design 4-to-1 Multiplexer Using Universal Gate with Standard Process Technology

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***Abstract*—Nowadays, CMOS is widely being used in integrated circuit design. In this project, the original 4-to-1 multiplexer schematic is redesign by changing the gate inside the multiplexer with CMOS universal gate. NAND gate will be used as the universal gate in this project. Through this project, SILVACO EDA tools are used to design the integrated circuit, schematic and layout. The schematic of NAND gate and 4-to-1 multiplexer is analyzed in order to meet the specification based on datasheet of NAND gate and 4-to-1 multiplexer. The result of the analyses can be used to determine the size of the transistors. The size of transistors can be used to design the layout of NAND and 4-to-1 multiplexer. At the end of the project, a new design of 4-to-1 multiplexer using universal gate will be produced and it meets the specification required in the datasheet of 4-to-1 multiplexer. Moreover, the equivalent layout of 4-to-1 multiplexer will also be produced.**

***Index Terms*—CMOS, gate, multiplexer, IC, ICT, R& D, wafer.**

I. INTRODUCTION

Multiplexer is known as data selectors. Multiplexer allows digital information from several sources to be routed onto single line for transmission over that line which consist of several data-input lines, single output line and data-select inputs that permit digital data on any one of the inputs to switched to the output line [1]. Basically, multiplexer acts like a digitally controlled multi-position switch where the digital code applied to the select controls which data inputs will be switched to the output [1]. For example, a multiplexer select one out of N input data sources and transmits the selected data to a single output channel.

A gate is an electronic device that produces result based on two or more input values. Universal gate is being used in digital circuit other than AND, OR and NOT. It is also implementing any gate like AND, OR and NOT or any combination of this basic gates. NAND and NOR is known as universal gates [2].

This project is about to design schematic and layout of an integrated circuit (IC) of 4-to-1 multiplexer based on CMOS universal gate. SILVACO EDA tools software is used to design the schematic and layout such as GATEWAY and EXPERT. By using GATEWAY, the characteristics of 4-to-1 multiplexer can be determined and compared with datasheet established by other company in order to meet the specifications by designing the circuit. To design the layout, EXPERT is used and the design must be equivalent with the circuit design in GATEWAY.

II. METHODOLOGY

A. Schematic Circuit Design

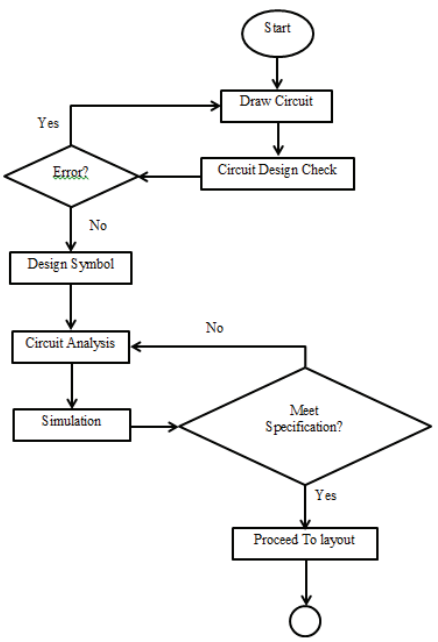

Figure 1: Process for schematic phase (GATEWAY)

Figure 1 shows the flow of the process on designing the schematic circuit. GATEWAY software from SILVACO EDA tools is used to design the schematic.

At the beginning of the process, the schematic circuit needs to be designed. The design is check in order to avoid error after connecting all the components. If error occurs, the circuit needs to be redesigned. If there is no error, proceed to design the symbol of the circuit such as in this project using the NAND gate and multiplexer symbol. Next, the symbol can be used to do the circuit analyses which were DC analysis and AC analysis [3]. The result is compared with datasheet from other company. If the results not meet the specification, the

circuit has to be analyzed again. If the results meet the specification, proceed to design the layout.

B. Layout Design

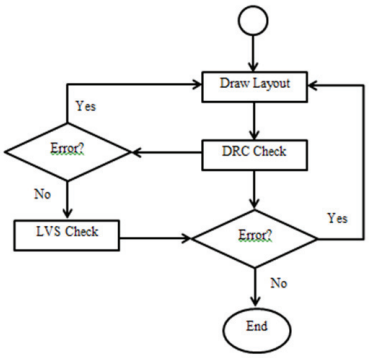

Figure 2: Process for layout phase (EXPERT)

Figure 2 shows the flow of designing the layout process. In this part, layout is designed using EXPERT software from SILVACO EDA tools.

Firstly, the layout is design based on the size of width (W) and length (L) that has been determined during the analysis. The layout needs to be checked through DRC check process. The layout is check whether it is compatible with the design rule or not. If there are errors at this level, the layout needs to be redesigned. If there are no error can proceed to LVS check process. In this process, the layout is compare with the schematic circuit that is designed previously. If there are errors, both layout and schematic needs to be check and designed again. If there are no errors, the layout is considered equivalent.

There are several steps to design 4-to-1 multiplexer as below:

1. Design NAND gate schematic
2. Design NAND gate layout
3. Design 4-to-1 multiplexer schematic
4. Design 4-to-1 multiplexer layout

C. NAND Gate Design

Based on theory of CMOS logic gate, NAND gate contain four transistors which two of it are PMOS and another two are NMOS. Design of NAND gate schematic is shown in Figure 3.

NAND gate schematic can be design using GATEWAY simulator. The selected 4-to-1 multiplexer is design based on Boolean expression. Size of the transistor will be determined through DC analysis and AC analysis which the result of the analysis are compared with datasheet of NAND gate [4]. Size of the transistor for this project is 260µm for both PMOS and NMOS of NAND gate.

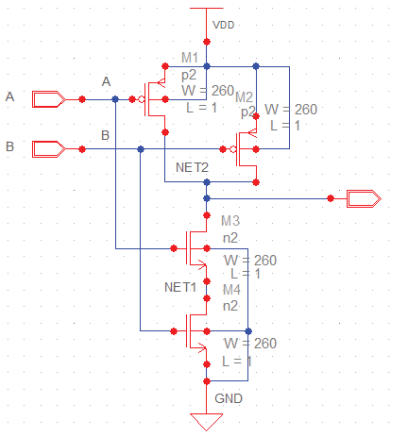

Figure 3: NAND gate schematic

EXPERT simulator is used to design layout of the NAND gate. Stick diagram can be used to determine the layout design. Although stick diagram does not represent all details of a layout but it makes some relationship much clear and it is simpler to draw. Figure 4 show the layout of NAND gate that is designed using EXPERT simulator.

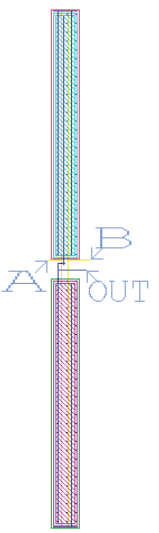

Figure 4: NAND gate layout

Layout designed will go through DRC and LVS process which DRC process will check the design based on Silterra design rules and minimize the layout while LVS process need to compared the layout design with schematic design in order to ensure the connection on the layout is correct. These processes will be gone through few times until the layout is equivalent.

D. 4-to-1 Multiplexer Design

The 4-to-1 multiplexer circuit will use the NAND gate that has been analyzed previously. Schematic circuit of 4-to-1 multiplexer will gone through the same process as previous such as DC and AC analysis in order to meet the specification in the datasheet. Datasheet that been used for the 4-to-1 multiplexer is datasheet Dual 4-Line to 1-Line Multiplexer from Philips Semiconductors.

Figure 5 show the schematic that have been redesign to follow the specification based on the datasheet which enable is used in the circuit.

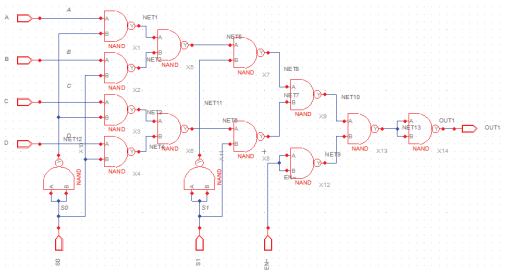

Figure 5: 4-to-1 multiplexer with enable schematic design circuit

To design 4-to-1 multiplexer layout, NAND gate layout is used and connect each layout using metal. Same processes gone through by NAND gate layout, 4-to-1 multiplexer layout will be checked through DRC process and LVS process. Figure 6 shows the layout of 4-to-1 multiplexer.

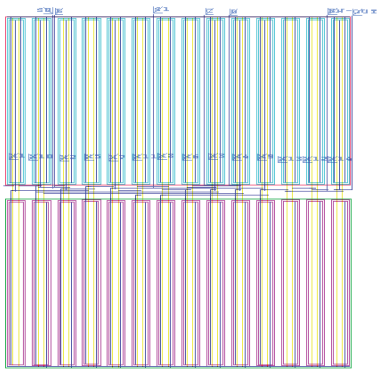

Figure 6: Layout of 4-to-1 multiplexer

III. RESULTS AND DISCUSSIONS

A. NAND Gate Analysis

From DC analysis process, voltage for input and output can be determine and compared with the datasheet for NAND gate. Below show the Voltage Transfer Curve (VTC) for VIH, VIL, VOH and VOL. Figure 7 shows the VTC of VIH and VIL. Figure 8 shows the VTC for VOH which the result is determined at highest output value. While Figure 9 shows the VTC for VOL and it is determined at lowest output voltage.

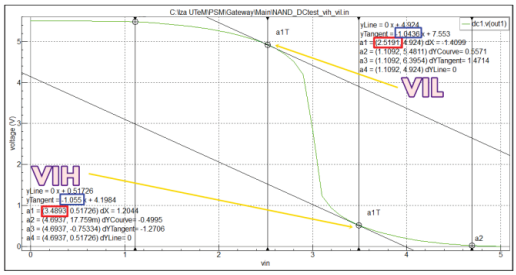

Figure 7: VTC for VIH and VIL of NAND gate

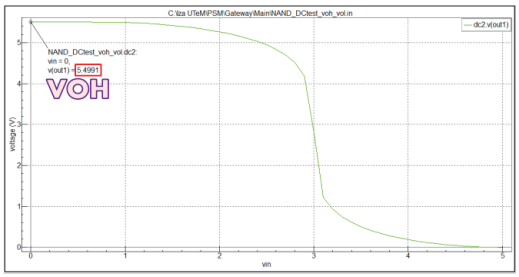

Figure 8: VTC for VOH of NAND gate

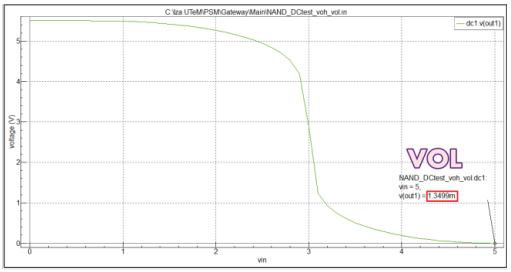

Figure 9: VTC for VOL of NAND gate

Table 1
DC Analysis Result of NAND Gate

Symbol	Test Condition		Datasheet Value (25°C)			Simulate Value	Unit
	VCC		Min	Typ	Max		
VIH	5.5V		3.85	2.75	-	3.4893	V
VIL	5.5V		-	2.75	1.65	2.5191	V
VOH	5.5V	IO= -50µ	5.4	5.49	-	5.4991	V
VOL	5.5V	IO= 50µ		0.001	0.1	0.0013	V

Table 1 showed the comparison between datasheet value and simulation value for DC Analysis of NAND gate. Based on datasheet, there are several test conditions that need to be followed in order to meet the specification. For this project

maximum DC voltage is supplied to DC analysis circuit for NAND gate. By referring to Table I, the simulation results all are in range between maximum and minimum value of datasheet. This shows that the NAND gate meets the specification as in the datasheet and can be used for the next step.

AC analysis can show input and output result and compare the result with NAND gate truth table as in Figure 10 below. As seen in the Figure 11, the result is as expected as shown in truth table. When input A low and input B low will give result for output high and vice versa. When input A low and input B high will give output high and vice versa.

A	B	out
0	0	1
0	1	1
1	0	1
1	1	0

Figure 10: NAND gate truth table

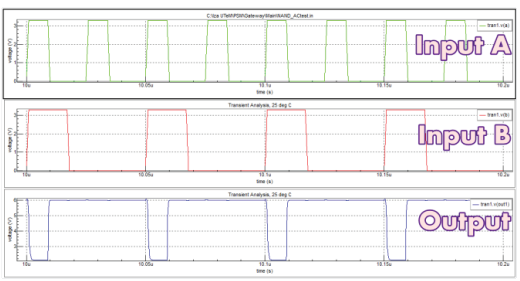

Figure 11: AC analysis graph result of NAND gate

By referring to the datasheet of NAND gate, AC analysis can determine propagation delay between input and output. Table II shows the comparison between datasheet value and simulation value.

Table 2
AC Analysis Result Of NAND Gate

Symbol	Test Condition	Datasheet Value (25°C)			Simulate Value	Unit
	VCC	Min	Typ	Max		
(A) t_{PLH}	5.5V	1.5	4	8	0.5976	ns
(A) t_{PHL}	5.5V	1.5	4	8	0.3353	ns
(B) t_{PLH}	5.5V	1.5	4	8	0.5476	ns
(B) t_{PHL}	5.5V	1.5	4	8	8.3353	ns

Referring to Table 2, simulation values are smaller than datasheet values except for t_{PHL} for input B and output. Although the simulation values are not in range but this result is still consider meet the specification because the delay is smaller. Meanwhile t_{PHL} value for input B and output is still acceptable because the difference is not too high [5].

Layout of NAND gate is designed by using transistor size that have been determine through DC and AC analysis which is 260µm for PMOS and NMOS width, while for the length is 1µm. The layout needs to go through DRC and LVS process using Expert simulator. DRC will check the layout based on Silterra design rules. Figures 12 and 13shows the DRC and LVS report after NAND gate layout is equivalent.

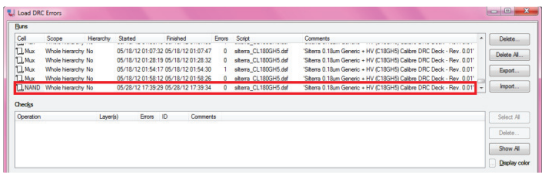

Figure 12: DRC report of NAND gate layout

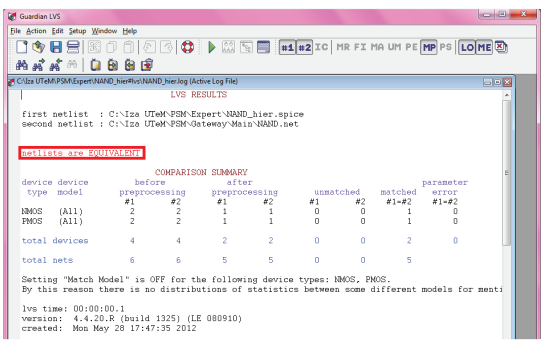

Figure 13: LVS report of NAND gate layout

B. 4-to-1 Multiplexer Analysis

Through DC analysis, voltage input and voltage output of 4-to-1 multiplexer can be determined [6]. The result will be compared with values from datasheet of 4-to-1 multiplexer that shown in Table III. Figure 14 shows the VTC for VIH and VIL of 4-to-1 multiplexer. Figure 15 shows the VTC for VOH of 4-to-1 multiplexer which it is determine at highest output voltage. Figure 16 shows the VTC for VOL of 4-to-1 multiplexer which it is determine at lowest output voltage.

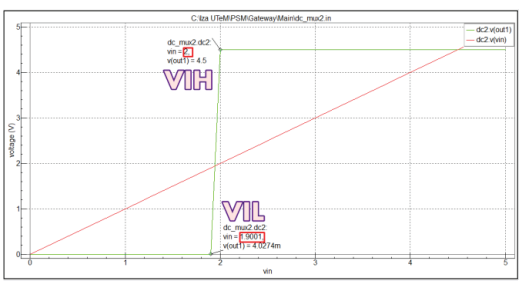

Figure 14: VTC for VIH and VIL of 4-to-1 multiplexer

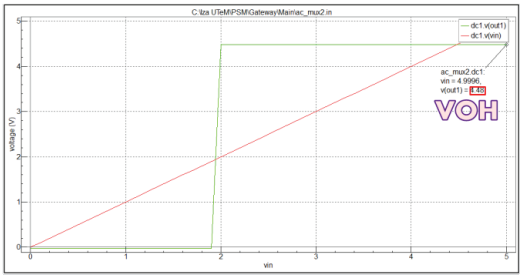

Figure 15: VTC for VOH of 4-to-1 multiplexer

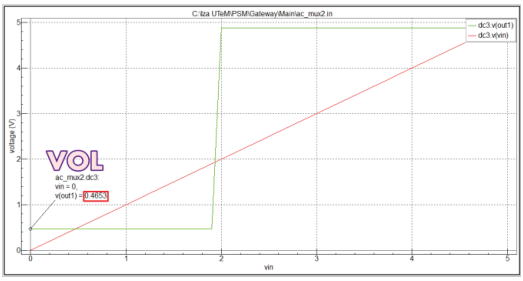

Figure 16: VTC for VOL of 4-to-1 multiplexer

There is test condition that needs to be followed in order to do the DC analysis of 4-to-1 multiplexer which is to supply current to DC analysis circuit of 4-to-1 multiplexer [7]. To determine VOH, -1mA current is used. While to determine VOL, 20mA is used.

By referring to Table III, simulation results for 4-to-1 multiplexer are all in range of datasheet values. For VIH, the value for simulation is exactly the same as datasheet value. While for VIL, VOH and VOL values are not exceed the maximum or the minimum values of the datasheet. This means the multiplexer is has meet the specifications.

Table 3
DC Analysis Result Of 4-To-1 Multiplexer

Symbol	Test Condition	Datasheet Value (25ºC)			Simulate Value	Unit
		Min	Typ	Max		
VIH	VCC = 4.5V	2.0	-	-	2.0000	V
VIL	VCC = 4.5V	-	-	0.8	1.9001	V
VOH	VCC = 4.5V, IOH=-1mA	2.7	3.4	-	4.2542	V
VOL	VCC = 4.5V, IOL = 20mA		0.30	0.50	0.4947	V

4-to-1 multiplexer circuit design will go through AC analysis and Figure 17 shows the result of AC analysis in graph. There are four inputs A, B, C and D, one input Enable (En) and two inputs Selector (S0, S1). This result can be compared with 4-to-1 multiplexer truth table for enable active low in Figure 18 to ensure the result is correct.

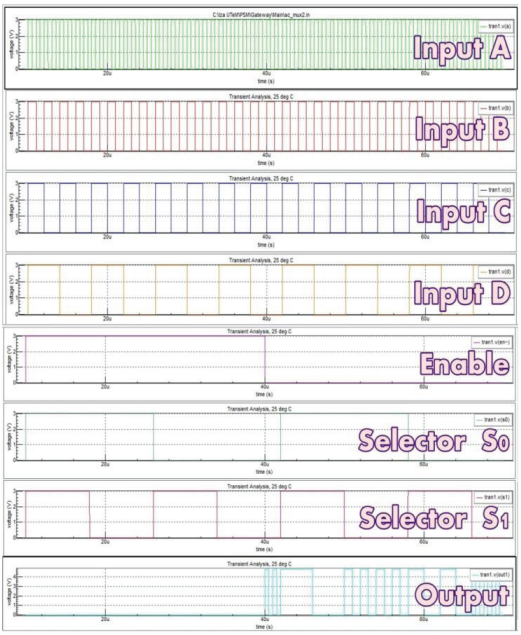

Figure 17: AC analysis graph result of 4-to-1 multiplexer

S_1	S_0	E	Output
X	X	1	Z
0	0	0	Input 0
0	1	0	Input 1
1	0	0	Input 2
1	1	0	Input 3

Figure 18: 4-to-1 multiplexer truth table

Based on Table 4, the simulation values are much smaller compared to the datasheet values. This means that, the output for this 4-to1 multiplexer design can give faster respond to signal changes at the input under condition of 5.0V voltage, 50pF capacitor, 500Ω resistor and temperature of 25°C. Simulations values give better result compared to datasheet values.

Previous NAND gate layout design is used to design 4-to-1 multiplexer. 14 copies of NAND gate layout is rearranged to get the smallest area to use. The connection between each NAND gate is followed as in the schematic design. To ensure the design is satisfies with the recommended parameters, the design have to go through DRC process which to check the design by compare the design with the design rule produce by Silterra. The report of DRC is shown in Figure 19. The result shows that the layout design has no error.

Table 4
DC Analysis Result Of 4-To-1 Multiplexer

Symbol	Test Condition	Datasheet Value (25°C)			Simulate Value	Unit
		Min	Typ	Max		
(A) T_{PLH}	VCC=5.0V, C_L=50PF, R_L=500Ω	3.0	4.5	7.0	3.2216	NS
(A) T_{PHL}	VCC=5.0V, C_L=50PF, R_L=500Ω	3.0	5.0	7.5	2.2402	NS
(B) T_{PLH}	VCC=5.0V, C_L=50PF, R_L=500Ω	3.0	4.5	7.0	3.6803	NS
(B) T_{PHL}	VCC=5.0V, C_L=50PF, R_L=500Ω	3.0	5.0	7.5	1.9063	NS
(C) T_{PLH}	VCC=5.0V, C_L=50PF, R_L=500Ω	3.0	4.5	7.0	4.2850	NS
(C) T_{PHL}	VCC=5.0V, C_L=50PF, R_L=500Ω	3.0	5.0	7.5	2.2191	NS
(D) T_{PLH}	VCC=5.0V, C_L=50PF, R_L=500Ω	3.0	4.5	7.0	3.1702	NS
(D) T_{PHL}	VCC=5.0V, C_L=50PF, R_L=500Ω	3.0	5.0	7.5	1.8841	NS
(EN) T_{PLH}	VCC=5.0V, C_L=50PF, R_L=500Ω	5.0	7.5	9.0	0.9220	NS
(EN) T_{PHL}	VCC=5.0V, C_L=50PF, R_L=500Ω	4.0	5.5	7.0	3.6014	NS
(S0) T_{PLH}	VCC=5.0V, C_L=50PF, R_L=500Ω	5.0	8.0	10.5	3.2064	NS
(S0) T_{PHL}	VCC=5.0V, C_L=50PF, R_L=500Ω	5.0	8.0	10.5	2.0262	NS
(S1) T_{PLH}	VCC=5.0V, C_L=50PF, R_L=500Ω	5.0	8.0	10.5	2.7155	NS
(S1) T_{PHL}	VCC=5.0V, C_L=50PF, R_L=500Ω	5.0	8.0	10.5	2.1177	NS

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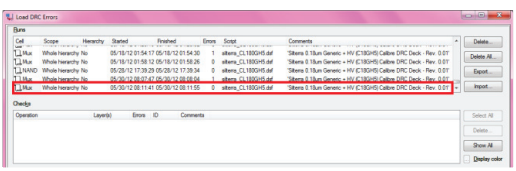

Figure 19: DRC report of 4-to-1 multiplexer

To ensure the connections are correct between schematic and layout, this layout design must go through LVS process. The report of LVS in Figure 20 shows that the result of the layout is equivalent with the schematic design. Figure 21 shows the layout of 4-to-1 multiplexer which added ports input, output, VDD and GND. This design can be used for the fabrication on wafer.

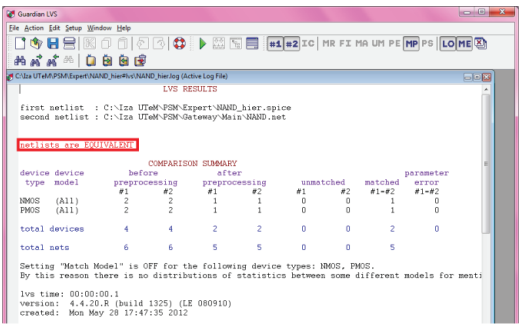

Figure 20: LVS report of 4-to-1 multiplexer

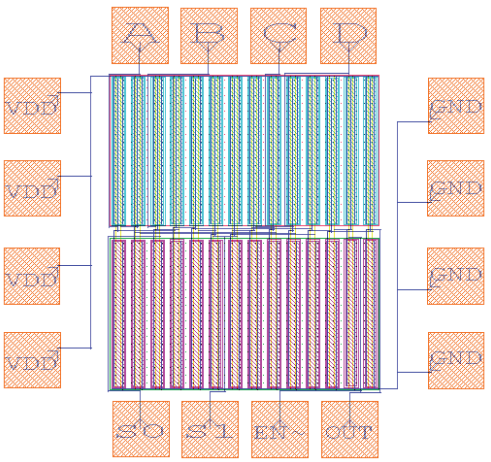

Figure 21: Layout of 4-to-1 multiplexer

IV. Conclusion

The main task of this project is to design a 4-to-1 multiplexer using universal gate with standard process technology. The universal gate that is used in this project is NAND gate. The NAND gate is analyzed through DC and AC analysis in order to find the size for the transistors using GATEWAY simulator in SILVACO EDA tools. The analysis is compared with datasheet of NAND gate which is Quad 2-input NAND Gate from STMicroelectronic. After the analysis, the size transistor that is suitable is 260µm of width and 1µm of length for both PMOS and NMOS. Then, the layout of NAND gate is designed using EXPERT simulator. The size of the transistor is applied in designing the layout. There are two

process during layout analysis which is DCR and LVS process. Through both process, the NAND gate design is equivalent without any error.

In designing the 4-to-1 multiplexer, the NAND gate that successfully analyzed will be used. A 4-to-1 multiplexer goes through the same analysis and process for both schematic and layout. The design of 4-to1 multiplexer also meet the specification based on datasheet used which is Dual 4-Line to 1-Line Multiplexer from Philips Semiconductors. The layout designed of 4-to-1 multiplexer also equivalent with its schematic without any error. Thus, a design of 4-to-1 multiplexer using universal gate with standard process technology was done successfully without any error for all analysis and process for both NAND gate and 4-to-1 multiplexer.

ACKNOWLEDGMENT

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