

# Comparison of electrical characteristics between Bulk MOSFET and Silicon-on-insulator (SOI) MOSFET

M.N.I.A.Aziz, F.Salehuddin, A.S.M.Zain, K.E.Kaharudin, S.A.Radzi  
Centre for Telecommunication Research and Innovation (CeTRI)  
Faculty of Electronics and Computer Engineering (FKEKK)  
Universiti Teknikal Malaysia Melaka (UTeM), Malaysia  
fauziyah@utem.edu.my

**Abstract**— Conventional MOSFET has already passed lower than 45nm transistor fabrication. As silicon is now hitting the atomic resolution and reaching its physical and electrical limitation, producing a proper working transistor tends to be more difficult and complicated. The major challenge is to fabricate a transistor with a nominal threshold voltage ( $V_{TH}$ ), lower gate leakage current ( $I_{OFF}$ ) and lower drain induced barrier lowering (DIBL). To overcome these problems, Silicon-on-insulator (SOI) MOSFET has been proposed, and it is believed to be capable of suppressing short channel effects (SCEs) by burying oxide layer in the silicon substrate. ATHENA and ATLAS module of SILVACO software were used in simulating the virtual fabrication and electrical performance of the transistors. An investigation on the characteristics and performance of the devices has been conducted in order to compare their electrical characteristics. The MOSFET structure was constructed by utilizing SILVACO Athena module, and the electrical characteristics were simulated using SILVACO Atlas module. The results of both the conventional bulk MOSFET and the SOI MOSFET were analyzed. It was observed that SOI MOSFET was superior compared to the conventional MOSFET in terms of their overall electrical characteristics.

**Index Terms**— MOSFET, Silvaco, DIBL, Athena, SOI

## I. INTRODUCTION

Metal-Oxide Semiconductor Field Effect Transistor (MOSFET) is a device that has been widely used in the industry. These devices are, such as the digital circuit, microprocessor and memory circuit industry. MOSFET is used as a switch to amplify the electronic signal. The integrated circuit (IC) comprises million numbers of MOSFET devices due to their small size characteristic, and this feature is another advantage of this device to the electronic industry in the world [1,2]. MOSFET technology is well-known in the industry, especially for switching application. It has been used widely since the early 60-70s. There have been a lot of gains in the performance of the MOSFET device since their size dimension keeps decreasing. [1].

The cost and size are the main attributes of MOSFETS devices. Since the technology is well established, the fabrication process of MOSFET device has experienced a great decrease in cost. Due to their small physical attribute and low cost, MOSFET devices are mainly used in developing CMOS logic chips. At present, MOSFET technologies have

become the heart of every computer. Thus, a new technology has been introduced to optimize the performance of MOSFET device. With the presence of Buried oxide (BOX) layer, the characterization of MOSFET can be enhanced, thus, it speeds up the performance of the MOSFET device. This technology is known as Silicon-on-insulator MOSFET or SOI MOSFET.

Short channel effect (SCE) of Silicon-on-insulator (SOI) MOSFET is tremendously suppressed as it has been proven theoretically and experimentally by many researchers. The superiority of SOI is mainly due to the dependency on film thickness, body and back gate (substrate) biases. This dependency enables a superior control of drain bias, carrier velocity saturation, channel length modulation and its effect on out conductance, as well as devices degradation due to the channel effect immunity to SOI MOSFETS. The use of SOI MOSFET in VLSI circuits provides the designer with additional flexibility compared to the bulk-MOSFET design [3]. The short body effect in the SOI MOSFET has been split into various instances, which are the Threshold Voltage Reduction, Drain-Induced Conductivity Enchantment (DICE) and Velocity Saturation and Channel-Length Modulation [3,4].

One of the advantages of silicon-on-insulator (SOI) MOSFET over their bulk silicon counterparts is its ability to operate in a very high-speed switching due to its lower parasitic capacitances. In order to increase the drive current available from the transistors for the purpose of obtaining the highest possible speed, it is necessary to set the threshold voltage to the lowest value. This would easily enable the transistors to be turned off; thus, reducing the slope of the sub threshold characteristics. This outcome can be expressed as the change in gate voltage required reduces the drain current by an order of magnitude. The slope of the subthreshold is regarded as an important figure of merit for a MOSFET device [5,6].

## II. RESEARCH METHODOLOGY

The structures of SOI MOSFET and Conventional Bulk MOSFET have been designed using the Technology Computer

Aided Design (TCAD) tool, which is known as SILVACO International. Specifically, the structure of MOSFET device was developed using Athena module, and the analysis of electrical characteristic was done using Atlas module.

After completing the literature study about the Bulk MOSFET and SOI MOSFET, both structures were virtually fabricated using Athena tool. The electrical characteristics of these two devices were then compared and analyzed. The graphs were plotted in order to compare the electrical characteristic of the Bulk MOSFET and SOI MOSFET. Graph of  $I_D$ - $V_G$  curve was produced to allow an extraction of the value of subthreshold voltage and threshold voltage of both MOSFET devices. Meanwhile, the  $I_D$ - $V_D$  curve was produced to measure the value of leakage current. From the graph, the differences of performance between the SOI MOSFET and Bulk MOSFET can be recognized. Fig. 1 shows the flowchart of how the SOI MOSFET had been virtually fabricated. For the Bulk MOSFET, the BOX formation was excluded from the virtual fabrication process [7].

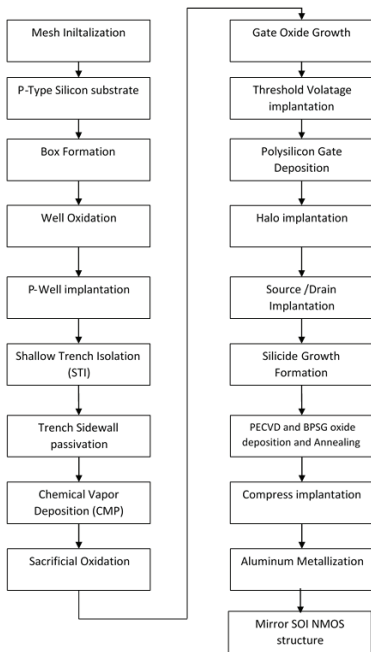


Figure 2: SOI structure.

### III. RESULTS AND DISCUSSION

There are three important characteristics of the conventional Bulk MOSFET and Silicon-on-insulator (SOI) MOSFET that were compared, which are the Leakage current ( $I_{OFF}$ ), Drive Current ( $I_{ON}$ ) and Sub-threshold voltage swing. These electrical characteristics indicate the performance of MOSFET devices in terms of their SCEs suppression, switching speed and driving capability.

#### A. Structure of Bulk and SOI MOSFET

Figure 3 shows the structure of Bulk MOSFET without SOI.

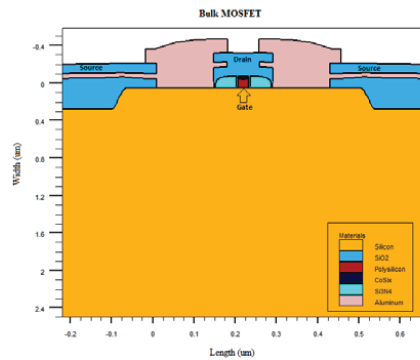


Figure 3: Structure of Bulk MOSFET

Meanwhile, Fig. 4 shows the structure of SOI MOSFET. The buried oxide layer with 100nm thickness is formed in this MOSFET structure. This MOSFET contains silicon, silicon dioxide, polysilicon, silicon nitride, cobalt nitride and aluminium. Doping concentration is one of the significant elements that determines the electrical characterization of the MOSFET device [8,9].

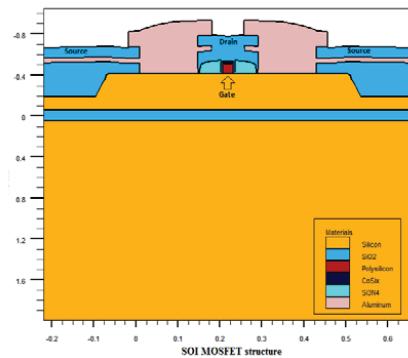


Figure 4: Structure of 100nm SOI MOSFET

#### B. Electrical characteristic of Bulk MOSFET and SOI MOSFET.

Fig. 5 depicts the  $I_D$ - $V_{DS}$  characteristics for different applied gate voltage ( $V_G$ ) in bulk MOSFET device. Four different values of gate voltage, which are 0.5V, 1.0V, 1.5V and 2.0V have been swapped in order to observe the relation between drain current ( $I_D$ ) and gate voltage ( $V_G$ ). Based on the graph, it was observed that the drain current ( $I_D$ ) was proportionate with the gate voltage ( $V_G$ ). The higher gate voltage ( $V_G$ ) is, the higher the drain current ( $I_D$ ) will be [10]. Hence, the bulk

MOSFET device has met the expected  $I_D$ - $V_{DS}$  characteristics.

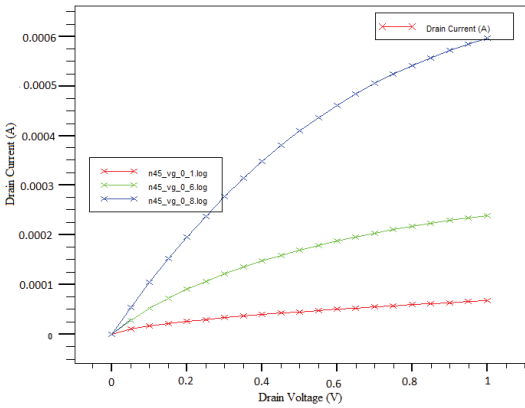


Figure 5: Graph  $I_D$ - $V_D$  for Bulk MOSFET.

It was observed that the value of threshold voltage for this bulk is 0.2879V and this value was closer to 0.289V of ITRS value [11]. Fig. 7 shows the value of  $I_{ON}$  and  $I_{OFF}$  for the device of Bulk MOSFET. Specifically, the transistors should have a high drive current and a low sub-threshold voltage swing in order to increase the switching speed of the MOSFET device [12,13].

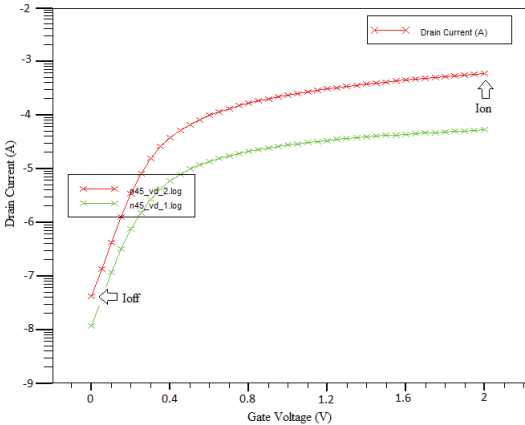


Figure 6:  $I_{ON}$  and  $I_{OFF}$  level for Bulk MOSFET

Figure 7 shows the precise electrical characteristic values of bulk MOSFET. It can be seen that the  $I_{ON}$  values of this bulk MOSFET was  $596.71\mu A/\mu m$ , while the  $I_{OFF}$  value was  $41.36nA/\mu m$ . The Sub-threshold Swing ( $Sub_{VT}$ ) value was also displayed in Fig. 8, where the value is  $97.42mV/decade$ .

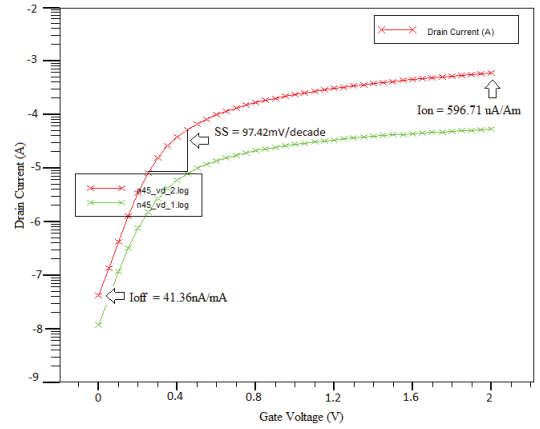


Figure 7: Electrical characteristic of bulk MOSFET.

Fig. 8 shows the characteristic of the curve of Silicon on insulator (SOI) MOSFET device. This will ensure us that our structure is indicated by the MOSFET structure.

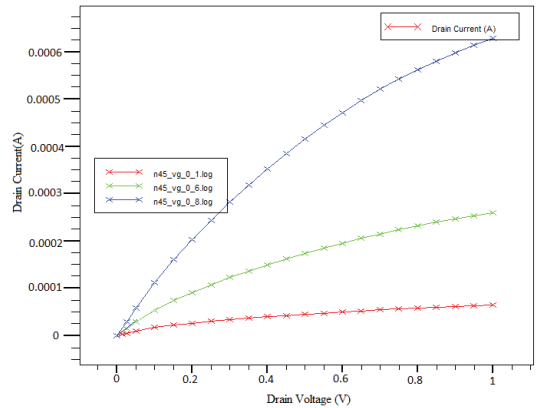


Figure 8: Graph  $I_D$ - $V_D$  for SOI MOSFET.

The threshold voltage ( $V_{TH}$ ), state ON current ( $I_{ON}$ ) and state OFF Current ( $I_{OFF}$ ) can be extracted from this curve as shown in Fig. 9.

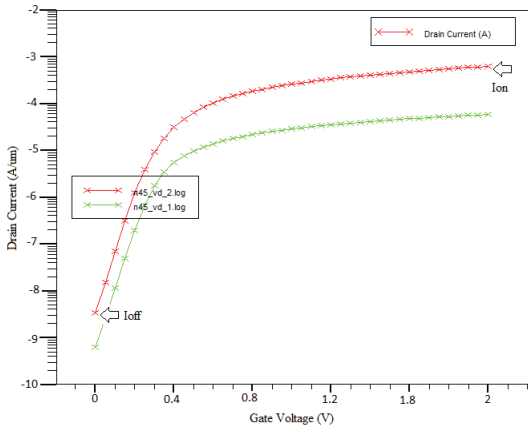


Figure 9:  $I_{ON}$  and  $I_{OFF}$  level for SOI MOSFET

Fig. 10 shows electrical characteristic of 100nm Silicon on Insulator (SOI) MOSFET device. The value of  $I_{ON}$  in this device is  $628.4\mu A/\mu m$ . The value of  $I_{OFF}$  is very low compared to the bulk MOSFET, which is  $3.364\mu A/\mu m$ . The threshold voltage of the 100nm SOI MOSFET is also closer to ITRS 2011 value, which is  $0.2902V$ , whereas, the sub-threshold swing value is  $74.62mV/decade$ .

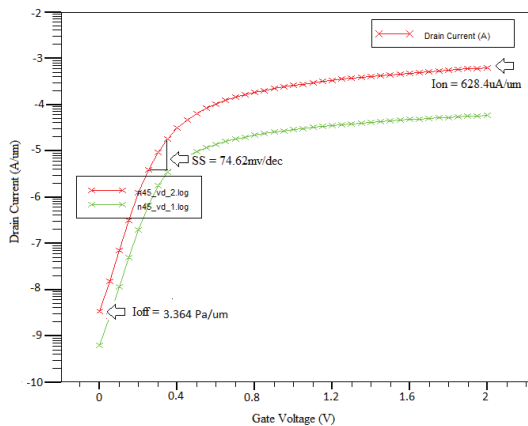


Figure 10: Characteristic value of SOI MOSFET.

Fig. 11 shows the comparison between the bulk MOSFET and SOI MOSFET devices in electrical characteristic. Silicon on insulator (SOI) MOSFET has a lot of improvements from the aspect of electrical characteristic towards the bulk MOSFET.

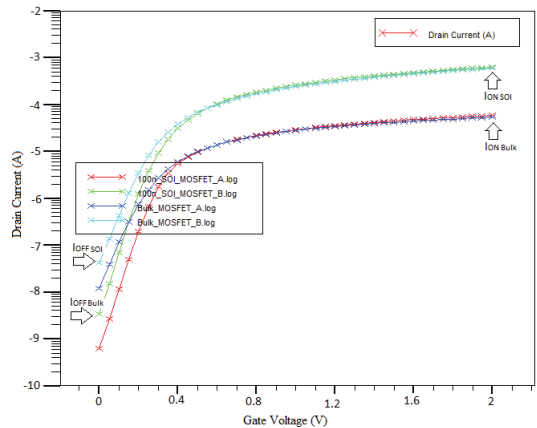


Figure 11: Electrical characteristic value comparison between bulk and SOI MOSFET devices.

Based on Table 1, the values of subthreshold swing for SOI and conventional bulk MOSFET are  $74.62mV/decade$  and  $97.42mV/decade$  respectively. The results show that the sub-threshold swing of SOI MOSFET is smaller than the conventional bulk MOSFET. It also shows that the SOI MOSFET can make faster transition between the off (low current) and the on (high current) states [12].

Table 1  
Comparison between SOI MOSFET and Conventional Bulk MOSFET

Response characteristic	SOI MOSFET	Conventional MOSFET
$V_{TH}$	0.2902 V	0.2879 V
$Sub_{VT}$	74.62 mV/decade	97.42 mV/decade
$I_{ON}$	628.4 $\mu A/\mu m$	596.71 $\mu A/\mu m$
$I_{OFF}$	3.336 $\mu A/\mu m$	41.36 $\mu A/\mu m$

#### IV. CONCLUSION

This paper emphasizes the investigation and comparison of electrical characteristics between the Conventional Bulk MOSFET device and Silicon-on-insulator (SOI) MOSFET device. The analysis of the results shows that the electrical characteristic of the SOI MOSFET was much better than the conventional Bulk MOSFET device. The presence of buried oxide (BOX) in SOI MOSFET device is capable of reducing the charge sharing between the source region and drain region, thereby increasing the drive current ( $I_{ON}$ ). As a result, the leakage current ( $I_{OFF}$ ) of SOI MOSFET device is reduced as it indicates a better suppression of short channel effects (SCEs). The Sub-threshold voltage swing ( $Sub_{VT}$ ) of SOI MOSFET device was observed to be lower than the conventional Bulk MOSFET device. The low sub-threshold voltage swing ( $Sub_{VT}$ ) is desired in order to attain faster switching speed operation.

ACKNOWLEDGMENT

The author would like to thanks to the Ministry of Education (MOE) for sponsoring this work under project (PJP/2014/FKEKK(6B)/S01341) and Faculty of Electronics and Computer Engineering (FKEKK), Universiti Teknikal Malaysia Melaka (UTeM) for the moral support throughout the project.

REFERENCES

- [1] B. Mehandia, "Study of Electrical Characteristics of SOI MOSFET Using Silvaco TCAD Simulator," Vol. 1, pp. 15–18, 2012.
- [2] A. Wei, "Effect of floating-body charge on SOI MOSFET design," *Electron Devices, IEEE*, Vol. 45(2), pp. 430–438, 1998.
- [3] S. Veeraraghavan and J. Fossum, "Short-channel effects in SOI MOSFETs," *Electron Devices, IEEE*, Vol. 36(3), pp. 522–528, 1989.
- [4] J. Colinge, "Reduction of kink effect in thin-film SOI MOSFETs," *Electron Device Lett. IEEE*, pp. 88–90, 1988.
- [5] J. Davis and A. Glaccum, "Improved subthreshold characteristics of n-channel SOI transistors," *Device Letter. IEEE*, No. 10, pp. 4–6, 1986.
- [6] M. Yoshimi and M. Takahashi, "Analysis of the drain breakdown mechanism in ultra-thin-film SOI MOSFETs," *Electron Devices*, Vol. 37(9), pp. 2015–2021, 1990.
- [7] A. Kumar, N. Kar, A. Jaiswal, and A. Kar, "Characterization of SOI PMOSFET using Silvaco TCAD Tools," *IJAIEM org*, Vol. 2(6), pp. 540–546, 2013.
- [8] Nasaruddin Mohammad, F.Salehuddin, H.A.Elgomati, I.Ahmad, N. Amizan Abd Rahman, Maria Mansor, Zulkifli Mansor, K.E.Kaharudin, A.S.Mohd Zain, N.Z.Haron, "Characterization & Optimization of 32nm P-Channel MOSFET Device," *Journal of Telecommunication, Electronic and Computer Engineering*, Vol. 5(2), pp. 49-53, 2013.
- [9] F. Salehuddin, I. Ahmad, F.A.Hamid, A.Zaharim, U.Hashim, P.R.Apte, "Optimization of input process parameters variation on threshold voltage in 45nm NMOS device," *Int. Journal of the Physical Sciences*, Vol. 6(30), pp. 7026-7034, 2011.
- [10] K.E.Kaharudin, A.H.Hamidon, F.Salehuddin, "Design and Optimization Approaches in Double Gate Device Architecture," *Int. Journal of Engineering and Technology (IJET)*, Vol. 6(5), pp. 2070-2079, 2014.
- [11] ITRS 2011 Report, <http://www.itrs.net>
- [12] I. Ferain, C. a Colinge, and J.-P. Colinge, "Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors," *Nature*, Vol. 479(7373), pp. 310–316, 2011.
- [13] K.E.Kaharudin, A.H.Hamidon, F.Salehuddin, "Impact of Height of Silicon Pillar on Vertical DG-MOSFET Device," *Int. Journal of Computer, Information, Systems and Control Engineering*, Vol. 8(4), pp. 583-587, 2014.

