Analysis of Crosstalk Noise for 2π RC Model considering Interconnect Parameters in Deep Sub-micron VLSI Circuit

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***Abstract*— As the technology enters into deep sub-micron region, signal integrity is becoming a very crucial parameter. In order to deal with the challenges associated with signal integrity problem, such as, crosstalk noise and delay, estimation and minimizing techniques should be addressed with great importance. Along with this, the peak noise amplitude and noise width values in the sensitive node must be verified and confirmed that they are below the certain threshold levels. Hence, for a particular range of frequency, an accurate and efficient crosstalk noise estimation model is necessary to confirm the signal integrity. Therefore, this work aims to analyse the crosstalk noise between two interconnect lines using 2π RC model, and considering its physical parameters, such as the parasitic capacitance, resistance and inductance and interconnect parameters, specifically the spacing between two interconnects, length, width, thickness, height from substrate in deep sub-micron VLSI circuit. In this paper, analytical expressions for peak noise amplitude and noise width in 2π model with RC interconnects for unit step input were derived, and then it was simulated in MATLAB and HSPICE software platform. The MATLAB based results represent that 2π model possesses less errors, and showed better performance compared to some other popular models by adjusting the interconnecting parameters for any certain range of operating frequency. The HSPICE simulation justifies the accuracy of the approach with full satisfaction.**

***Index Terms*— Deep sub-micron; VLSI; Interconnects; Crosstalk noise; 2π RC model.**

I. INTRODUCTION

The design of powerful and flexible processors has become possible due to development of integrated circuit (IC), which provides highly intelligent and versatile devices. ICs are fabricated using hundreds of thousands of transistors in a single chip, and they usually fall under the category of very large scale integration (VLSI). VLSI circuits have entered into deep sub-micron (DSM) design phase, which introduces transistors having smaller feature size of millimetre range and faster switching rate. The technologies having the feature sizes less than 0.25 µm are considered as DSM technology, which provides a big scope to implement things that were impossible before. The capability of IC has exponentially increased by following Moor's Law, which also helps in the factors such as computational power, resulting in the reduction of the area of IC. Because of the small feature size and high number of IC in a single chip, maintaining signal integrity and reliability becomes the main design issue in DSM technology [1]. A digital signal having fast transitions, valid and stable logic levels, accurate placement in time, free of any transient and reliable high-speed data transmission is known as signal integrity of any digital system [2].

In this paper, we focus on the signal integrity. The interconnect lines, assumed to be isolated can interfere with one another. This interference is due to the density of integrated circuits and the particular interference that are caused by parasitic coupling defined as crosstalk.

The crosstalk noise and crosstalk delay are the main concerns of crosstalk problem, in which a signal transmitted on one circuit or channel of a transmission system creates an undesired effect in another circuit or channel [3]. Usually the undesired capacitive, inductive or conductive coupling from one circuit, part of a circuit, or channel, to another causes this phenomenon on the ICs [4] [5] [6]. Figure 1 shows the two-parallel coupled transmission lines. In these lines, the wire that produces signal integrity is called 'aggressor line' and it is the one affected by this problem is called 'victim line'. Coupling capacitance virtually exists only between these two lines, and capacitive crosstalk is localized.

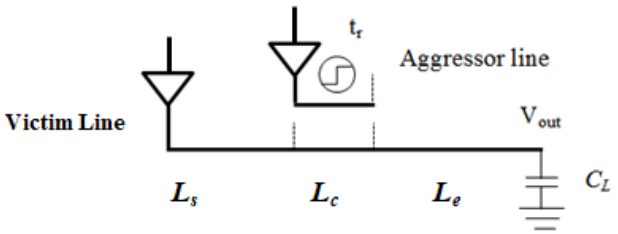

Figure 1: Two parallel coupled transmission line [7].

The crosstalk due to capacitive coupling affects both delay and signal integrity [8]. To minimize the crosstalk noise for increasing system integrity in transmission line, several models, such as, Devgan's model [9], Vittal's model [10], Heydari's model [11], Kuhlmann's model [12], Lumped model [13], 2π model [7] have already been proposed. Among them 2π Model possesses comparatively better performance in high frequency operation. Along with that, some researchers performed crosstalk minimization depending on the material used in the structure of the transmission model, such as silicon dioxide [14] [15] [16], while others used Carbon Nanotube interconnects to find the solution to reduce crosstalk [17], However, most of the

authors did not show any explicit relations with interconnect parameters in their papers. Thus, the main objective of this work is to estimate the crosstalk noise in 2π model RC interconnects, considering the calculation of noise amplitude and the width of the noise with respect to different parameters of interconnects, such as, length, width, thickness, height from substrate and spacing between two interconnects. For this purpose, analytical estimation and simulation using MATLAB and HSPICE software platform were conducted. The other objective of this work is to compare the results of this 2π RC model with the results of other models mentioned earlier. It reveals that 2π RC model is more effective and less complicated to implement than the other models.

II. MATERIALS AND METHODS

We first present the 2π model for the estimation of crosstalk noise at the victim line, and then derive the analytical expressions for peak noise amplitude and noise width for unit step input at aggressor line, taking into account the substrate and coupling capacitance. We ccalculated the peak noise amplitude and noise width using MATLAB (R2012b) software platform, and then simulated 2π model based circuit using HSPICE software platform.

As shown in Figure 1, let the aggressor shown voltage pulse at the coupling location be a unit step input with transition time being t_r, and the interconnect length of the victim line before the coupling, at the coupling and after the coupling be L_s, L_c and L_e, respectively.

The 2π model is generated, as shown in Figure 2, to compute the crosstalk noise at the receiver [18]. The victim driver is modelled by effective resistance R_d. The coupling capacitance between aggressor and victim lines are modeled by C_x. And the aggressor and victim line is modeled by other RC parameters, such as, C_1, R_s, C_2, R_e and C_L. The coupling node (node 2) is set to be the centre of the coupling portion of the victim line.

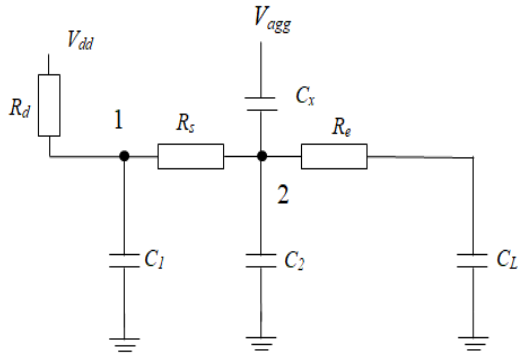

Figure 2: Crosstalk 2π RC noise model [18].

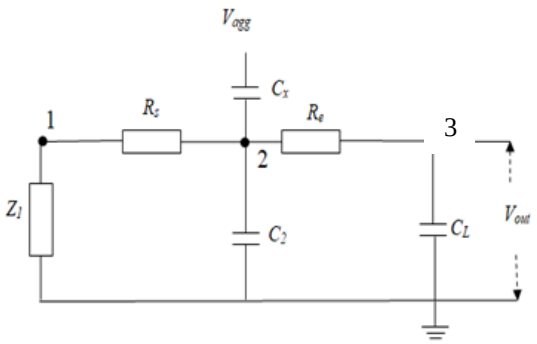

Figure 3: Modified circuit of 2π RC noise model of Figure 2.

This reduction of 2π model is very useful while calculating the value of crosstalk noise at the receiver end. This model contains two π type RC circuits, known as 2π RC model. One RC circuit is located before the coupling and the other is after the coupling. The resulting 2π RC model is solved analytically in [18]. From Figure 3, we have the impedance at node 1, Z_1 satisfying the following relation

$$Z_1 = R_d \parallel X_{c1}$$

$$\Rightarrow Z_1 = \frac{R_d}{1+sR_dC_1} \quad (1)$$

According to Figure 3, the impedance at coupling node 2,

$$Z_2 = (Z_1 + R_s) \parallel X_{C_2} \parallel (R_e + X_{C_L})$$

Here, $X_{C_L} = \frac{1}{j\omega C_L}$ and $X_{C_2} = \frac{1}{j\omega C_2}$.

Applying $s = j\omega$ in Equation (2), and using the value of Z_1 from Equation (1),

$$\Rightarrow \frac{1}{Z_2} = \frac{1+sR_dC_1}{R_d+R_S+sR_dR_sC_1} + sC_2 + \frac{sC_L}{(sR_eC_L+1)} \quad (2)$$

Figure 4 is the modified circuit of Figure 3, where Z_2 is used.

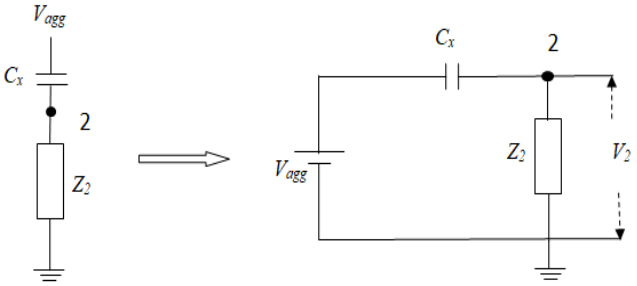

Figure 4: Equivalent noise model circuit.

The s-domain voltage $V_2(s)$ at point 2, across the impedance Z_2 satisfying the following relation

$$V_2(s) = \frac{Z_2}{Z_2 + \frac{1}{sC_x}} V_{agg}(s)$$

$$\Rightarrow$$

$$V_2(s) = \frac{sC_x}{sC_x + \frac{1+sR_dC_1}{R_d+R_s+sR_dR_sC_1} + sC_2 + \frac{sC_L}{sR_eC_L+1}} V_{agg}(s) \quad (3)$$

The output voltage V_{out} in the s-domain is

$$V_{out}(s) = V_2(s) \frac{\frac{1}{sC_L}}{R_e + \frac{1}{sC_L}}$$

$$V_{out}(s) = V_2(s) \frac{1}{sC_LR_e+1} \quad (4)$$

Substituting Z_1, Z_2, and $V_2(s)$ into $V_{out}(s)$ yields,

$$V_{out}(s) = \frac{\frac{sC_x}{sR_eC_L+1}}{s(C_x+C_2) + \frac{1+sR_dC_1}{R_d+R_s+sR_dR_sC_1} + \frac{sC_L}{sR_eC_L+1}} V_{agg}(s)$$

Let, $R_dR_sC_1C_x = K_1$, $R_dR_sC_1C_LR_e(C_x+C_2) = K_2$, $a_2 = \frac{C_x(R_d+R_s)}{K_2}$,

$$a_2 = \frac{K_1}{k_2},\ b_1 = \frac{(C_x + C_2)(R_d + R_s) + (R_d C_1 + C_L R_e) + C_L(R_d + R_s)}{K_2},$$
$$b_2 = \frac{(C_x + C_2)(R_d R_s C_1 + C_L R_e) + (R_d R_e C_1 C_L + R_d R_s C_1 C_L)}{K_2} \text{ and}$$
$$b_0 = \frac{1}{K_2}.$$

Then,

$$V_{out}(s) = \frac{a_2 s^2 + a_1 s}{s^2 + b_2 s^2 + b_1 s + b_0} V_{agg}(s) \quad (5)$$

Now, let the aggressor voltage with unit step input and the normalized value is, $V_{dd} = 1$, be

$$V_{agg} = \begin{cases} 1 & t \geq 0 \\ 0 & \text{Otherwise} \end{cases}$$

And its s-domain representation is $V_{agg}(s) = \frac{1}{s}$.

A. ***Noise amplitude calculation:*** Using dominant-pole approximation m*e*thod [7] in Equation (5), we obtain

$$V_{out}(s) = \frac{a_1 s}{b_1 s + b_0} \times \frac{1}{s}$$
$$V_{out}(s) = \frac{a_1}{b_1 s + b_0} \quad (6)$$

$$V_{out}(s) = \frac{C_x(R_d + R_s)}{(C_x + C_2)(R_d + R_s) + (R_d C_1 + C_L R_e) + C_L(R_d + R_s)s + 1}$$
$$V_{out}(s) = \frac{t_x}{t_v(s + \frac{1}{t_v})} \quad (7)$$

Here, $C_x(R_d + R_s) = t_x$ (8)

and $(C_x + C_2)(R_d + R_s) + (R_d C_1 + C_L R_e) + C_L(R_d + R_s) = t_v$ (9)

The term t_x represents the RC delay term from the upstream resistance of the coupling element times the coupling capacitance. The term t_v represents distributed Elmore delay [19] of victim line. The output voltage shown in Equation (7) can be expressed in time domain as given in Equation (10).

$$V_{out}(s) = \frac{t_x}{t_v} e^{\frac{-t}{t_v}}, \text{ where } t \geq 0 \quad (10)$$

From the noise expression shown in Equation (10), it is evident that noise monotonically decreases as $t \geq 0$. The value of noise will be maximum at $t = 0$. This maximum value of noise can be calculated by putting $t = 0$ in Equation (10).

$$V_{out}(s) = \frac{t_x}{t_v} \quad (11)$$

Let, thickness (e), width (w), height from substrate (h) and distance between two metal tracks(d) of interconnected metals used for aggressor and victim line are the same.

According to [8], the expression of substrate capacitance can be written as

$$(C_1 = C_2 = C_L = \varepsilon_0 \varepsilon_r \left[1.13\left(\frac{w}{h}\right) + 1.443\left(\frac{w}{h}\right)^{0.11} + 1.475\left(\frac{e}{h}\right)^{0.425} \right] \quad (12)$$

According to [8], the expression of coupling capacitance can be written as,

$$C_x = \varepsilon_0 \varepsilon_r \left(\left(\frac{w}{h}\right)^{0.32} + 1.82\left(\frac{e}{h}\right)^{0.18} \right) \left(\frac{d}{h} + 0.43\right)^{-1.38} \quad (13)$$

Let the metal used for aggressor and victim lines be counted as squares. Then, according to [14],

The sheet resistance of metal $(R_S) = \frac{\rho}{e}$. (14)

The total resistance of metal, $R = \frac{\rho L}{ew}$ (15)

From Equations (8), (9), (12), (13), (14) and (15), the expression of t_x and t_v can be written as,

$$t_x = 2\frac{\rho L}{ew} \varepsilon_0 \varepsilon_r \left(\left(\frac{w}{h}\right)^{0.32} + 1.82\left(\frac{e}{h}\right)^{1.08} \right) \left(\frac{d}{h} + 0.43\right)^{-1.38} \quad (16)$$

And

$$t_v = 2\frac{\rho L}{ew} \varepsilon_0 \varepsilon_r \left\{ \left[\left(\left(\frac{w}{h}\right)^{0.32} + 1.82\left(\frac{e}{h}\right)^{1.08} \right) \left(\frac{d}{h} + 0.43\right)^{-1.38} \right] + 3\left[1.13\left(\frac{w}{h}\right) + 1.443\left(\frac{w}{h}\right)^{0.11} + 1.475\left(\frac{e}{h}\right)^{0.425} \right] \right\} \quad (17)$$

From the maximum amplitude of noise, as shown in Equation (11), it is written with the inclusion of the interconnect thickness (e), width (w), height from substrate (h) and distance between two metal tracks(d) of aggressor and victim lines using Equations (16) and (17),

i.e. , $V_{max} = \frac{t_x}{t_v}$

$$\Rightarrow V_{max} = \frac{2\frac{\rho L}{ew} \varepsilon_0 \varepsilon_r \left(\left(\frac{w}{h}\right)^{0.32} + 1.82\left(\frac{e}{h}\right)^{1.08} \right) \left(\frac{d}{h} + 0.43\right)^{-1.38}}{2\frac{\rho L}{ew} \varepsilon_0 \varepsilon_r \left\{ \left[\left(\left(\frac{w}{h}\right)^{0.32} + 1.82\left(\frac{e}{h}\right)^{1.08} \right) \left(\frac{d}{h} + 0.43\right)^{-1.38} \right] + 3\left[1.13\left(\frac{w}{h}\right) + 1.443\left(\frac{w}{h}\right)^{0.11} + 1.475\left(\frac{e}{h}\right)^{0.425} \right] \right\}}$$

$$\Rightarrow V_{max} = \frac{1}{\left[1 + \frac{3\left[1.13\left(\frac{w}{h}\right) + 1.443\left(\frac{w}{h}\right)^{0.11} + 1.475\left(\frac{e}{h}\right)^{0.425} \right]}{\left(\left(\frac{w}{h}\right)^{0.32} + 1.82\left(\frac{e}{h}\right)^{1.08} \right) \left(\frac{d}{h} + 0.43\right)^{-1.38}} \right]} \quad (18)$$

The noise expression shown in Equation (10) can also be written including interconnect thickness (e), width (w), height from substrate (h) and distance between two metal tracks (d) of aggressor and victim lines using Equations (16), (17) and (18), i.e.,

$$V_{max} = \frac{t_x}{t_v} e^{\frac{-t}{t_v}}, \text{ where } t \geq 0.$$

$$\Rightarrow V_{out}(t)=\frac{1}{\left[1+\frac{3\left[1.13\left(\frac{w}{h}\right)+1.443\left(\frac{w}{h}\right)^{0.11}+1.475\left(\frac{e}{h}\right)^{0.425}\right]}{\left(\left(\frac{w}{h}\right)^{0.32}+1.82\left(\frac{e}{h}\right)^{1.08}\right)\left(\frac{d}{h}+0.43\right)^{-1.38}}\right]\left\{e^{-\frac{t}{2\frac{\rho L}{ew}\varepsilon_0\varepsilon_r\left\{\left[\left(\left(\frac{w}{h}\right)^{0.32}+1.82\left(\frac{e}{h}\right)^{1.08}\right)\left(\frac{d}{h}+0.43\right)^{-1.38}\right]+3\left[1.13\left(\frac{w}{h}\right)+1.443\left(\frac{w}{h}\right)^{0.11}+1.475\left(\frac{e}{h}\right)^{0.425}\right]\right\}}}\right\}} \quad (19)$$

B. ***Noise width calculation:*** The noise width for a noise pulse is defined to be the length of time interval so that the noise spike voltage V is larger than or equal to V_t.

Here V_t represents the threshold voltage. Now from Equation (10),

$$V_{max}=\frac{t_x}{t_v}e^{\frac{-t}{t_v}}$$
$$t=t_v\ln\left(\frac{1}{V_{out}}.\frac{t_x}{t_v}\right) \quad (20)$$

Thus, noise width is calculated by the width of time interval between t_1 and t_2.

Here t_1 = initial time = 0

And t_2 is the time when noise voltage is equal to the threshold voltage V_t.

The value of t_2 can be calculated using Equation (19). Hence, t_2 can be derived as,

$$t_2=t_v\ln\left(\frac{1}{V_t}.\frac{t_x}{t_v}\right)$$

Noise width is given by,

$$t_{width}=t_2-t_1=t_2-0=t_2$$
$$t_{width}=t_v\ln\left(\frac{1}{V_t}.\frac{t_x}{t_v}\right) \quad (21)$$

In this paper, we assume the value of threshold voltage V_t to be half of the value of the peak noise voltage V_{max} [7].

$$\text{i.e., } V_t=\frac{V_{max}}{2} \quad (22)$$

Now from Equations (11), (20) and (21),

$$t_{width}=t_v\ln(2)=0.69t_v \quad (23)$$

Equation (23) represents the expression of the width of the noise voltage waveform. For unit step input, note that when the time increases beyond t_2, the noise voltage becomes very less. This can be expressed clearly by some noise amplitude versus noise width plots.

From Equations (17) and (23), the expression of width of noise voltage waveform can be written as

$$t_{width}=0.69\left\{2\frac{\rho L}{ew}\varepsilon_0\varepsilon_r\left\{\left[\left(\left(\frac{w}{h}\right)^{0.32}+1.82\left(\frac{e}{h}\right)^{1.08}\right)\left(\frac{d}{h}+0.43\right)^{-1.38}\right]+3\left[1.13\left(\frac{w}{h}\right)+1.443\left(\frac{w}{h}\right)^{0.11}+1.475\left(\frac{e}{h}\right)^{0.425}\right]\right\}\right\}$$

$$\Rightarrow t_{width}=1.38\frac{\rho L}{ew}\varepsilon_0\varepsilon_r\left\{\left[\left(\left(\frac{w}{h}\right)^{0.32}+1.82\left(\frac{e}{h}\right)^{1.08}\right)\left(\frac{d}{h}+0.43\right)^{-1.38}\right]+3\left[1.13\left(\frac{w}{h}\right)+1.443\left(\frac{w}{h}\right)^{0.11}+1.475\left(\frac{e}{h}\right)^{0.425}\right]\right\} \quad (24)$$

This expression represents the width of the noise voltage with respect to time.

III. RESULTS AND DISCUSSION

The estimation of noise voltage is very important to measure the system performance. To estimate the noise voltage across the victim line, noise amplitude versus distance between two interconnects has been plotted, as seen in Figure 5, using Equation (18) and keeping the aspect ratio (w/h) constant. The figure shows that increasing the distance between interconnects decreases the noise amplitude and vice versa. In the plot, X-axis represents the distance between interconnects in meter, and Y- axis represents the maximum amplitude of noise voltage in volt. Thus, this result shows that noise amplitude is inversely proportional to the distance between interconnects.

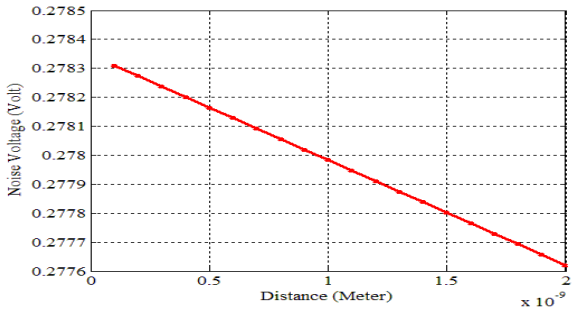

Figure 5: Noise amplitude versus distance, keeping the aspect ratio constant.

Again noise amplitude versus aspect ratio of interconnect has been plotted to estimate noise amplitude, using Equation (18), keeping the distance between interconnects constant, as seen in Figure 6. In the plot, X-axis represents the aspect ratio (dimensionless) and Y- axis represents the maximum amplitude of noise voltage in volt. The plot in Figure 6 shows that increasing the aspect ratio of interconnects decreases the noise amplitude and vice versa reveal that noise amplitude is inversely proportional to the aspect ratio of interconnects.

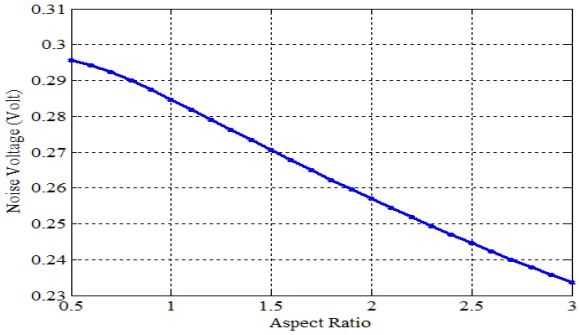

Figure 6: Noise amplitude versus aspect ratio, keeping the distance constant.

Then output noise voltage with respect to time for unit step input is plotted in Figure 7, using Equation (19) when 2πRC model is used, taking into account the different values of width, height, thickness, spacing between interconnects, length of interconnects. The figure shows the output noise voltage developed at the victim line for the application of unit step input in aggressor line when 2π RC model is considered. In the plot, X-axis represents the time in second and Y-axis represents the noise voltage in volt. The figure expresses that the amplitude of the noise voltage gradually decreases with respect to time. The maximum amplitude of this noise voltage is 0.266 volt.

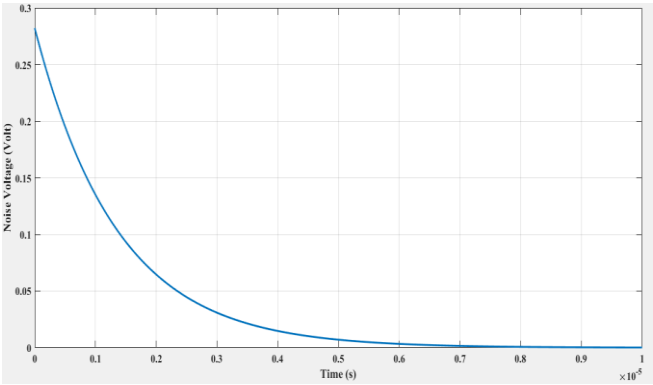

Figure 7: output noise voltage versus time for unit step input when 2π model is used.

After that, the 2π RC model of Figure 3 is designed with HSPICE simulator for 180 nm technology. The extracted values for the parameters R and C are given in Table 1.

Table 1
Values of R and C for 180 nm technology [20]

Parameters	Value/m
Resistance (R)	120 kΩ
Capacitance (C)	240 pF
Coupling Capacitance (Cc)	681 pF

In HSPICE software platform, we simulated the 2π model with unit step impulse at aggressor line using different parameters' values of interconnection. Figure 8 represents the result of input impulse provided to the aggressor line and output noise at the victim line, which is obtained by simulating 2π model in HSPICE software platform. Based on Figure 8, the unit step impulse is applied to the aggressor line resulting in the development of aggressor voltage across aggressor capacitor. This effect also results in a new development of voltage across victim capacitor. After some time, the capacitor starts discharging and goes to its initial state. We applied transient condition and measured the results with HSPICE software, as shown in Table 1.

The SPICE plot shown in Figure 8 represents the input unit step voltage and noise voltage across the victim capacitor combined. In the plot, red line represents the input unit step and blue is the noise voltage (node 3).

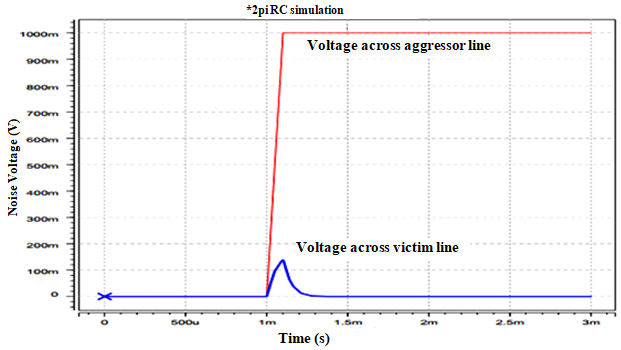

Figure 8: Input unit step voltage and developed noise voltage at the victim capacitor.

The values of different parameters, namely the width of wire (w), thickness of wire (e), spacing between two wires (d), height of interconnects from substrate (h), and length of wires (L) were calculated. Finally, the peak noise was estimated for each set of physical parameters, which are given in Table 2.

Table 2
Estimation of output peak noise voltages for 2π RC models

Sl. No	(w) µm	(h) µm	(e) µm	(d) µm	(w/h)	(L) mm	V_{max} (Volts)
01	1.173	1.173	0.117	0.1	1.0	1.2	0.282
02	0.645	0.810	0.080	0.3	0.8	2.0	0.287
03	1.230	1.118	0.011	0.2	1.1	0.8	0.277
04	0.460	0.511	0.05	0.52	0.9	1.6	0.284
05	0.860	0.573	0.114	0.10	1.5	2.0	0.282
06	1.110	0.925	1.026	0.2	1.2	2.0	0.301
07	1.133	1.890	0.184	0.4	0.6	2.0	0.291
08	1.314	3.285	0.327	0.2	0.4	2.0	0.250
09	0.360	1.800	0.180	0.1	0.2	0.7	0.270
10	0.523	1.740	0.346	0.6	0.3	2.0	0.312

We analysed the performance of different models by varying the values of physical parameters, while keeping the passive elements constant, as given in Table 1. For this analysis, the noise amplitude expression Equation (18) has been used. The MATLAB software was initially used for simulation and the result demonstrated the accuracy of the 2π RC model, when calculating the peak noise amplitude of two capacitively coupled interconnects for a unit step input at the aggressor line. We have analysed Devgan model [9], Vittal model [10], Heydari model [11] and 2π models [7] [18] using the method described above, and found similar results for peak noise at the victim line, as reported in their works.

Estimation of the noise voltage peak and width with the values of different physical parameters can play a great role to improve the system performance in DSM technology. We found that the use of these values help us to identify the physical parameters to calculate peak noise in victim line, which is very effective to reduce noise in the transmission line for the existing models, and 2π model possesses better result by this new approach in comparison to the other models.

We then calculated the peak noise widths. Table 3 gives the result of peak noise widths (t_{width}) for the victim line by using both analytical and simulation methods respectively. İn this table, it is clearly seen that noise width of our simulation is quite similar to the noise width of the analytical 2π RC model. Therefore, it is concluded that the length of time interval of spike voltage is comparable, causing less effect of crosstalk for small interval of time.

Table 3
Summary of results for noise width

Sl. No	(w) µm	(h) µm	(e) µm	(d) Mm	(w/h)	(L) µm	t_{width} (Anal.) (µsec)	t_{width} [HSPICE] (µsec)
01	1.173	1.173	0.117	0.1	1	1.2	0.9154	1.25
02	0.645	0.810	0.080	0.3	0.8	2	2.2930	1.29
03	1.230	1.118	0.011	0.2	1.1	0.8	5.6164	2.00
04	0.460	0.511	0.051	0.52	0.9	1.6	3.1552	2.77
05	0.860	0.573	0.114	0.1	1.5	2	2.7535	3.00
06	1.110	0.925	1.026	200	1.2	2	3.1295	3.21
07	1.314	3.285	0.327	0.2	0.4	2	0.3737	3.20
08	0.360	1.800	0.180	0.1	0.2	0.7	2.8838	2.80

Finally, the simulation of 2π model to estimate the peak noise amplitude was performed using HSPICE software platform. Taking all parameters value of interconnects, 2π

model circuit design, a simulation was conducted at the node where crosstalk noise affect the victim line due to different issues, especially coupling capacitance between aggressor line and victim line. With the help of the Equations (12), (13), (14) and (15), and using the optimum values of physical parameters which reduces the noise peak values, we calculated the passive elements values for the 2π model to find the parcentage of error for various passive elements values and estimate the average parcentage of error, which is given in Table 4.

Table 4
Estimation of percentage of errors for 2π model

Sl. No	R (kΩ)	Cs (pF/m)	Cc (pF/m)	2π (Anal.) Volts	2π (HSPICE) Volts	2π (This paper) (% Err.)
1	150	107	127	0.282	0.204	27.65
2	400	98	120	0.287	0.250	12.89
3	1000	100	115	0.277	0.262	5.40
4	527	103	123	0.284	0.250	11.9
5	350	136	161	0.282	0.245	13.12
6	30	150	195	0.301	0.211	29.90
7	160	90	111	0.291	0.204	29.8
8	80	80	99	0.250	0.238	4.80
9	527	68	83	0.270	0.236	12.5
10	190	81	110	0.312	0.223	12.59
					Average	16.06

By using the same combination of passive elements values provided in Table 4, we calculated the peak noise voltages for the four different models and estimated the percentage of error for each combinations. At the end of the process, we calculated the average values of errors for the respective models to measure the system performance, as presented in Table 5.

Table 5
Comparison of the errors of different models

Sl. No	2π (This paper) (% Err.)	Devgan (% Err.)	Vittal (%Err.)	Heydari (% Err.)
1	27.65	2.55	27.00	3.22
2	12.89	21.07	39.70	38.95
3	5.40	35.82	27.79	11.94
4	11.90	26.49	14.43	18.30
5	13.12	11.29	4.138	8.31
6	29.90	3.68	13.30	3.30
7	29.80	4.17	8.59	9.69
8	4.80	3.49	32.00	11.52
9	12.50	12.57	21.81	21.74
10	12.59	1.92	39.10	36.89
Average	16.06	12.30	21.78	16.386

We calculated the percentage of noise errors for Devgan model [9], Vittal model [10], Heydari model [11], 2π model [This paper], comparing them with HSPICE simulation result and errors of 16.06%, 12.30%, 21.78%, and 16.39%, respectively. Although the percentage of noise error of 2π [This paper] and Heydari models are almost at the same range, the implementation of 2π RC model is more effective and less complicated in terms of transmission line modeling.

At the end, the analysis of noise voltages with respect to frequency has been performed, taken into consideration of the same parametersas mentioned above for 2π model. AC unit step input is provided to the aggressor line with increasing frequency. We plotted innoise (node 2) and outnoise (node 4) at panel 1 and panel 2 in HSPICE simulator respectively, as shown in Figure 9, where X-axis represents the frequency in Hz and Y-axis represents the noise voltage at aggressor node. In Figure 9 (a), it clearly indicates an exponentially decrease of innoise resulting from the frequency increasing, and in Figure 9 (b) indicates the outnoise at aggressor. Therefore, we can establish that noise is inversely proportional to frequency within a certain level.

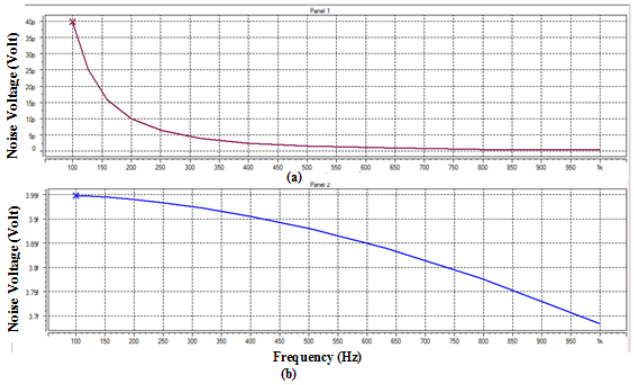

Figure 9: Noise calculation (a) innoise (b) outnoise for AC analysis.

The existing models did not take into account the physical parameters for estimating and minimizing crosstalk noise over a range of operating frequency. In our work, we used the value of resistors, capacitors according to [20] and established a relation between the passive elements and physical parameters of transmission line to find the peak noise voltage and noise width at the victim line.

IV. CONCLUSION

In this work, we focus on the analysis of 2π RC model to get accurate modelling of crosstalk noise using different interconnect parameters' (width of wire, thickness of wire, spacing between two wires, height of interconnects from substrate, length of wires) values for RC interconnects in DSM VLSI circuits and derived expressions for peak amplitude, pulse width, and time-domain waveform of crosstalk noise. MATLAB and HSPICE software platform have been used to simulate 2π model with different parameters' values, and these simulation results were compared with analytical values of different crosstalk estimation models. It is concluded that although the crosstalk noise amplitude and width in victim line are the major problems in transmission line signal propagation, this can be minimized by optimizing the interconnecting parameters for any particular range of frequency.

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