Optimization of Process Parameters for Threshold Voltage and Leakage Current based on Taguchi Method

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***Abstract*— In this study, the effect of process parameters on the threshold voltage (V_{th}) and leakage current (I_{leak}) were explored and the optimization of these parameters were carried out using the Taguchi method. The virtual device was initially constructed using ATHENA and ATLAS environment in Silvaco Technology Computer Aided Design (TCAD) tools. The simulation studies were directed under four varying process parameters, which are V_t adjust implantation dose, the halo tiling angle, the S/D implantation dose and the compensation implantation dose. The L9 Orthogonal Array (OA), the signal-to-noise ratio (SNR), and the analysis of variance (ANOVA) were used to study the performance characteristics and to gain an optimum combination of parameter settings. It was revealed that the V_t adjust implantation dose was the most influential parameter on the V_{th} and I_{leak}. Furthermore, it also improves the device performance. The result of V_{th} complied with the projections made by the International Technology Roadmap for Semiconductors (ITRS).**

***Index Terms*— ANOVA; ATHENA; ATLAS; Taguchi Method; Silvaco TCAD tools.**

I. INTRODUCTION

There is always an increasing demand for a low-power-high-speed transistor. This is because the transistor is the most important component for all electronic circuits. In order to meet the consumer's demands besides being bound by Moore's law, more transistors were crammed into a single chip, leading to difficulties in controlling the dopants concentration and their placements [1].

Extensive studies were carried out to overcome these problems. While some researchers invented new device topology such as those in [2-3] and proposed the utilization of new materials such as those in [4-6], the key may lie within the transistor itself by optimizing the design parameters of the device. The optimization of process parameters is of great importance where the quality and the cost of fabricating transistors play a key role.

There are a few commonly used optimization approaches available such as the grey relational analysis, build-test-fix, and full factorial analysis; Taguchi method provides an efficient and systematic way to optimize the device performance, cost and quality. Taguchi method has been utilized successfully in designing reliable and high-quality products at low cost in many areas such as aerospace and automotive [7-9]. Previously, some of the conventional technologies such as Silicon transistors [1, 10-12] were optimized using Taguchi method. This work is the first to use the Taguchi method for the graphene transistor optimization.

The objective of this article is to demonstrate the application of the L9 Taguchi design parameters in order to determine the optimum threshold voltage and leakage current performance with a specific combination of four process parameters. The process parameters were the halo tilting angle (**A**), the S/D implantation dose (**B**), the compensation implantation dose (**C**), and the V_t adjust implantation dose (**D**). These process parameters were varied at three levels and two levels of noise factors known as Phosphor Silicate Glass (PSG) temperature (**X**) and Boron Phosphor Silicate Glass (BPSG) temperature (**Y**). The results of the optimization were benchmarked with the ITRS prediction for 14 nm gate length technology. The V_{th} is set to be within the range of 0.230 V ± 12.7 % and I_{leak} should be equals to or lower than 100 nA/um.

II. EXPERIMENTAL PROCEDURE

A. Fabrication Method

The 14 nm planar p-type graphene transistor was virtually fabricated using ATHENA environment while its electrical characteristic was analyzed using ATLAS environment. Both modules can be found in SILVACO TCAD simulation tools. The method follows the established recipe in [13] and the summary of the process flow is shown in Table 1. The final step took place by reflecting the half-made device after the deposition of Aluminium metal. The doping profile of the well-formed device can be seen in Figure 1. This device shows that there is a clear separation between the source and the drain which leads to a conclusion that the lower leakage current is achieved. The key is to use the correct dopant value. This is because a good doping value will ensure that the transistor can function effectually i.e. perfect gate control and low leakage current [14].

Table 1
Simulation Procedure

Steps	Parameters
Substrate	• Silicon • <100> orientation • 200Å oxide screen by 970°C, 20min of dry oxygen
Retrograde well implantation	• $3.75x10^{10}$ cm^{-3} Phosphorous • 50min, 900°C diffused in Nitrogen • 36min, dry Oxygen • 130Å stress buffer by 900°C, 25min of dry oxygen
STI isolation	• 1500Å Si_3N_4, applying LPCVD • 1.0um photoresist deposition • 15min annealing at 900°C
Gate oxide	• diffused dry oxygen for 0.001min, 825°C
V_t adjust implant	• $1.75x10^{11}$ cm^{-3} Boron difluoride • 5KeV implant energy, 7° tilt • 20min annealing at 800°C
Halo implantation	• 5.41 $x10^{13}$ cm^{-3} Phosphor • 19.8° tilt • 160KeV implant energy
Bilayer graphene deposition	• 0.00068um Graphene
High-K/Metal gate deposition	• 0.00067um HfO_2 • 0.050um WSi_2 • 30min, 800°C annealing
Sidewall spacer deposition	• 0.047um Si_3N_4
S/D implantation	• 1.301 $x10^{13}$ cm^{-3} Arsenic • 10KeV implant energy • 7° tilt
PMD deposition	• 0.05um BPSG • 20min, 850°C annealing • 1.2 $x10^{12}$ cm^{-3} Phosphor • 60KeV implant energy • 7° tilt
Metal 1	• 0.04um Aluminium
IMD deposition	• 0.05um BPSG • 15min, 950°C annealing
Metal 2	• 0.12um Aluminium

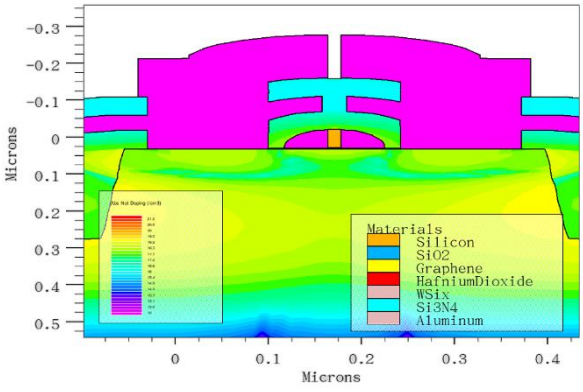

Figure 1: Doping profile of 14 nm p-type graphene MOSFET

B. *The L9 OA*

The performance analysis of the process parameters variations using Taguchi's method is a reliable and systematic approach. Unlike the conventional methods which are too complex to be utilized, a certain standard of OA was designed where the analysis can be done in a minimum number of tests In Taguchi's method [12]. Through the analysis, a loss function was defined to measure the aberrations between the experimental value and the desired value where it was then transferred into an SNR, ŋ. There are three types of SNR available depending on the type of characteristics which includes the lower-the-better (LTB), the nominal-the-better (NTB), and the higher-the-better (HTB). In this research, an optimum V_{th} and lower I_{leak} are indications of a transistor with good performance. Hence, to obtain the optimum device performance, the SNR of NTB (η_{NTB}) and the SNR of LTB (η_{LTB}) were selected for V_{th} and I_{leak} respectively. The SNR for each type of characteristic is calculated as follows [9] [13]:

$$\eta_{NTB} = 10 \log \left[\frac{\mu^2}{\sigma^2} \right] \quad (1)$$

$$\eta_{LTB} = -10 \log \left(\frac{1}{n} \sum_{i=1}^{n} Yi^2 \right) \quad (2)$$

where μ is the average of the observed data, σ is the variance of y, n is the number of observations, and y is the observed data. The optimum level of process parameter was chosen based on the highest SNR. This was because greater SNR value indicated better performance characteristics [8]. In this research, four process parameters were chosen and varied at three levels, denoted as Level 1, Level 2, and Level 3. The process parameters include halo tilting angle (**A**), S/D implantation dose (**B**), Compensation implantation dose (**C**), and V_t adjusts implantation dose (**D**). The noise factors which were varied at two levels includes PSG temperature (**X**) and BPSG temperature (**Y**). The factors and their levels are tabulated in Table 2 and Table 3 respectively. Next, the degree of freedom (DOF) was computed in order to choose a proper OA for the experiments, where it should be equal to or greater than those for the design parameters. For this case, L9 OA was utilized as it had eight DOF and was able to handle three level design parameters. The L9 OA can be seen in [7]. The results of the simulations for V_{th} and I_{leak} are shown in Table 4 and Table 5.

Table 2
Process parameters and the settings of levels

Sym	Process parameter	Units	Level 1	Level 2	Level 3
A	Halo tilting angle	°	19.78	19.79	19.8
B	S/D implantation dose	$atom/cm^3$	$1.301x10^{13}$	$1.302x10^{13}$	$1.303x10^{13}$
C	Compensation implantation dose	$atom/cm^3$	$1.19x10^{12}$	$1.2x10^{12}$	$1.21x10^{12}$
D	V_t adjust implantation dose	$atom/cm^3$	$1.7x10^{11}$	$1.75x10^{11}$	$1.8x10^{11}$

Table 3
Noise factors and the settings of levels

Sym.	Process parameter	Units	Level 1	Level 2
X	PSG Temperature	°C	900	910
Y	BPSG Temperature	°C	850	852

Table 4
Experimental results of V_{th} (V)

Exp. No	X1Y1	X1Y2	X2Y1	X2Y2
1	-0.2349	-0.2379	-0.1900	-0.1934
2	-0.2316	-0.2345	-0.1862	-0.1896
3	-0.2282	-0.2312	-0.1824	-0.1857
4	-0.2305	-0.2335	-0.1851	-0.1884
5	-0.2400	-0.2432	-0.1955	-0.1988
6	-0.2304	-0.2333	-0.1849	-0.1882
7	-0.2388	-0.2420	-0.1942	-0.1975
8	-0.2291	-0.2321	-0.1835	-0.1869
9	-0.2384	-0.2416	-0.1939	-0.1972

Table 5
Experimental results of I_{leak} (nA/um)

Exp. No	X1Y1	X1Y2	X2Y1	X2Y2
1	22.05	21.68	22.49	22.11
2	22.50	22.12	22.95	22.56
3	22.96	22.57	23.42	23.02
4	22.62	22.24	23.08	22.69
5	21.43	21.07	21.85	21.49
6	22.61	22.23	23.06	22.67
7	21.58	21.21	22.00	21.63
8	22.77	22.38	23.22	22.83
9	21.57	21.21	21.99	21.62

III. Analysis and Discussions

A. Analysis of the Signal-to-Noise Ratio

The next steps were to analyze the SNR values for V_{th} and I_{leak}. The mean for each level of process parameters was calculated and the results are shown in Table 6 and Table 7. From Table 6 and Table 7, the optimum process parameter for the V_{th} and I_{leak} was obtained at the same level for all four parameters. The results were obtained at 19.8° of **A** (level 3), $1.301x10^{13}$ atom/cm^3 of **B** (level 1), $1.21x10^{12}$ atom/cm^3 of **C** (level 3) and $1.7x10^{11}$ atom/cm^3 of **D** (level 1). The plots of the SNR for the process parameters **A**, **B**, **C** and **D** at three levels are presented in Figure 2 and Figure 3 respectively. The SNR corresponds to the smaller variance of the output characteristics around the target value [12].

Table 6
SNR Analysis and significant interaction for V_{th}

Performance Parameter	Process parameter	Signal-to-noise ratio (SNR)			Overall Mean SNR
		Level 1	Level 2	Level 3	
V_{th}	**A**	18.12	18.24	18.35[a]	18.24
	B	18.32[a]	18.23	18.16	
	C	18.12	18.24	18.34[a]	
	D	18.50[a]	18.23	17.97	

[a]Optimum level

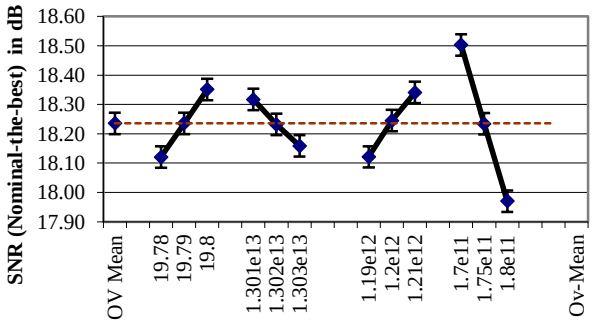

Figure 2: Mean SNR plots for V_{th}

Table 7
SNR Analysis and significant interaction for I_{leak}

Performance Parameter	Process parameter	Signal-to-noise ratio (SNR)			Overall Mean SNR
		Level 1	Level 2	Level 3	
I_{leak}	**A**	152.94	153.05	153.15[a]	153.05
	B	153.11[a]	153.05	152.99	
	C	152.95	153.05	153.15[a]	
	D	153.27[a]	153.05	152.83	

[a]Optimum level

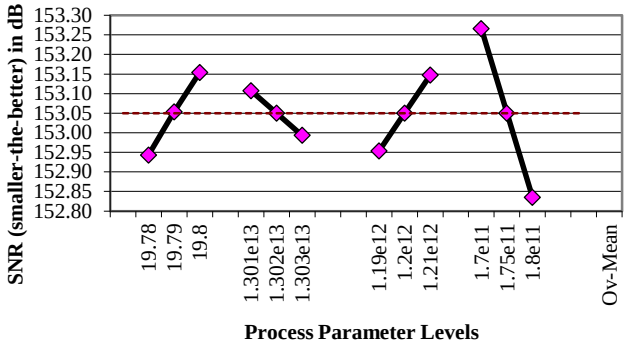

Figure 3: Mean SNR plots for I_{leak}

B. Analysis of Variance

The purpose of performing the ANOVA was to determine which process parameter significantly affects the device performances. At this stage, the relative importance of the process parameter with respect to V_{th} and I_{leak} was studied to determine precisely the optimum combination of process parameters. The analysis was consummated for the level of significance of 1 % (the level of confidence is 99 %) [12]. The results of the ANOVA for the device design outputs are shown in Table 8 and Table 9. The contribution percentage of each parameter indicates their degree of impact to the device performance. This means, the higher the percentage of contribution, the higher the influence of a parameter on the device performance. The results of ANOVA for the V_{th}, which can be seen in Table 8 show that V_t adjusts implantation dose has the most dominant effect (69.13 %) followed by halo tilting angle (12.92 %), compensation implantation dose (11.82 %) and S/D implantation dose (6.13 %). The change of S/D implantation dose in the range given in Table 2 has an irrelevant effect on the V_{th}. The results of ANOVA for I_{leak} on the other hand are shown in Table 9. It shows the same arrangement like V_{th} where the most dominant factor effect to the I_{leak} was V_t adjust implantation dose (66.18 %, followed by halo tilting angle (15.8 %) and compensation implantation dose (13.39 %). The S/D implantation dose has an insignificant effect on I_{leak} (4.63 %).

Table 8
ANOVA results for V_{th}

Performance Parameter	Process parameter	DOF	SSQ	F value	Contribution (%)
V_{th}	**A**	2	0.0796	6.46	12.92
	B	2	0.0378	3.07	6.13
	C	2	0.0728	5.91	11.82
	D	2	0.4260	34.56	69.13

Table 9
ANOVA results for I_{leak}

Performance Parameter	Process parameter	DOF	SSQ	F value	Contribution (%)
I_{leak}	**A**	2	0.0666	7.90	15.80
	B	2	0.0195	2.32	4.63
	C	2	0.0565	6.69	13.39
	D	2	0.2791	33.09	66.18

C. Verification Tests

Once the optimum level of the process parameters was selected, the next step was to predict and verify the improvement of the performance characteristics during the analysis phase. The results of the verification test for V_{th} is shown in Table 10. The increase of SNR from the initial parameters to the level of optimum parameters is 0.4 dB. Though the V_{th} is increased by 1.04 times, the result is valid as it is still within the ITRS prediction of -0.230 V ± 12.7 %. Table 11 shows the results of verification test for I_{leak}. The improvement of SNR from the initial parameters to the optimum parameters is 0.38 dB. The I_{leak} is greatly decreased by 1.06 times using the approach adopted in this research. A good agreement was observed between the actual value and the predicted value from the verification tests. This also confirms the efficacy of Taguchi method in embellishing the device performance.

Table 10
Results of verification test for V_{th}

	Initial process parameter	Optimal process parameter	
		Prediction	Experiment
Level	**A**2**B**2**C**2**D**2	**A**3**B**1**C**3**D**1	**A**3**B**1**C**3**D**1
V_{th} (V)	0.230901		0.241102
SNR (dB)	18.3	18.5	18.7
Improvement of SNR		0.4	

Table 11
Results of verification test for I_{leak}

	Initial process parameter	Optimal process parameter	
		Prediction	Experiment
Level	**A**2**B**2**C**2**D**2	**A**3**B**1**C**3**D**1	**A**3**B**1**C**3**D**1
I_{leak} (nA/um)	22.628		21.285
SNR (dB)	153.05	153.31	153.43
Improvement of SNR		0.38	

IV. CONCLUSIONS

The utilization of Taguchi method to optimize the device performance based on the process parameters has been reported in this article. Summarizing the results of the analysis in this research, the following conclusions can be drawn:

- The ANOVA results for V_{th} and I_{leak} shows that the V_t adjust implantation dose (**D**) is the major factor affecting the device performance while the S/D implantation dose (**B**) is insignificant to the device performance.
- It can be concluded that **A**3**B**1**C**3**D**1 (**A**= 19.8°, **B**= $1.301x10^{13}$ atom/cm^3, **C**= $1.21x10^{12}$ atom/cm^3, **D**= $1.7x10^{11}$ atom/cm^3) settings are the optimal process parameters for V_{th} and I_{leak}.
- The increase in the V_{th} (104 %), from the initial parameters to the optimum parameters is still within the ITRS prediction whereas the I_{leak} is decreased by 106 %.

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REFERENCES

[1] F. Salehuddin, K. E. Kaharudin, A. S. M. Zain, A. K. M. Yamin, and I. Ahmad, "Analysis of process parameter effect on DIBL in n-channel MOSFET device using L27 orthogonal array," in *International Conferences on Fundamental and Applied Sciences, AIP Conf. Proc.*, 2014.

[2] M. N. I. . Aziz, F. Salehuddin, A. S. . Zain, K. . Kaharudin, and S. . Radzi, "Comparison of electrical characteristics between Bulk MOSFET and Silicon-on-insulator (SOI) MOSFET," *J. Telecommun. Electron. Comput. Eng.*, 2014.

[3] K. E. Kaharudin, A. H. Hamidon, and F. Salehuddin, "Impact of Height of Silicon Pillar on Vertical DG-MOSFET Device," *Int. J. Comput. Information, Syst. Control Eng.*, vol. 8, no. 4, pp. 576–580, 2014.

[4] Y. J. Yu, Y. Zhao, S. Ryu, L. E. Brus, K. S. Kim, and P. Kim, "Tuning the graphene work function by electric field effect," *Nano Lett.*, vol. 9, no. 10, pp. 3430–3434, 2009.

[5] G. Giovannetti, P. A. Khomyakov, G. Brocks, V. M. Karpan, J. Van Den Brink, and P. J. Kelly, "Doping graphene with metal contacts," *Phys. Rev. Lett.*, vol. 101, no. 2, pp. 4–7, 2008.

[6] J. Zhu and J. C. S. Woo, "A novel graphene channel field effect transistor with Schottky tunneling source and drain," in *ESSDERC 2007 - Proceedings of the 37th European Solid-State Device Research Conference*, 2008.

[7] A. C. Mitra, M. Jawarkar, T. Soni, and G. R. Kiranchand, "Implementation of Taguchi Method for Robust Suspension Design," in *Procedia Engineering*, 2016.

[8] M. Jiang and R. Komanduri, "Application of Taguchi method for optimization of finishing conditions in magnetic float polishing (MFP)," *Wear*, 1997.

[9] M. Kouhi, "Robust Design Methods In Aerospace Engineering Robust Design Methods In Aerospace Engineering," November, 2008.

[10] N. F. Z. Abidin, I. Ahmad, and A. H. Afifah Maheran, "Statistical Process Modelling For 32nm High-k/Metal Gate NMOS Device," in *2nd National Graduate Conference(NadGrad2014)*, 2014, no. February, pp. 62–66.

[11] F. Salehuddin *et al.*, *Analysis of Threshold Voltage Variance in 45nm N-Channel Device Using L27 Orthogonal Array Method*, vol. 903, no. February. 2014.

[12] A. H. Afifah Maheran, P. S. Menon, I. Ahmad, and S. Shaari, "Optimisation of process parameters for lower leakage current in 22 nm n-type MOSFET device using Taguchi method," *J. Teknol. (Sciences Eng.*, vol. 68, no. 4, pp. 1–5, 2014.

[13] Z. A. N. Faizah, I. Ahmad, P. J. Ker, and P. S. Menon, "Process Characterization of 32nm Semi Analytical Bilayer Graphene-based MOSFET," in *MATEC Web of Conferences*, 2016, vol. 78, pp. 1–6.

[14] N. F. Z. A, I. Ahmad, P. J. Ker, and P. S. Menon, "Modelling and Characterization of a 14 nm Planar p-Type MOSFET Device," vol. 7, no. 3, pp. 27–30, 2015.