High-k Dielectric Thickness and Halo Implant on Threshold Voltage Control

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***Abstract*—High-k dielectric oxides have been used to replace the widely used silicon dioxide (SiO_2) gate dielectrics to overcome physical limits of transistor scaling. The thickness of high-k gate dielectric influences the threshold voltage (V_{TH}) and off-state leakage current (I_{OFF}). A device with high drive current (I_{ON}) and low I_{OFF} gives a high on-off current ratio (I_{ON}/I_{OFF}), which leads to a faster switching speed for the N-type Metal Oxide Semiconductor Field Effect Transistor (NMOS). In order to achieve the best I_{ON}/I_{OFF} ratio for a pre-determined range of V_{TH}, halo implant was used to adjust the threshold voltage. The finding shows that optimum V_{TH} and I_{ON}/I_{OFF} ratio can be achieved by selecting the most suitable halo implant dose in a virtually fabricated 14nm gate-length La_2O_3-based NMOS device with varying high-k dielectric oxide thickness.**

***Index Terms*—High-k dielectric; La_2O_3; metal gate; NMOS.**

I. INTRODUCTION

The semiconductor industry continuously develops new technologies to maintain its competitive edge. The downsizing of transistors has been the way forward to fuel the continued performance enhancement for the past few decades. The desire to have the smaller device is not without its benefits. A smaller device cost less to manufacture, comes with fewer defects and furthermore, size and speed have a strong correlation. Smaller transistors demonstrate faster switching speeds. As the size shrinks, gate oxide thickness and power supply voltage are the two major parameters that are affecting the on-current of the transistor, which comes with scaling.

The need to further miniaturize the transistors comes with many advantages such as smaller components, increased energy efficiency and modern integrated powerful processors. However, the major disadvantage is the challenging, complicated and complex fabrication process that is required to produce reliable products. Most of the advanced CMOS products have been using hafnium dioxide (HfO_2) as the high-k material to replace silicon dioxide (SiO_2) in the effort of continuing the historical progress of scaling [1, 2].

The thicker high-k dielectric is used to eliminate the effect of having high tunneling current that causes increased power consumption and reliability issues. It was observed that thicker high-k gate dielectric exhibits higher fringing field effect from gate to source/drain regions, and thus has weaker gate control. As a consequence, it showed reduced subthreshold performance and degradation of short channel performance [3]. Further reducing the Equivalent Oxide Thickness (EOT) but maintaining a low leakage current has been the focus of many researchers in the usage of high-k material in the gate oxide. Various high-k materials such as Aluminum Oxide (Al_2O_3), Lanthanum Oxide (La_2O_3), Zirconium Oxide (ZrO_2), Tantalum Oxide (Ta_2O_5), Praseodymium Oxide (Pr_2O_3) and HfO_2 have the potential to replace SiO_2 [4, 5, 6] because of their high dielectric constants and wide band gaps. The incompatibility between the high-k material and the polysilicon gate resulted in the research on the other alternative gate materials to suppress the depletion effect, to minimize dopant penetration and to decrease gate sheet resistance. The metal gate is most commonly chosen as the alternative material to replace polysilicon gate.

The reduction of EOT below 1nm remains a challenging task even with the introduction of high-k dielectric with appropriate metal gates in order to continue the aggressive device scaling. The elimination of SiO_2-high-k interface has been demonstrated to achieve lower EOT [7]. Direct deposition of a high-k material such as lanthanum aluminate [8], HfO_2 [9], and Y_2O_3 [10] on silicon without a layer of SiO_2 on top of silicon have been reported. La_2O_3, which has a dielectric constant of 27, forms a silicate layer that has relatively high dielectric constant (k =8~14) with silicon substrate upon annealing. SiO_2 interfacial layer that was reported to be formed on Hf-based oxides at the silicon substrate interface was not observed [11].

In this paper, NMOS with direct high-k/Si without SiO_2 interfacial layer has been realized on a La_2O_3-based 14nm (NMOS) device through simulation using SILVACO software. Both the EOT and physical gate oxide thickness affect the short channel effects (SCEs) [12, 13]. Thus it is important to pay attention to both parameters in order to reduce the gate leakage to an acceptable level.

La_2O_3 gate dielectrics have gained increased attention and much research has been conducted to investigate its properties due to the fact that La_2O_3 could make direct contact with Si substrate by forming a La-silicate layer without the need of SiO_2 as the interfacial layer. In addition, La_2O_3 exhibits good thermal stability, high dielectric constant (~27), wide band gap (~5.6 eV) and large conduction band offset (~2.4 eV) that make it the right candidate for gate dielectric and to meet its goal of reducing leakage current.

The contribution of the I_{OFF}, which consists of various sources of leakage current to the speed and power tradeoff of NMOS, can be observed from the I_{ON}/I_{OFF}. Therefore, apart from concentrating on the I_{OFF}, the I_{ON}/I_{OFF} ratio is also

important. However, I_{ON}/I_{OFF} decreases significantly with a decrease in supply voltage. Thus, the ability to suppress I_{OFF} but at the same time increase, I_{ON} would improve gate controllability and overall device performance. The importance of having the correct V_{TH} and acceptable I_{ON}/I_{OFF} ratio are necessary to prevent short-circuit currents during switching, high power dissipation, slow output transitions or low output swings, in fulfilling design demands for high-performance NMOS.

The paper aims to investigate the effect of different high-k dielectric thickness [14], namely thickness of La_2O_3 on the I_{ON}/I_{OFF} ratio for the 14nm NMOS. Halo implant was adopted near the source and drain to prevent punch-through operation and reduce the effect on threshold voltage [15, 16]. Although halo implantation was implemented to reduce the short channel effect, it caused a threshold voltage shift due to dopant channeling [17]. The process also affected I_{OFF} and then directly impacted on the I_{ON}/I_{OFF} ratio. According to International Technology Roadmap for Semiconductors (ITRS) 2013, V_{TH} must be 0.230V±12.7% while I_{ON} must be more than 1267μA/μm and I_{OFF} must be below 100nA/μm for a device with good performance.

II. Materials and Methods

A 14nm La_2O_3-based NMOS was fabricated virtually using advanced process simulation tools from SILVACO TCAD software. The design of NMOS with high-k metal gate (HKMG) technology was modeled based on previous design simulated using the ATHENA process simulator [18-21]. La_2O_3 was identified to be the high-k oxide and tungsten as the metal gate for the fabricated NMOS. A schematic structure of the NMOS is given in Figure 1. Different thicknesses of La_2O_3, which were 2nm, 3nm, 4nm and 5nm, were deposited directly on top of silicon in separate experiments to fabricate four NMOS devices with different high-k oxide thicknesses. Tungsten with a fixed thickness of 38nm was then deposited on top of the high-k oxide on the devices [19]. It was followed by halo implantation to adjust the value of threshold voltage to meet the ITRS requirement [21].

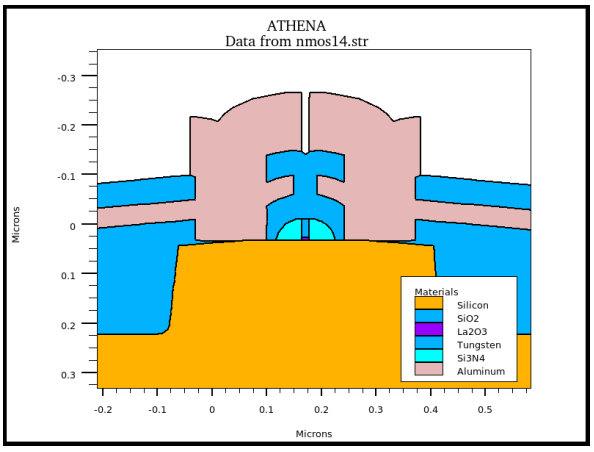

Figure 1: Structure of 14nm NMOS

The data used in the design of 14nm NMOS fabrication recipes are summarized in Table 1. Four HKMG NMOS with 2nm, 3nm, 4 nm and 5nm La_2O_3 thicknesses and 38nm tungsten thickness were fabricated respectively. The design parameters used in the design are summarized in Table 2. Throughout the four different device fabrication steps, all the parameters were kept the same except for halo implantation doses [22]. Halo implantation dose was varied in order to keep the V_{TH} within the ITRS value as the thickness of La_2O_3 were varied from 2nm to 5nm.

Table 1
HKMG NMOS Fabrication Recipes

No	Process Step	NMOS Parameters
1	Silicon substrate	<100> orientation
2	Retrograde well implantation	200Å oxide screen by 970°C, 20 min of dry O_2 4.5 x $10^{11}cm^{-3}$ Phosphorus 30 min, 900°C diffused in nitrogen 36 min, dry O_2
3	STI Isolation	130Å stress buffer by 900°C, 25 min of dry O_2 1500 Å Si_3N_4, applying LPCVD μm photoresist deposition 15 min annealing at 900°C
4	V_{TH} adjust implant	2.75 x $10^{12}cm^{-3}$ Boron difluoride 5keV implant energy, 7° tilt 20 min annealing at 800°C
5	High-k/Metal gate deposition	2 nm/3nm/4nm/5nm La_2O_3 38 nm tungsten 30 min, 900°C annealing
6	LDD Implantation	1.5 x $10^{12}cm^{-3}$ Phosphor 7° tilt
7	Sidewall spacer deposition	0.008 μm Si_3N_4

Table 2
Design Parameters for NMOS

No	Process Parameter	Units	Best Value
1	V_{TH} Implantation Dose	$atom/cm^3$	2.75×10^{12}
2	V_{TH} Implantation Energy	keV	5
3	V_{TH} Implantation Tilt Angle	°	7
4	Halo Implantation Dose	$atom/cm^3$	6.80×10^{13}(2nm) 6.73×10^{13}(3nm) 6.40×10^{13}(4nm) 6.25×10^{13}(5nm)
5	Halo Implantation Energy	keV	140
6	Halo Implantation Tilt Angle	°	30
7	S/D Implantation Dose	$atom/cm^3$	1.0×10^{14}
8	S/D Implantation Energy	keV	12
9	S/D Implantation Tilt Angle	°	7
10	Compensation Implantation Dose	$atom/cm^3$	0.61×10^{14}
11	Compensation Implantation Energy	keV	60
12	Compensation Implantation Tilt Angle	°	7

III. Results and Discussion

The fabricated HKMG NMOS devices were simulated for its electrical behavior using ATLAS module of SILVACO. Figure 2 shows the NMOS load profile with net doping concentrations of the input parameters. Figure 3 shows the characteristic curve between drain current (I_D) and drain voltage (V_D) at gate voltage (V_G) of 1.0V, 1.5V, 2.0V and 2.5V, while Figure 4 and Figure 5 show the plot of I_D versus V_G and sub-threshold I_D versus V_G at V_D = 0.5V and 1.0V respectively for the 14nm NMOS with 2nm-La_2O_3 thickness. I_{ON} and I_{OFF} values are extracted from the sub-

threshold graph as shown in Figure 5. The ratio of I_{ON}/I_{OFF} was then calculated from the values extracted from Figure 5. A good I_{ON}/I_{OFF} ratio is essential for a good signal to noise ratio in circuit operation. Table III shows the comparison of simulated results for V_{TH}, I_{ON}, I_{OFF} and I_{ON}/I_{OFF} ratio of NMOS with 2nm, 3nm, 4nm and 5nm La_2O_3 thickness with ITRS2013 predicted values.

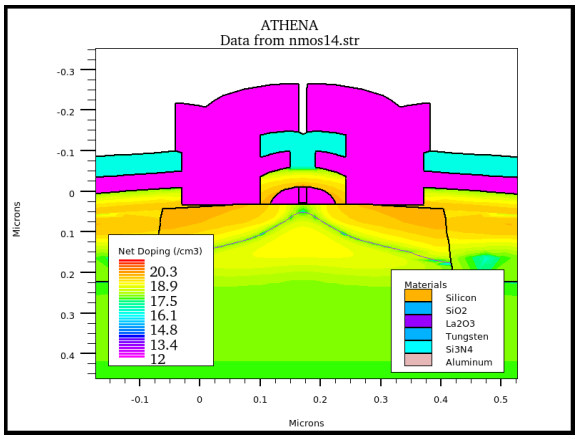

Figure 2: Load profile of 14nm NMOS

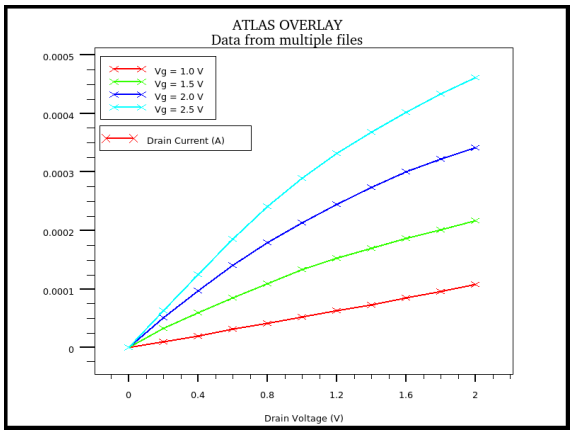

Figure 3: Graph of Drain Current(I_D) versus Drain Voltage(V_D)

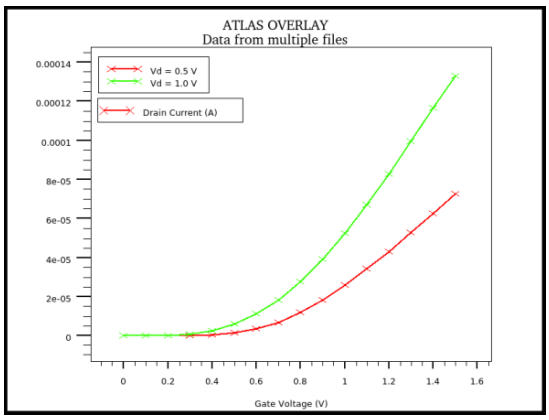

Figure 4: Graph of Drain Current(I_D) versus Gate Voltage(V_G)

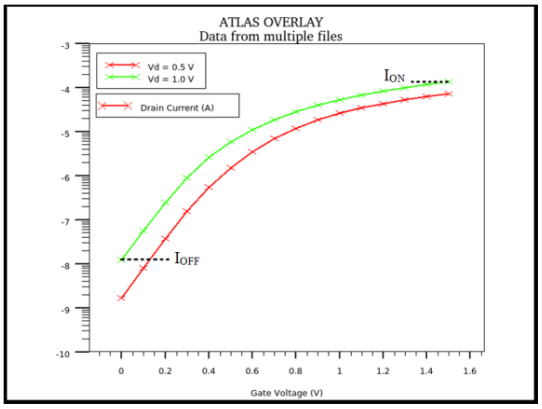

Figure 5: Graph of Sub-threshold Drain current(I_D) versus Gate Voltage(V_G)

Table 3
Simulated Results of Various High-k Thickness with ITRS 2013 Prediction

	Thickness of La_2O_3				ITRS2013 Prediction
	2nm	3nm	4nm	5nm	
V_{TH} (V)	0.216024	0.217559	0.213721	0.215406	0.20079-0.25921
I_{ON} (A/μm)	133	117	108	97.9	1267
I_{OFF} (A/nm)	12.1	19.5	32.7	49.7	100
I_{ON}/I_{OFF}	1.10×10^4	6.01×10^3	3.29×10^3	1.97×10^3	1.3×10^4
V_{TH}(V)	0.216024	0.217559	0.213721	0.215406	0.20079 0.25921

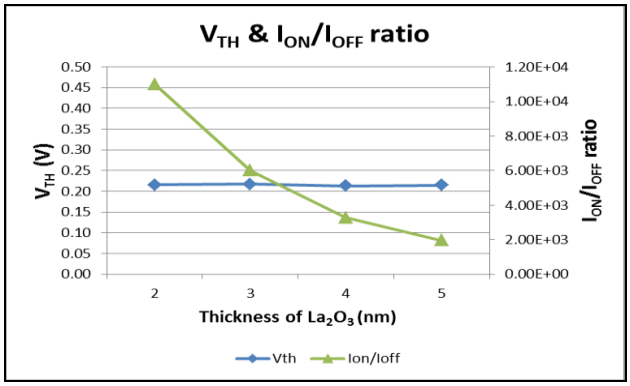

Figure 6: Graph of threshold voltage (V_{TH}) and on/off current ratio (I_{ON}/I_{OFF}) for different La_2O_3 thicknesses

According to ITRS2013, I_{OFF} must be below 100nA/μm as high I_{OFF} degrades the sub-threshold swing and as a consequence, the I_{ON} as well. As the channel length was fixed in the experiment, La_2O_3 thickness and halo implantation are the dominant components in determining the V_{TH} in the NMOS. Halo implantation dose was reduced to keep the V_{TH} at ITRS value as the La_2O_3 thickness was increased.

Figure 6 shows that thinner La_2O_3 are required to achieve better I_{ON}/I_{OFF} ratio while maintaining V_{TH} at a fixed value. The variations of I_{ON} and I_{OFF} with respect to the different La_2O_3 thicknesses are shown in Figure 7. It was observed that I_{ON} reduced while I_{OFF} increased as the La_2O_3 thickness increased. The thickness control of ultrathin high-k dielectric below 2nm to produce the smooth film is considered very challenging with the current technology. It

is observed that I_{ON} and I_{ON}/I_{OFF} ratio increases with the decrease in La_2O_3 thickness.

A higher I_{ON}/I_{OFF} ratio means faster switching for the NMOS. Figure 8 shows that the reduction of halo implantation dose is required to keep the V_{TH} at the required level as the thickness of La_2O_3 increases. However, non-linear relationship between the two variables was observed. Figure 9 shows the effect of variation of La_2O_3 thickness on halo implantation dose and I_{OFF}. Halo implant was adopted to suppress the SCE and control the leakage current. It was observed that I_{OFF} was minimized by having thicker La_2O_3 layer as shown in Figure 9.

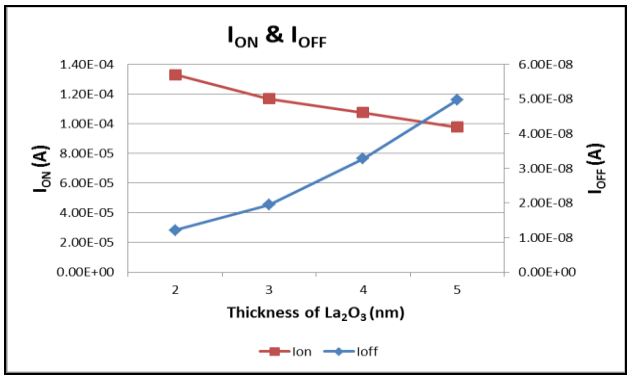

Figure 7: Graph of on-current (I_{ON}) and off current (I_{OFF}) for different La_2O_3 thickness

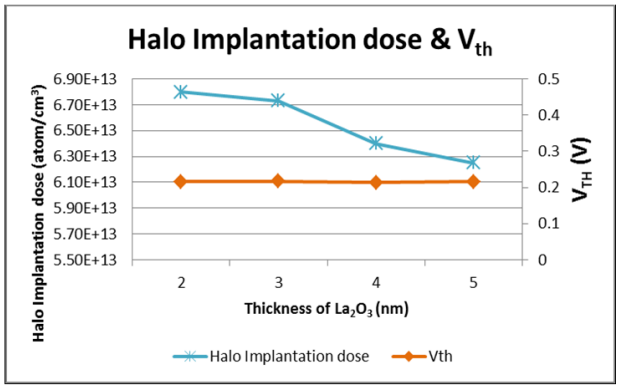

Figure 8: Graph of Halo Implantation dose and threshold voltage (V_{TH}) for different La_2O_3 thicknesses

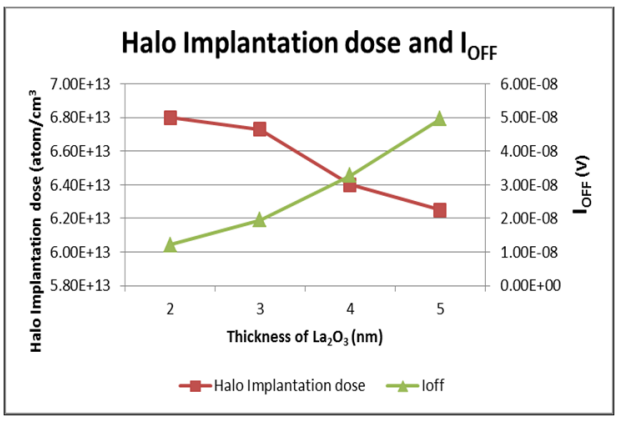

Figure 9: Graph of Halo Implantation dose and off-current (I_{OFF}) for different La_2O_3 thickness

IV. Conclusion

In this study, the effect of adjusting halo implant dose to maintain the V_{TH} for various high-k material thicknesses on 14nm NMOS were comprehensively investigated. It was observed that I_{ON}/I_{OFF} ratio increased with reduced thickness of La_2O_3 dielectric. The dependence of I_{ON}/I_{OFF} ratio on the high-k thickness can be observed.

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