CURRENT-VOLTAGE ANALYSIS OF NANOSCALE PLANAR AND VERTICAL MOSFET INCORPORATING DIELECTRIC POCKET

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Abstract

Characterization of nanoscale planar and vertical metal-oxide-semiconductor field effect transistor incorporating dielectric pocket (DP-MOSFET) is demonstrated by using numerical simulation. Vertical MOSFET is one solution to shrink the channel length (L_g) into nanometer regime. The comparison between planar and vertical MOSFET was done to show an advantages of dielectric pocket and each performances in current-voltage analysis. Dielectric pocket is incorporated between the channel and source/drain for suppression of short-channel effects (SCE) and bulk punch-through. The current-voltage analysis for both structure shows rational value of threshold voltage (V_T), drive current (I_{ON}), off-state leakage current (I_{OFF}), subthreshold swing (S) and Drain Induced Barrier Lowering (DIBL). A better control of VT roll-off was also demonstrated by incorporation of DP and better for vertical MOSFET compared to planar MOSFET. Thus, the incorporation of DP will enhance the electrical performance and give a very good control of the SCE for scaling the MOSFET in nanometer regime for future development of nanoelectronics product.

Keywords: *Vertical, planar, dielectric pocket, SCE, DIBL.*

I. INTRODUCTION

AS the MOSFET undergoes scaling down of the size in order to improve integrated circuit performance such as speed, power consumption, and packing density, a number of challenges need to be overcome. This improvement in device speed and scaling down of device dimensions has continued successfully for over 30 years and the channel length is now in the sub-100 nm regime. As Complementary Metal Oxide Semiconductor (CMOS) channel lengths shrink in order to improve performance, lithography, gate oxide thickness, junction depth limits and short channel effects have proved to be major limitations. Revolutionary technology and fundamental device physics approach are required to meet the above challenges. Possible solutions include new materials and new device structures [1-2].

In current deep submicron MOSFET technology, pocket implantation appears to be a commonly used strategy for suppressing short-channel effects (SCE) [3]. However, shrinking the channel length causes many inconveniences such as an increase of the body factor and junction capacitance as well as the junction leakage current. Besides, high doping increases the risk of avalanche breakdown at the drain/substrate junction. Another problem relating to pockets consists of an increase of threshold voltage fluctuations that they induce. Instead of reducing the junction depth, dielectric pockets that limit dopant diffusion in planar MOSFETs have been proposed [4]. This achievement is able to overcome all of the above-mentioned problems and efficiently suppress SCE.
Recently, vertical MOSFETs, especially fully-depleted surround-gate transistors, have been shown to overcome these

process limitations. A vertical MOSFET arranges the source, channel and drain vertically [5, 6]. The gate electrode surrounds a Si pillar, and the channel region exists at the surface of the sidewalls of the Si pillar. There are several advantages to this device structure. The gate length can be adjusted by the height of the pillar and is independent of lithography. Another advantage of the vertical MOSFET is that the channel width is large even in a small-occupied area because all the sidewalls of the pillar can be used as the channel region. Therefore, the packing density can be increased with this device structure [7, 8]. In this paper, the combination of dielectric pocket and vertical MOSFET was done and compared with planar DP-MOSFET successfully.

II. DEVICE STRUCTURE AND MODELING

The device structure was designed and simulated using SILVACO (ATLAS) software package. Figure 1 shows the simulated planar DP-MOSFET device structure with all the dimension of respective region explicitly shown.

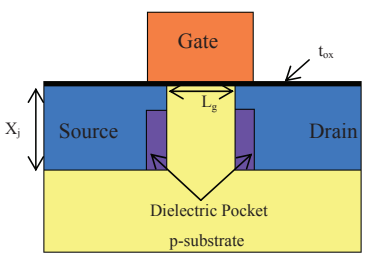

Figure 1 Schematic structure of a planar DP-MOSFET.

The device consists of a silicon semiconductor substrate with uniform boron doping of 10^{18} cm^{-3} on which a thin layer of insulating oxide (SiO_2) is grown. A conducting layer called the polysilicon gate electrode is deposited on top of the oxide. The gate is heavily doped with arsenic of 10^{20} cm^{-3}. Two heavily arsenic doped of 10^{20} cm^{-3} regions with depth X_j = 100 nm, called the source and the drain are formed in the substrate on either side of the gate. The source and the drain regions overlap slightly with the gate. The channel length region of 50 nm is designed for an analysis of the characteristics. The width and height of the dielectric pocket is 30 nm and 70 nm, respectively. A heavily dense mesh is needed in critical regions such as the channel, DP area and gate oxide for accurate characterization of the device.

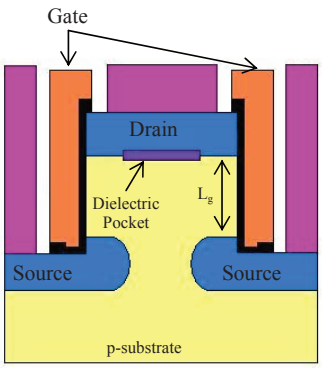

Figure 2 Schematic structure of vertical DP-MOSFET.

Figure 2 shows the vertical DP-MOSFET device structure. As the name implies, in the vertical MOSFET the channel is vertical. A silicon semiconductor with uniform boron doping of 10^{18} cm^{-3} is use as substrate on which a silicon pillar is etched followed by implanting drain and source regions with uniform arsenic doping of 10^{20} cm^{-3}. Then, gate oxide is grown on the vertical sidewall surfaces. N+ polysilicon gates are deposited on the oxide and then etched in particular regions to form the gates. Contact holes are formed at the source and drain regions and aluminum is deposited to make the contacts. As planar DP-MOSFET, a heavily dense mesh is needed in critical regions such as channel, DP area and gate oxide for accurate characterization of the device.

The inversion layer mobility model from Lombardi [9] was employed for its dependency on the transverse field (i.e field in the direction perpendicular $E^{\perp}$ to the Si/SiO_2 interface of the MOSFET) and through velocity saturation at high

longitudinal field (i.e field in the direction from source-to drain parallel E to the Si/SiO_2 interface) combined with SRH (Shockley-Read-Hall Recombination) with fixed carrier lifetimes models [9].

This recombination model was selected since it takes into account the phonon transitions effect due to the presence of a trap (or defect) within the forbidden gap of the semiconductor. An interface fixed oxide charge of 3 x 1010 Coulomb is assumed with the used of n-type polysilicon gate contact for the device. The Drift-Diffusion transport [9] model with simplified Boltzmann carrier statistics [9] is employed for numerical computation of the designed device.

III. RESULTS AND DISCUSSION

The combination of Gummel and Newton numerical methods was employed for a better initial guess in solving quantities for obtaining a convergence of the device structure. Figure 3 shows the comparison of current-voltage (I_{GS}-V_{GS}) characteristics between planar and vertical DP-MOSFET device with channel length L_g = 50 nm, body channel doping of 10^{18} cm^{-3} and taken at V_{DS} = 0.1 V and 1.0 V. By using a linear extrapolation of transconductance gm (V_{GS}) to zero [6] a 0.09 V threshold voltage, V_T for planar DP-MOSFET device was obtained at V_{DS} = 0.1 V and reduce to -0.21 V at V_{DS} = 1.0 V. The threshold voltage of the vertical DP-MOSFET is higher than that of the planar DP-MOSFET which V_T = 1.06 V for V_{DS} = 0.1 V and VT = 0.65 V at VDS = 1.0 V. The moderately high VT was expected since the vertical DP-MOSFET device has less short-channel effects than non-extended planar DP-MOSFET.

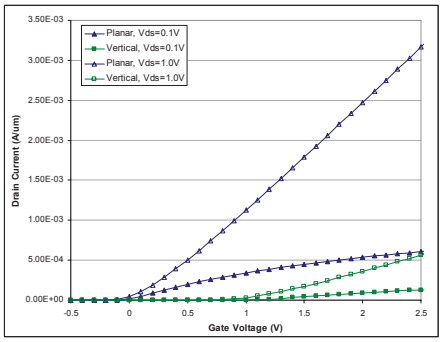

Figure 3 Current-Voltage characteristic of planar and vertical DP-MOSFET taken at V_{DS}=0.1V and V_{DS}=1.0V.

In the off-state operation mode the transistors show a drain leakage current I_{OFF} which is independent of the gate voltage, but increases with increasing drain voltage as depicted in Figure 4. I_{OFF} of the planar DP-MOSFET is very high when it is biased at maximum drain voltage and is lower in the vertical DP-MOSFET. In planar DP-MOSFET, an off-state leakage current, I_{OFF} = 1.35 x 10^{-5} A/μm and drive current, I_{ON} = 5.36 x 10^{-4} A/μm taken at V_{DS} = 0.1 V while I_{OFF} = 4.29 x 10^{-5} A/μm and I_{ON} = 2.47 x 10^{-3} A/μm taken at V_{DS} = 1.0 V was explicitly shown. In vertical DP-MOSFET, the I_{OFF} was reduced to 9.63 x 10^{-15} A/μm at V_{DS} = 0.1 V and 2.77 x 10-12 A/μm at V_{DS} = 1.0 V while I_{ON} = 9.14 x 10^{-5} A/μm and 3.6 x 10^{-4} A/μm taken at V_{DS} = 0.1 V and 1.0 V. The off-state drain current was measured at V_{GS} = 0 V and the on-state drain current is measured when V_{GS} - V_T = 1 V. To find the origin of this leakage, the currents from all electrodes of the device have been measured simultaneously. This shows that the leakage current origins from the reverse biased drain-substrate diode. Due to a good I_{OFF}/I_{ON} ratio of the devices, the subthreshold characteristics also highlighted a reasonably well-controlled SCE with subthreshold swing SubV_T = 85 mV/dec and 39 mV/dec taken at V_{DS} = 0.1 V and increase to 108 mV/dec and 65 mV/dec taken at V_{DS} = 1.0 V for planar and vertical DP-MOSFET. In addition as shown in Figure 5, the output characteristic was also highlighted a very

good drain current for both planar and vertical DP-MOSFET. The drain current was measured at different gate voltage (V_{GS} = 1.1 V and 2.2 V) with increasing drain voltage. It also shows no avalanche breakdown within the specified voltage range for the 50 nm device.

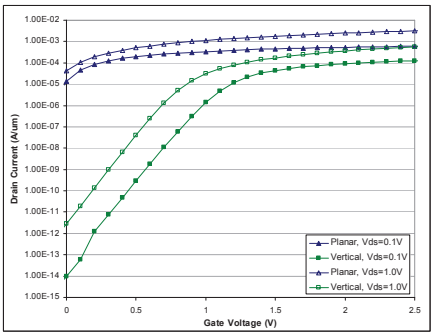

Figure 4 Transfer characteristic of planar and vertical DP-MOSFET device taken at V_{DS}=0.1V, V_{DS}=1.0V and V_S=V_B=0V

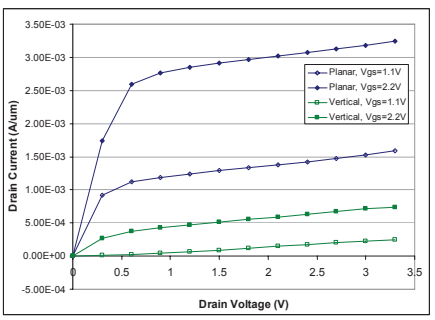

Figure 5 Output characteristic of planar and vertical DP-MOSFET with L_g=50nm for V_{GS}=1.1V and 2.2V.

IV. CONCLUSION

In conclusion, the results described above indicated a better performance depends on I-V characteristics demonstrated by incorporation of DP and better for vertical MOSFET compared to planar MOSFET. Thus, the incorporation of DP will enhance the electrical performance and give a very good control of the SCE for scaling the MOSFET in nanometer regime for future development of nano-electronics product.

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