IMPACT OF SALICIDE AND SOURCE/DRAIN IMPLANTS ON LEAKAGE CURRENT AND SHEET RESISTANCE IN 45NM NMOS DEVICE

F.Salehuddin[1], I.Ahmad1, F.A.Hamid[1], A.Zaharim[2], H.A.Elgomati[3], B.Y.Majlis[3]

[1]College of Engineering,
Universiti Tenaga Nasional (UNITEN)
43009 Kajang, Selangor, Malaysia

[2]Faculty of Engineering and Built Environment,
Universiti Kebangsaan Malaysia (UKM)
Bangi, Selangor, Malaysia

[3]Institute of Microengineering and Nanoelectronic,
Universiti Kebangsaan Malaysia (UKM)
43600 Bangi, Selangor, Malaysia

fauziyah@utem.edu.my, aibrahim@uniten.edu.my,
fazrena@uniten.edu.my, burhan@eng.ukm.my

Abstract

In this paper, we investigate the impact of Source/Drain (S/D) implant and salicide on poly sheet resistance (RS) and leakage current (I_{Leak}) in 45nm NMOS device performance. The experimental studies were conducted under varying four process parameters, namely Halo implant, Source/Drain Implant, Oxide Growth Temperature and Silicide Anneal Temperature. Taguchi Method was used to determine the settings of process parameters. The level of importance of the process parameters on the R_S and I_{Leak} were determined by using analysis of variance (ANOVA). The fabrication of the devices was performed by using fabrication simulator of ATHENA. The electrical characterization of the device was implemented by using electrical characterization simulator of ATLAS. These two simulators were combined with Taguchi method to aid in design and optimizing the process parameters. The optimum process parameter combination was obtained by using the analysis of signal-to-noise (S/N) ratio. In this research, the most effective process parameters with respect to poly sheet resistance and leakage current are silicide anneal temperature (88%) and S/D implant (62%) respectively. Whereas the second ranking factor affecting the poly sheet resistance and leakage current are S/D implant (12%) and silicide anneal temperature (20%) respectively. As conclusions, S/D implant and silicide anneal temperature have the strongest effect on the response characteristics. The results show that the R_S and I_{Leak} after optimizations approaches are 42.28□□ and 0.1186mA/□m respectively.

Keywords: *45nm NMOS, S/D implant, SALICIDE, Taguchi Method..*

I. INTRODUCTION

The scaling of the Complementary Metal-Oxide Semiconductor (CMOS) devices to smaller physical dimensions has become the driving force for the semiconductor industry to meet the market's demand for greater functionality and performance of the integrated circuit at a low cost. This was the primary activity of advanced device development almost since the basic technology was established. In CMOS, polysilicon gate is widely used. For sub-nanometer (less than 100nm) devices, the silicide growth is being applied on the top of polysilicon in order to produce better devices. A silicide is a compound that has silicon with more electropositive elements. Metal such as tungsten, titanium, cobalt and nickel, is alloyed with the top layers of the polysilicon. These metals react with

polysilicon to form the metal silicide layer that posses better physical and electrical properties to interface with aluminum. The process in which silicide is formed on both the gate electrode and the source and drain regions is sometimes called self-aligned silicide (SALICIDE) [1,2]. The term salicide refers to a technology used in the microelectronics industry used to form electrical contacts between the semiconductor device and the supporting interconnect structure. The salicide technology has been widely used to reduce sheet resistance of polysilicon gates. This is because the sheet resistance will be the major limiting factor of the device performance [3].

Metal-Oxide Semiconductor MOS process invariability use ion implantation into the channel region, which alters the doping profile near the surface of silicon substrate. Ion implantation is processes by which dopant ions are forcefully add into the semiconductor in the form of energetic ion beam injection [4]. The ion implantation process provides much more precise control of doping than the diffusion process [5]. By changing dose, energy and rotation of these implants can change the profile and the electrical characteristics of the device.

In this paper, for identify semiconductor process parameters would impact most on the device characteristics is realized using Taguchi Method. Taguchi method is being applied to reduce development time and to ensure that the products are in the acceptable quality range [6]. Optimization of process parameters is the key step in the Taguchi method to achieve high quality without increasing cost. Taguchi's parameter design method is an important tool for robust design, where the optimal process parameters obtained from the Taguchi method are insensitive to the variation of environmental conditions and other noise factor. The Taguchi method involves an analysis that reveals which of the factors are most effective in reaching the goals and the directions in which these factors should be adjusted to improving the results [7]. The method using an array set is known as Taguchi orthogonal L_9 array method. By using an orthogonal array to design the experiment could help the designers to study the influence of multiple controllable factors on the average of quality characteristics and the variations in a fast and economic way, while using a signal-to-nose ratio to analyze the experimental data could help the designers of the product or the manufacturer easily to find out the optimal parametric combinations [8].

II. MATERIAL AND METHODS

Sample used in these experiments were <100> orienting and p-type (boron doped) silicon wafers. P-wells was created starting with developing a 200Å oxide layer on the wafers followed by boron doping. The oxide layer was etched after the doping process was completed. It was followed by annealing process to strengthen the structure. Next, STI was developed to isolate neighbouring transistor. A 130Å stress buffer was developed on the wafers with 25-minute diffusion processes. Then, a 1500Å nitride layer was deposited using the Low Pressure Chemical Vapour Deposition (LPCVD) process. This thin nitride layer was acted as the mask when silicon was etched to expose the STI area. Photo resistor layer was then deposited on the wafers and unnecessary part will be removed using the Reactive Ion Etching (RIE) process. An oxide layer was developed on the trench sides to eliminate any items from entering the silicon substrate. Chemical Mechanical polishing (CMP) was then applied to eliminate extra oxide on the wafers. Lastly, STI was annealed for 15 minutes at 900oC temperature. A sacrificial oxide layer was then developed and etched to eliminate defects on the surface.

The gate oxide was grown and a Boron Difluoride (BF_2) threshold-adjustment implant was done in the channel region through this oxide. The polysilicon gate was then laid and defined followed by the halo implantation. In order to get an

optimum performance for NMOS device, indium was doped. Halo implantation was followed by developing sidewall spacers. Sidewall spacers were then used as a mask for source/drain implantation. Arsenic atom was implanted at a desired concentration to ensure the smooth current flow in NMOS device.

Silicide layer was then annealed on the top of polysilicon. The next step in this process was the development of Boron Phosphor Silicate Glass (BPSG) layer. This layer will be acted as Premetal Dielectric (PMD), which is the first layer deposited on the wafer surface when a transistor was produced. This transistor was then connected with aluminum metal. After this process, the second aluminum layer was deposited on the top of the Intel Metal Dielectric (IMD) and unwanted aluminum was etched to develop the contacts [9,10]. The procedure was completed after the metallization and etching were performed for the electrode formation and the bonding pads were opened. Once the devices were built with ATHENA, the complete devices can be simulated in ATLAS to provide specific characteristics such as the I_D versus V_{GS} curve. The threshold voltage (V_{TH}) can be extracted from that curve [11].

A. Taguchi Orthogonal L_9 Array Method

The optimizations of the NMOS device has been done by changing individual process parameters (factors) laid out by the ATHENA [11]. The factors that were modified and examined include: halo implant, S/D implant, oxide growth temperature and silicide anneal temperature. The value of the process parameter at the different levels is listed in Table 1.

Table 1:Process Parameters And Their Levels

Symbol	Process Parameter	Unit	Level 1	Level 2	Level 3
A	Halo Implant	atom/ cm^3	3.25E13	3.28E13	3.30E13
B	S/D Implant	atom/ cm^3	5.80E14	5.82E14	5.86E14
C	Oxide Growth Temp	°C	815	820	821
D	Silicide Anneal Temp	°C	900	910	950

In this research, an $L_9(3^4)$ orthogonal array which has 9 experiments was used. The experimental layout for the process parameters using the $L_9(3^4)$ orthogonal array is shown in Table 2.

Table 2: Experimental Layout Using $L_9(3^4)$ Orthogonal Array

Exp. No.	Process Parameter level A Halo Implant	B S/D Implant	C Oxide Growth Temp	D Silicide Anneal Temp
1	1	1	1	1
2	1	2	2	2
3	1	3	3	3
4	2	1	2	3
5	2	2	3	1
6	2	3	1	2
7	3	1	3	2
8	3	2	1	3
9	3	3	2	1

III. RESULT AND ANALYSIS

The fabrication result of the first set experiment that has been done by using ATHENA module was discussed. The result obtained shows from fabrication process and electrical characteristics NMOS device. Beside that, this section also shows the optimization result of NMOS device by using Taguchi Method Approach.

A. 45nm Transistor Fabrication

Fig. 1 shows the graph of I_D versus V_G at V_D=0.05V and V_D=1.1V for NMOS devices. The threshold voltage value is 0.1545V. These values are still in range ±12.7% from the nominal values. The nominal value of threshold voltage for NMOS is 0.15V [12]. At V_{TH}=0.1545V, the values of poly sheet resistance and leakage current are 42.78Ω/□ and 0.125mA/μm respectively.

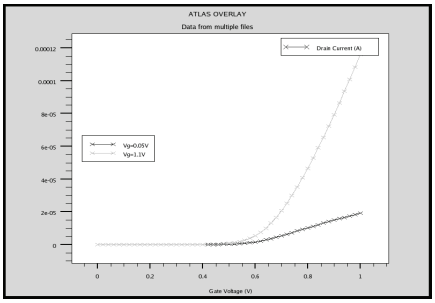

Fig. 1 Graph ID-VG for 45nm NMOS device

The results of RS and ILeak were then analyzed and processed with Taguchi Method to get the optimal design. The optimized result from Taguchi Method was then simulated in order to verify the predicted optimal design.

B. Analysis of Effect Process Parameters to Poly Sheet Resistance and Leakage Current

The results of poly sheet resistance and leakage current for NMOS device using the L_9 orthogonal array are shown in Tables 3 and 4 respectively.

Table 3: R_s Values For Nmos Device

Exp. No	Poly Sheet Resistance (Ω/□)			
	R_S 1	R_S 2	R_S 3	R_S 4
1	42.7752	42.7723	42.7723	42.7763
2	42.5984	42.5950	42.5954	42.5948
3	42.0633	42.0541	42.0595	42.0610
4	42.2752	42.2519	42.2705	42.2699
5	42.7187	42.7160	42.7177	42.7187
6	42.4754	42.4723	42.4728	42.4767
7	42.6864	42.6835	42.6842	42.6857
8	42.2148	42.2076	42.2120	42.2154
9	42.5933	42.5958	42.5904	42.5896

Table 4: I_{LEAK} Values For Nmos Device

Exp. No	Leakage Current (mA/μm)			
	I_{Leak} 1	I_{Leak} 2	I_{Leak} 3	I_{Leak} 4
1	0.125042	0.123929	0.124456	0.124744
2	0.127775	0.126668	0.127190	0.127354
3	0.134437	0.133246	0.133883	0.134195
4	0.121709	0.120714	0.121145	0.121274
5	0.122649	0.121494	0.122085	0.12235
6	0.128150	0.127103	0.127567	0.127877
7	0.117182	0.116029	0.116628	0.116905
8	0.121127	0.120056	0.120562	0.12086
9	0.124627	0.123528	0.124046	0.124230

After nine experiments of L_9 array have been done, the next step is to determine the required values for selected factors, which are halo implant, S/D implant, oxide growth temperature and silicide anneal temperature that gave the effect to a device. Poly sheet resistance and leakage current of the 45nm devices belongs to the smaller-the-best quality characteristics. The S/N Ratio, η of the smaller-the-best quality characteristics can be expressed as [8,13]:

$$\eta = 10\mathrm{Log}_{10}\left[\frac{1}{n}\sum\left(Y_1^2 + Y_2^2 + \ldots + Y_n^2\right)\right] \quad (1)$$

Where n is the number of tests and Yi the experimental value of the poly sheet resistance and leakage current. By applying Equation (1), the η for each device were calculated and given in Table 5. The effect of each process parameter on the S/N Ratio at different levels can be separated out because the experimental design is orthogonal. The S/N ratio for each level of the process parameters is summarized in Table 6. In addition, the total mean of the S/N ratio for the 9 experiments is also calculated and listed in Table 6.

Table 5: S/N Ratios For NMOS Device

Exp. No	S/N Ratio (dB)	
	Poly Sheet Resistance	Leakage Current
1	-32.62	79.34
2	-32.59	77.91
3	-32.48	77.46
4	-32.52	78.33
5	-32.61	78.26
6	-32.56	77.88
7	-32.61	78.66
8	-32.51	78.37
9	-32.59	78.12

Table 6
S/N REsponses For The Threshold Voltage In NMOS Device

Parameter	Symbol	Process Parameter	S/N Ratio (Smaller-the-Best) Level 1	Level 2	Level 3	Total Mean S/N	Max - Min
R_S	A	Halo Implant.	-32.56	-32.56	-32.57	-32.56	0.01
	B	S/D Implant.	-32.58	-32.57	-32.54		0.04
	C	Oxide Growth Temp.	-32.56	-32.56	-32.56		0.00
	D	Silicide Anneal Temp.	-32.61	-32.59	-32.50		0.11
I_{Leak}	A	Halo Implant.	78.24	78.16	78.38	78.26	0.22
	B	S/D Implant.	78.78	78.18	77.82		0.96
	C	Oxide Growth Temp.	78.53	78.12	78.13		0.41
	D	Silicide Anneal Temp.	78.58	78.15	78.05		0.53

Fig. 2 and Fig. 3 show the S/N ratio graphs where the dashed line is the value of the total mean of the S/N ratio. Basically, the larger the S/N ratio, the quality characteristic for the poly sheet resistance and leakage current are better [8,13].

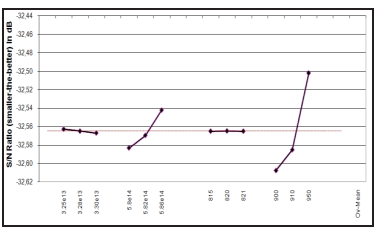

Fig. 2 S/N graph for poly sheet resistance in NMOS Device

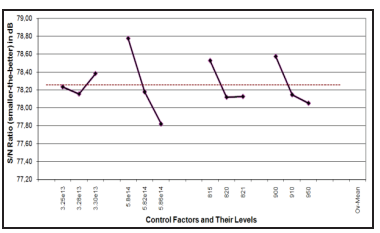

Fig. 3 S/N graph for leakage current in NMOS Device

C. Analysis of variance (ANOVA)

A better feel for the relative effect of the different process parameter on the poly sheet resistance (R_S) and leakage current (I_{Leak}) were obtained by decomposition of variance, which is called analysis of variance (ANOVA) [6]. The results of ANOVA for the R_S and I_{Leak} in NMOS device are presented in Table 7 and Table 8 respectively. Statistically, F-test provides a decision at some confidence level as to whether these estimates are significantly different. Larger F-value indicates that the variation of the process parameter makes a big change on the performance [8].

According to Table 7, the most effective process parameters with respect to poly sheet resistance are silicide anneal temperature, S/D implant, halo implant and oxide growth temperature. Percent factor effect indicates the relative power of a factor to reduce variation. For a factor with a high percent contribution will have a great influence on the performance. Referring to Table 8, the most effective process parameters with respect to leakage current are S/D implant, silicide anneal temperature, oxide growth temperature and halo implant. According to Table 7 and Table 8, silicide anneal temperature and S/D implant were found to be the major factor affecting the poly sheet resistance and leakage current respectively.

Table 7
Results Of Anova For R_s In NMOS Device

Symbol	Process Parameter	Degree of Freedom	Sum of Square	Mean square	F-Value	Contribution percentage
A	Halo Implant.	2	0	0	0	0
B	S/D Implant.	2	0	0	6	12
C	Oxide Growth Temp.	2	0	0	0	0
D	Silicide Anneal Temp.	2	0	0	44	88

[a] *At least 95% confidence*

Table 8
Results Of Anova For ILEAK In NMOS Device

Symbol	Process Parameter	Degree of Freedom	Sum of Square	Mean square	F-Value	Contribution percentage
A	Halo Implant.	2	0	0	2	4
B	S/D Implant.	2	1	1	31	62
C	Oxide Growth Temp.	2	0	0	7	14
D	Silicide Anneal Temp.	2	0	0	10	20

[a]*At least 95% confidence*

D. Confirmation Test

The confirmation experiment is the final step in the first interaction of the design of the experiment process. The purpose of the confirmation experiment is to validate the conclusions drawn during the analysis phase [6,8]. The confirmation experiment is performed by conducting a test with a specific combination of the factors and levels previously evaluated. After determining the optimum conditions and predicting the response under these conditions, a new experiment was designed and conducted with the optimum levels of the process parameters. The results of experimental confirmation using optimal process parameters and comparison of the predicted poly sheet resistance and leakage current with the actual poly sheet resistance and leakage current using the optimal process parameters are shown in Table 9. The improvement in percentage from the starting process parameters to the level of optimal process parameters is 0.47% and 6.68% for poly sheet resistance (42.28Ω/□) and leakage current (0.1186mA/μm) respectively. Therefore, the poly sheet resistance and leakage current are improved by using the Taguchi method.

Table 9:Results Of The Confirmation Experiment

	Process Parameter Settings	R_S (Ω/□□)		I_{Leak} (mA/μm)	
		Predicted	Observed	Predicted	Observed
Nominal	$A_2B_3C_1D_2$	42.61	42.48	0.1276	0.1271
Optimum	$A_3B_1C_1D_3$	42.32	42.28	0.1129	0.1186
Improvement (%)		0.68%	0.47%	11.5%	6.68%

This design method gave 9 set experiments. It has many variants that can be applied to the modeling device and a lot of parameters can be used. It is proven on time saving and the result is good according to objective and desired of the project. It easily to do 9 experiments in comparison to 81 experiments that might develop from 4 process parameters for 3 levels. Then, the analysis of variance shows the process parameter of S/D implant and silicide anneal temperature are significant based on 95% confidence level towards poly sheet resistance and leakage current respond. So that the poly sheet resistance and leakage current decreased follows the silicide anneal temperature and S/D implant doping. Analysis of variance also proved the factor of oxide growth temperature is significant towards leakage current respond.

ACKNOWLEDGMENT

The authors would like to thank the Ministry of Higher Education (MOHE) for their financial support and the Universiti Teknikal Malaysia Melaka (UTeM) for awarding a study leave to one of the authors.

REFERENCES

[1] Sung-Mo Kang, Yusuf Leblebici, "CMOS digital integrated circuit: analysis and design", McGarw-Hill Higher Companies, Inc., 3th Edition, 2003.

[2] P.D Agnello *et.al.*, "Process Requirements fo Continued Scaling of CMOS- the need and prospects for atomic level manipulation", IBM J. Res. & Dev. 46, No. 2/3, 2002.

[3] Hiroshi Iwai, Shun'ichiro Ohmi, "Silicon integrated circuit technology from past to future", Microelectronic Reliability, 2002, pp.465-491

[4] Hani Noorashiqin Abd. Majid, "Optimization and characterization of 130nm CMOS Transistor design Using TCAD Simulation", M.S. thesis, University of Malaya, 2007.

[5] S.M.Sze, Semiconductor Devices: Physics and Technology, John Wiley & Sons Inc, 2nd Edition, 1986.

[6] H.Abdullah, J.Jurait, A.Lennie, Z.M.Nopiah, I.Ahmad, "Simulation of Fabrication Process VDMOSFET Transistor Using Silvaco Software", European Journal of Scientific Research, ISSN 1450-216X, Vol.29 No.4, pp. 461-470, 2009.

[7] Douglas C. Montgomery, Design and Analysis of Experiments, John Wiley & Sons Inc., 6th Edition. 2005

[8] Ugur Esme, "Application of Taguchi Method for the Optimization of Resistance Spot Welding Process", The Arabian Journal for Science and Engineering, Vol. 34, No. 2B, 2009.

[9] Husam Ahmed Elgomati, "Characterizing Cobalt Silicide and Gate Dielectric Thickness in 65nm NMOS Device", M.S. Thesis, Universiti Kebangsaan Malaysia. 2007.

[10] Belal Ahmed Hamida "Optimization of pMOS 65nm Using Taguchi Method", M.S. Thesis, Universiti Kebangsaan Malaysia. 2007.

[11] Ashok K.Goel et al., "Optimization of Device Performance Using Semiconductor TCAD Tools", Silvaco International, Product Description, Silvaco International, 1995.

[12] ITRS 2007 Report; http://www.itrs.net

[13] N.V.R.Naidu, "Mathematical model for quality cost optimization, Robotics and Computer-integrated Manufacturing", Vol.24, Issue 6, 17th International Conference on Flexible Automation and Intelligent Manufacturing, pp. 811-815, 2008