Implementation of a 4-bit Ripple Carry Full Adder of Mirror Design Style Using Synopsys Generic 90nm Technology on a Full-Custom and Semi-Custom Design

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***Abstract*—The most frequently used component in the datapath block and the speed-limiting element is the adder. Because of this, it is essential to optimize the adder knowing it has a big impact on the overall system performance. In addition to that, adders are a very important subsystem in digital designs, thus, taking care about its performance must be spotted. By manipulating the transistor sizes and circuit topology, the speed can be optimized. A circuit of a CMOS (Complementary metal oxide semiconductor) 4-bit RCA (Ripple Carry Adder) is presented. The proposed adder cell refers to the CMOS adder class executed on CMOS mirror design style that has a smaller area and delay compared with the static adder implementation of the full adder. By simply cascading full-adder blocks, one obtains a Ripple-Carry Adder which perhaps the simplest to implement than that of the other carry adders. Creating the full adder in schematic diagram is a part of Pre-simulation. It incorporates the construction of CMOS transistors and connected through the use of wires. Widths and lengths of the transistors are the crucial parts in designing to place and route connections easily. Layout diagram is the equivalent of the schematic diagram but more on a detailed part and it should be the same as the transistor based circuit. With the aid of the verification processes such as DRC (Design Rule Check) and LVS (Layout versus Schematic), it can give an assurance that both the schematic and layout diagrams are similar and functioning properly.**

***Index Terms*—Full Adder; Layout Diagram; Schematic Diagram; Verification Process.**

I. INTRODUCTION

The adder comprehends the process of adding binary numbers. Addition is a prime operation in formation of basic logical functions of computational systems. It involves steps which includes summation, subtraction, multiplication, division exponentiation, and etc. Furthermore, addition plays a crucial role in the basic types of digital systems; in Digital Signal Processors (DSP), the core of the N-bit adder is one of the most important building blocks and the units of the microprocessors for the accomplishment of the increasing compulsion for speed [1]. This means that, the ^{adder} is the basic block of arithmetic logic units (ALU) and adders are significant blocks of the final signal processing for some of the modern architectures of high-speed analog digital converters (ADC) [2].

Previous researchers have found that teaching VLSI (Very Large Scale Integration) in universities must be constantly updated in order to reflect rapid industry developments. For most of these universities, access to modern CMOS technologies can be difficult due to legal issues and it is also inconvenient for industries due to intellectual property issues [3,4]. Furthermore, the logical style used in adder cells basically influences the speed, size, and power dissipation of the circuits. The number of inversion levels, the number of transistors in series, and transistor sizes determine the circuit delay [5]. Circuit size mostly depends on the number of transistors and their sizes [6,7]. All these characteristics may vary considerably from one logic style to another, thus, making the proper choice of logic style crucial for circuit designer to satisfy their needs [8,9].

This study generally aims to implement a 4-bit ripple carry full adder in a mirror design style using full custom and semi-custom design. The study specifically aims to: (1) create and simulate a schematic diagram of full-adder and cascade it to produce a ripple carry full adder; (2) design a layout of a 4-bit ripple carry full adder of mirror design style and compare it to the static CMOS full adder; (3) verify the layout and schematic of the 4-bit ripple carry full adder and; (4) design a Verilog HDL program of the full adder and verify it on an FPGA hardware.

The significance of using Mirror Adder is that the NMOS and PMOS are completely symmetrical which makes it easier for the Layout engineers to route the connections. In addition to that, only the transistors in the carry stage need to be optimized for optimal speed while all the transistors in the sum stage can be at minimal size.

The study will only cover a 4-bit full-adder since a ripple-carry adder operation is only good for not more than 4-bits and only 3 process corners will be used in this research such as TT (typical-typical), FF (fast-fast), and SS (slow-slow) to check if both pmos and nmos devices are affected evenly. For the verification process, parasitic extraction will not be implemented due to lack of software program. Moreover, the technology used in Galaxy Custom Designer is 90nm since it is the only available technology in the Institute. For the hardware part, Altera DE1 board will be used. Conversely, this research will not cover other types of full-adder since this

research only deal with less than 4-bits of information.

II. METHODOLOGY

A. *Full custom design flow using synopsys custom design tools*

Synopsys custom design environment is utilized in this study. The whole custom design flow and tools utilized for respective stage is shown in Figure 1

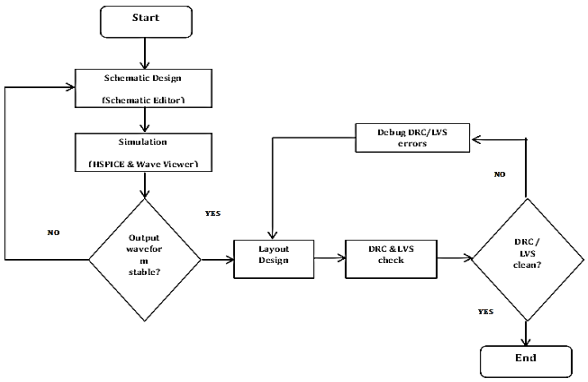

Figure 1: Full Custom Design Flow Chart

B. *Schematic diagram of 4-bit RCA and simulation*

In order for the researcher to create a layout of a cell or block, one must have a schematic diagram. This is where design and layout engineers are starting from to create an analog or digital design. Each full adder block is being cascaded so as to construct the ripple carry adder. Inside each block contains the schematic diagram of a full adder. Figure 2 shows the schematic diagram of a full adder designed in a mirror style.

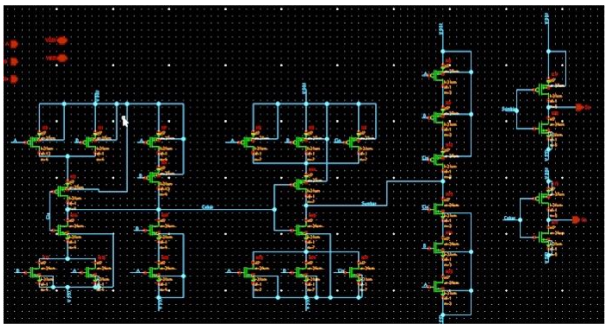

Figure 2: Mirror Full Adder Schematic

C. *Layout of a 4-bit ripple carry full adder*

After creating the schematic diagram, the layout comes next. Having a stick diagram is a means of capturing layer information using simple diagrams. Figure 3 represents the stick diagram for layout of mirror full adder. The stick diagram was used to help create what would become the final layout in Custom designer. The figure also gives the individual transistors as taken from the schematic to ensure the appropriate interfaces were translated into layout. After finishing the layout of a full adder, it will now be instantiated in another cell layout to create a 4-bit ripple carry adder. Since it is a 4-bit full adder, the generated full adder will be instantiated four times and cascaded to follow the schematic diagram. On the other hand, another layout will be created for the static CMOS full adder in order to compare that to the mirror full adder.

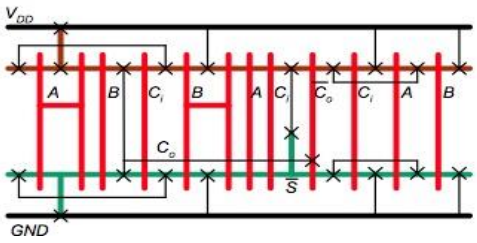

Figure 3: Stick diagram for layout of mirror full adder

D. *Verification of layout and schematic of a 4-bit RCA*

Verifying layout and schematic requires; (1) Design rule checking (DRC) and; (2) Layout vs. Schematic (LVS). Design rule checking is the area of Electronic Design Automation (EDA) that determines whether the physical layout of a particular chip layout that satisfies a series of recommended parameters called Design Rules. Figure 4 shows some of the common basic design rules. A width rule specifies the minimum width of any shape in the design. A spacing rule specifies the minimum distance between two adjacent objects. If design rules are violated, the design may not be functional.

Rule #	Rule description	µm	Mark
DIFF.W.1	Minimum width	0.12	a
DIFF.S.1	Minimum spacing	0.14	b
DIFF.S.2	Minimum spacing in DIFF_25	0.18	c
DIFF.E.1	Source/drain active to well edge (min enclosure by well)	0.24	d
DIFF.E.2	Substrate/well contact diff to well edge (min enclosure by well)	0.2	e
DIFF.R.1	DIFF w/o IMP is not allowed		
DIFF.A.1	Minimum area	0.08^2	f

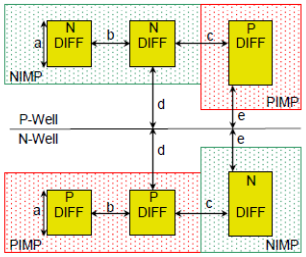

Figure 4: Basic DRC checks – width and spacing

E. *Designing a Verilog HDL program of the full adder and verify on FPGA hardware*

In designing a Verilog HDL program it is necessary to have a background in HDL programming language. Constructing the code will be based on the gate-level diagram to ensure that the code created is functioning similarly to the netlist generated in the full custom design. The Altera DE1 board has many interfaces to work with in order to display the inputs and outputs of the code like switch buttons, push buttons, LEDs, VGA's, etc. In addition to these hardware features, the DE1 board has software support for standard I/O interfaces and a control panel facility for accessing various components. To verify the code that will be created in Verilog is similar to the output produced in full-custom design; Table 1 shows the theoretical output of the full adder.

Table 1
Theoretical output of the full adder

A	B	Cin	Sum	Carry out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

III. RESULT AND DISCUSSION

The circuit was tested using a 90nm CMOS process and pmos4t/nmos4t for transistors working on a 1.2V power supply. By carrying HSPICE simulations with supply, VDD, equal to 1.2V, Temperature at 0 & 49C, and 3 process corners which are TT, FF, and SS. Figure 5 shows the initial output waveform of the RCA adder. Initially, by setting the width sizes of PMOS = 0.7um & NMOS = 0.4um and length = 0.1um, the output waveform is not stable. In addition to that, the 4 Sum outputs (S_0-S_3) and Carry out C_{out} are not synchronized

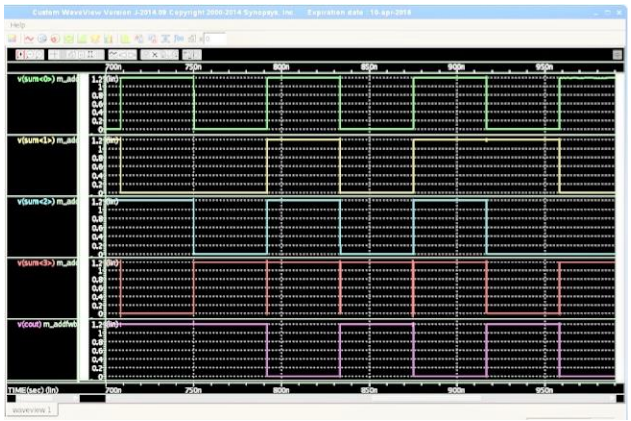

Figure 5: Initial output waveform

By increasing the diffusion of sizes of the transistors and adding buffers for each sum and carry output, it will result to a more stable waveform and less glitches. Figure 6 presents the new Block diagram of 4-bit RCA with buffers and Figure 7 shows the final output waveform of the RCA adder.

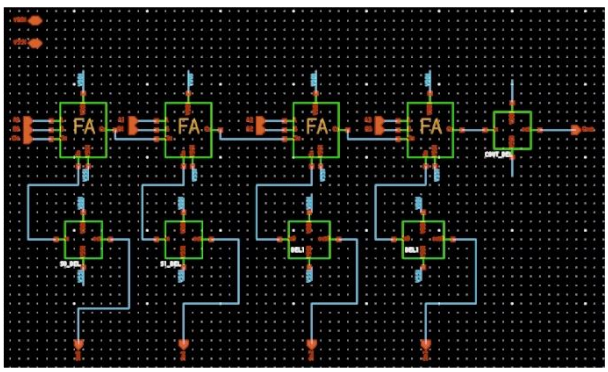

Figure 6: Final block diagram of 4-bit RCA

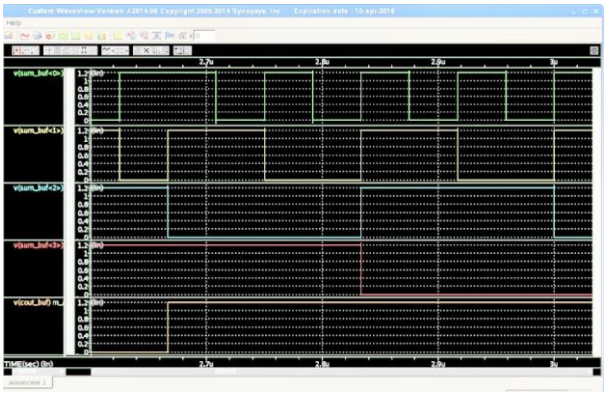

Figure 7: Final output waveform

Creating the layout of the mirror full adder changes from the stick diagram since the diffusion sizes of PMOS and NMOS were modified making it bigger than the stick diagram. Figure 8 shows the layout of 1-bit full adder of mirror design style. In the figure below, the connections on PMOS and NMOS are symmetrical following the mirror design style

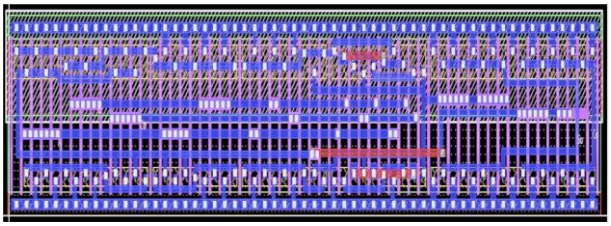

Figure 8: Layout of 1-bit full adder of mirror design style

On the other hand, the 1-bit static CMOS full adder layout is way different. There are some connections that cannot be connected by M1 (metal1) due to lack of spaces which requires us to use the M2 layer and VIA1 (used to connect M1 layer to M2 layer). Furthermore, the connections for PMOS and NMOS are totally not the same. Figure 9 illustrates the layout of 1-bit static CMOS full adder.

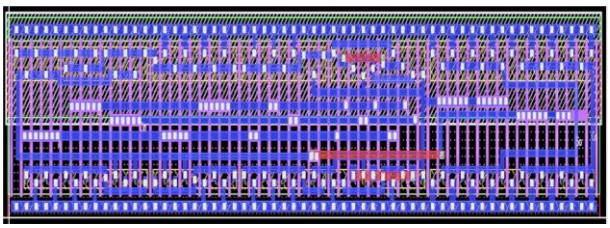

Figure 9: Layout of 1-bit full adder of mirror design style

Cascading the 1-bit full adder gives the ripple carry adder. Initial layout of 4-bit ripple carry adder was created too right before it was improved. During the initial layout, the top level consists of only four cells which is the 1-bit mirror full adder. The cells were cascaded vertically in order to share common power supply and ground since area compression is one of the factors that need to be considered when doing a layout. In addition to that, a guard ring was also implemented on the layout in order to block noise coupling that might otherwise interfere with the operation of low-power circuitry. M2 pins were also used for input and output signals in order to easily connect it to other cells or blocks (if any).

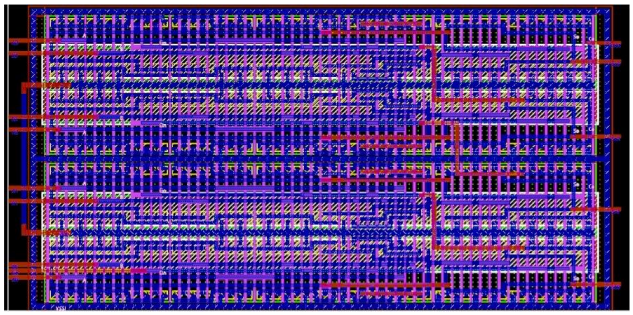

Figure 10: Layout of 4-bit ripple carry adder of mirror design style

The DRC verification process always has 2 results; either CLEAN or FAIL. If the layout created did not violate any rules given on the DRM (Design Rule Manual), then it will result to clean. On the other hand, if one of the layers on the layout was missing or wrong placing, it will then result to fail. Figure 11 shows the DRC status of the 4-bit ripple carry full adder after running the DRC verification[10].

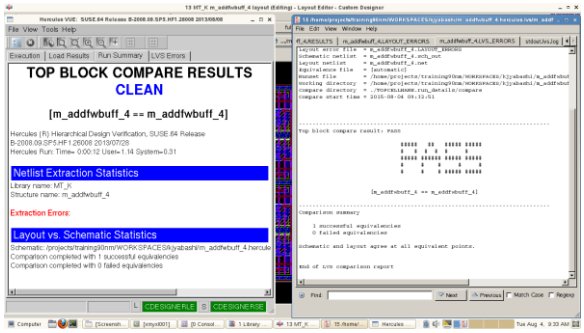

Figure 11: DRC status of 4-bit ripple carry adder

LVS is the class of EDA verification software that determines whether a particular integrated circuit layout corresponds to the original schematic diagram of the design. It recognizes the drawn shapes of the layout that represent the electrical components of the circuit, as well as the connections between them. Figure 12 shows the LVS status of the 4-bit ripple carry full adder after running the LVS verification.

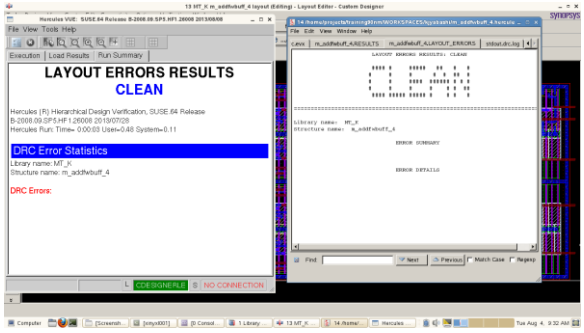

Figure 12: LVS status of 4-bit ripple carry adder

After assigning the source pins, the code was created based on the gate-level diagram and truth table for the full adder. A simple if-else statement was used in the code to easily detect where the output will be. Table 2 shows the actual output of the full adder after testing the code created.

Table 2
Actual output of the full adder

A	B	Cin	Sum	Carry out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

IV. CONCLUSION

In this paper, a 4-bit ripple carry full adder of mirror design style was proposed. Based on simulation results performed by HSPICE in Synopsys Generic 90nm CMOS process with 1.2V supply voltage, the minimum sizes for transistors cannot be implemented due to inappropriate functions of outputs causing the full adder to get bigger by adjusting the diffusion sizes both for PMOS and NMOS. Buffers in addition were also created for the outputs to be synchronized. The propagation time delay calculated on a TT corner with 0°C for So3 and C_{out} are 0.042us and 0.2505us respectively.

Laying out the mirror full adder is easier to layout compared to static CMOS full adder for the fact that NMOS and PMOS are completely symmetrical. This further lessens the metal congestions and improper routing, and Cin's are placed closest to the output. The 4-bit RCA has an area of 683.34 um^2, standard cell height of 16um, and composed of 14 cells.

DRC verification process takes time in order for a cell to clean. It requires familiarization of the DRM book to fully understand how the rules are implemented for each layer. On the other hand, in most cases, the layout will not pass LVS the first time it was verified. Typical errors encountered during LVS include short and open nets, component mismatches, missing components and parameter mismatch.

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