Analysis of Gate Poly Delayering in SOI Wafer

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***Abstract*—The advantages of silicon-on-insulator (SOI) technology are reduced parasitic device capacitance, improved performance as well as smaller build area. Despite the gains of SOI technology to manufacturers, new challenges arise in Physical Failure Analysis (PFA). The process of delayering polysilicon or active layer becomes impossible without harming the top silicon. This study discussed the challenges of the current fastest, reliable and reproducible method to delayer polysilicon and divulge active layer. Current delayering method using 49% Hydrofluoric (HF) concentration and SC1 solution is proven to be a faster way to reveal polysilicon layer for Bulk Commentary Metal-Oxide Semiconductor (Bulk CMOS). Thus, this method was tested on SOI Wafer to analyze the effect. The experiment was conducted by selecting small, thin and dense gate polysilicon such as in Static Random Access Memory (SRAM) cells. The result shows that high concentration of HF is not suitable for SOI since HF will etch Interlayer Dielectric (ILD) all the way down to Buried Oxide (BOX) and leave top silicon unattached. As a result, top silicon structure was peeled off or damaged. The result was not promising since the top silicon is crucial part as it holds information to discover physical cause of failure.**

***Index Terms*—SOI; Top Silicon; Physical Failure Analysis; Bulk CMOS.**

I. INTRODUCTION

The silicon-on-insulator (SOI) wafer increases chip functionality without the cost of major process equipment changes such as higher resolution lithography process tools. The advantages are faster circuit operation, reduced parasitic device capacitance, smaller devices build area and lower operating voltages [1]–[5]. The lower voltages, low power consumption and high performance for today requirements disclosed the limitations of Bulk Commentary Metal-Oxide Semiconductor (Bulk CMOS) [6].

In SOI wafers, transistors are formed on top of silicon layer which are isolated from the main body of the wafer by an insulator layer, usually silicon dioxide known as Buried Oxide (BOX). Underneath the BOX layer is a support surface wafer which called a 'handle' silicon wafer [5]. Since the SOI technology is differently structured as compared to Bulk CMOS, new challenges in Physical Failure Analysis (PFA) emerge [7]. For instance, challenges in layer de-processing technique or known as delayering method.

Delayering is a process of removing layer on a die to analyst visibility and access to Region of Interest (ROI) at below surface which cannot be accessed or seen. Visibility offers access to Defect of Interest (DOI) for chemical and physical characterization. On the other hand, delayering method also enables electrical accessibility to signal for failure site isolation. Due to increasing interconnect layers and shrinking feature sizes, delayering has become a complex process which requires high skill. Error in delayering can result in a loss of key information which is useful to discover physical cause of the failure.

Some common delayering methods in semiconductor are using dry or wet etching. In dry etching, plasmas or etchant gasses are used to remove material from wafer. This method utilizes high kinetic energy of particle beams, chemical reaction or combination of both to actively remove the material. In wet etching delayering, liquid chemical or etchant is used to etch away material from a wafer. Masks are employed on a wafer for a specific pattern etching. Material surfaces that are not protected by the masks will be etched away by dry or wet etching activity. The masks are deposited and patterned on the wafers in a previous fabrication step using lithography. Material etching activities will remove the material isotropically, anisotropically or both actions at the same time. Isotropic etching is uniform in all direction while anisotropic etching is uniform in vertical direction [8].

Another technology to delayer Integrated Circuit (IC) structures and other microelectronic devices is to use a Chemical and Mechanical Planarization (CMP). CMP uses liquid chemical and spinning pad to improve material removal rates. The CMP is the only process which can delayer and at the same time do planarization on a global scale [9]. Some hard material in a wafer-like tungsten (W) layer is efficiently removed by CMP delayering [10]. In Physical Failure Analysis (PFA), a similar delayering and planarization method is employed which known as parallel lapping.

This work focused on applying the best method in delayering Bulk CMOS into SOI wafer. In this paper, the delayering method and analysis result are discussed. The results of this experiment will hopefully give some brainstorming ideas on how to improve the delayering process for SOI Wafer.

II. METHODOLOGY

Gate poly delayering process in Bulk CMOS is shown in Figure 1. The method can be considered as the fastest way to remove all stacked layers of Intermetallic Dielectric (IMD). Commonly high concentration of Hydrofluoric (HF) acid

(49%) was used in this process. This really worked best when top metal line was exposed to the HF wet etching [11]. Before applying the high concentration of HF, the Reactive Ion Etching (RIE) was employed to remove the passivation layer such as Polyimide (PIQ). This front-end Bulk CMOS delayering technique worked for wide poly such as P-bulk capacitors.

Figure 1: The gate poly delayering process

In this research, the process in Figure 1 was applied to the SOI wafer. A small, thin and dense gate polysilicon such as in Static Random Access Memory (SRAM) cells were selected as the experiment sample. As shown in Figure 1, a full process of die sample was dipped in HF with concentration of 49% for 2 minutes to expose polysilicon. An optical microscope was employed to distinguish polysilicon layer. When polysilicon layer is exposed, it will look pinkish.

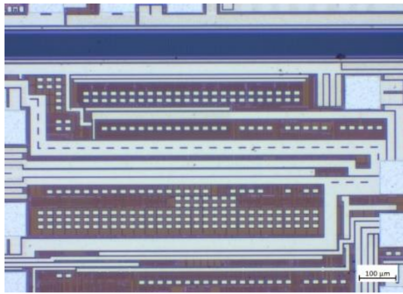
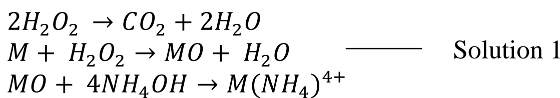


Figure 2: Optical image of full process die sample (Top metal line with passivation)

After that, the sample was immersed into SC1 solution (1NH4OH:1H2O2:5H2O) for 3 minutes at temperature of 50°C. The reason for using SC1 solution was to remove organic compound and metallic particle [11]. The samples were then cleaned with acetone as shown in Figure 2.The chemical reactions are shown in Solution 1:



$$2H_2O_2 \rightarrow CO_2 + 2H_2O$$
$$M + H_2O_2 \rightarrow MO + H_2O \quad \text{——— Solution 1}$$
$$MO + 4NH_4OH \rightarrow M(NH_4)^{4+}$$

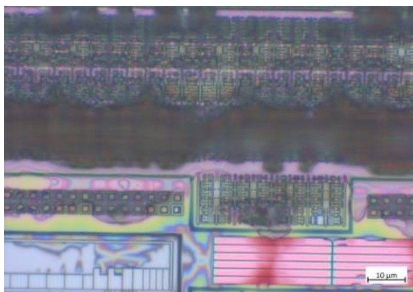
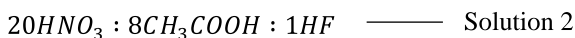


Figure 3: Optical image of gate poly (cell) after applied SC1 solution for 3 minutes and cleaned by acetone

Next, poly-etchant solution was employed to etch polysilicon layer [11] as shown in Figure 4. The polysilicon etch solution was derived by Solution 2.



$$20HNO_3 : 8CH_3COOH : 1HF \quad \text{——— Solution 2}$$

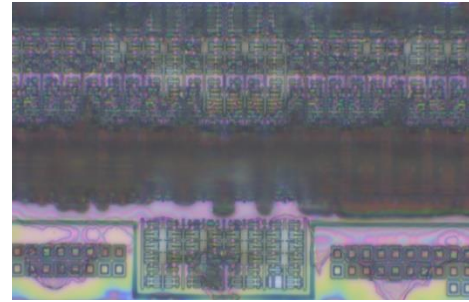


Figure 4: Optical image of gate poly (cell) poly-etchant solution

III. Result and Discussion

Optical inspection found uneven layer after dipping in 49% HF for 2 ~ 3 minutes and cleaning by acetone. Exposed polysilicon was observed in some areas and some was still covered by previous layer or etching's debris as shown in Figure 5. Although the SC1 solution and acetone cleaned clean the metallic and organic debris after HF etching, the remaining layers still persist.

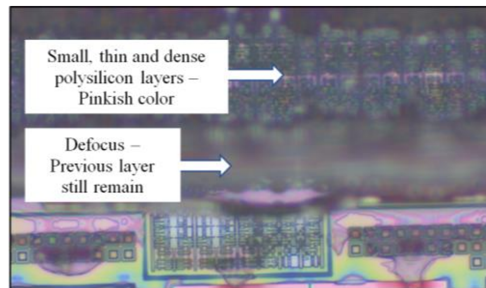


Figure 5: Optical image of gate poly (cell) after applying 49% HF for 2 minutes and cleaning with acetone.

The poly-etchant solution did not remove all the poly gates on the SRAM area. The surface was still uneven with previous layer stacking up. Poly-etchant chemical did not react with those regions which were still covered by oxide. Only exposed polysilicon will be etched away by poly-etchant Solution 2. The remnant materials were possibly metal, nitride and oxide as shown in Figure 6.

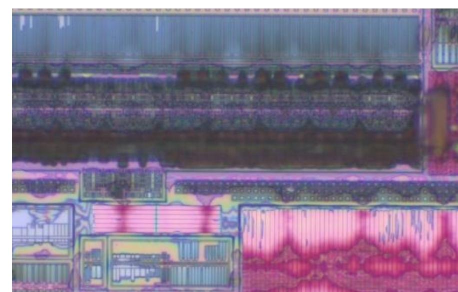
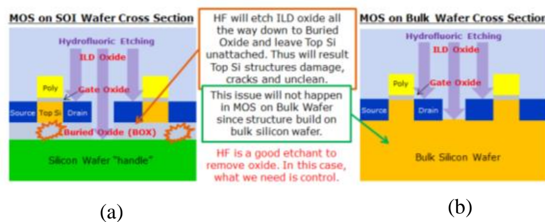


Figure 6 Poly-etchant solution to remove polysilicon

The existing of Buried Oxide (BOX) layer in between "handle wafer" and top silicon which linked with DTI oxide makes polysilicon removal more challenging. The chemical used in wet etching such as HF, which supposed to etch Gate Oxide (GOX), loosened the gate poly attachment on active surface and also etched the DTI trench oxide. In the worst scenario, etching can even go deeper into BOX layer which untie the Top Silicon attachment on BOX surface. Hence, the

peeled off top silicon plate during the cleaning will drive to a meaningless analysis.

The Bulk CMOS front-end delayering method (as shown in Figure 1) is only works for wide polysilicon such as capacitors but not dense gate poly. This method is also not suitable for SOI wafer. The 49% HF concentration easily etched away the BOX layer. Hence, the top silicon will peel off during cleaning. This method is only suitable for Bulk CMOS wafer where no concern of etching away BOX layer as shown in Figure 7.



(a) (b)

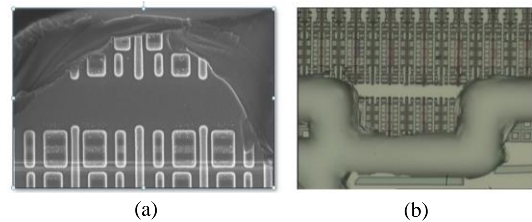
Figure 7: Challenges of delayering (a) SOI technology wafer compared to (b) Bulk CMOS wafer

By using HF etching method, the BOX layer was etched away and top silicon was peeled off. The damage can also be seen at the nearby survived top silicon where edge crack can be observed in Figure 8. The Front-End delayering method (Figure 1) resulted in the uneven layer etching. Some over-etched regions and some under-etched regions were observed. Those regions which are under-etched region will result in remaining polysilicon and oxides layer as shown in Figure 9.

IV. Conclusion and Future Work

In this paper, the assessment of Bulk CMOS Wafer Front-End delayering method into SOI Wafer is discussed. The result shows that high concentration HF is not suitable for SOI because HF etched Interlayer Dielectric (ILD) all the way down to BOX and left top silicon unattached. As a result, top silicon Structure was peeled off or damaged. This is not a problem for Bulk CMOS wafer. Furthermore, the HF isotropic wet etching created an uneven surface. Hence, it is difficult to maintain flatness which is the key for precise delayering.

For future work, there are two proposed techniques need to be explored to possibly open the door to precise delayering at front-end of SOI such as polysilicon and active layer. The first technique is to employ Chemical and Mechanical Polishing (CMP) technique or known as parallel lapping to improve surface uniformity. The second technique is to find an effective spot between HF concentrations and etching rate. The ideal combination of HF concentration and etch time is believed can remove oxides efficiently, detaching the gate poly while preserves the top silicon.



(a) (b)

Figure 8 (a) Scanning electron microscope (SEM) image and (b) Optical image of top silicon edge cracks due to over-etched DTI trench

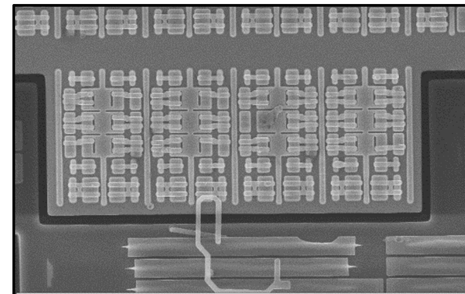


Figure 9 Polysilicon and oxides still remained on top of silicon surface due to HF under-etch

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