Design of CMOS Schmitt Triggers Circuit for Low Application Device

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***Abstract*—Schmitt triggers are electronic comparators circuit which are generally used to help improve the circuit immunity towards noise and disturbance. They had become significant components of various emerging applications. However, they are still facing a problem in term the noise problem in the output signal of the Schmitt Trigger which is do not able to operate at low voltage. In this research a Schmitt Trigger is design to function at low voltage. This design is realized based on 0.18µm CMOS technology by using Cadence simulation software. A few voltage values have been tested in this circuit and the optimized voltage for this project is 0.8 V to 1.5 V. Therefore this circuit design is applicable for various low voltage analogue or digital applications.**

***Index Terms*—Inverting; Hysteresis; Non-inverting; Schmitt Trigger.**

I. INTRODUCTION

Schmitt Trigger is a circuit that used in the microprocessor in electronics device such as computer, mobile phone and all other electronics devices that have a microprocessor. The main function of Schmitt Trigger inside a microprocessor is to reduce the noise signal, so that the device can perform faster in processing data [1]. It is a comparator circuit that has a hysteresis which is realized by giving positive feedback bias to the non-inverting input of a comparator or differential amplifier. A Schmitt Trigger is an active device that are able to turn an analogue input signal into a digital output signal.

Nowadays, there are many types of Schmitt Trigger invented in electronic industry, however, they are still facing problems in term the noise problem in the output signal of the Schmitt Trigger, having large static power and high dynamic power dissipation, operate at high voltage which is do not able to operate at low voltage and this will cause in the use of high power consumption and also having low speed in data processing. Hence the idea comes out in implementing the new design circuit of Schmitt Trigger to overcome these problems.

In this research a Schmitt Trigger is designed to function at low voltage. The low voltage is optimized for 0.8V to 1.5V. Furthermore, to verify the performance of the constructed circuit, in term of functionality and also to reduce noise of the Schmitt Trigger circuit. The simulation result must be in square form for both input voltage and output voltage. Hence, design a layout circuit in 2D graphic which is the final design for circuit to be implemented.

This design is based on 0.18µm CMOS technology using Cadence simulation software. The design circuit will then be simulated in the Cadence simulator application.

II. METHODOLOGY

Figure 1 shows the proposed design circuit for this project [3]. This design circuit is based on 0.18µm CMOS technology.

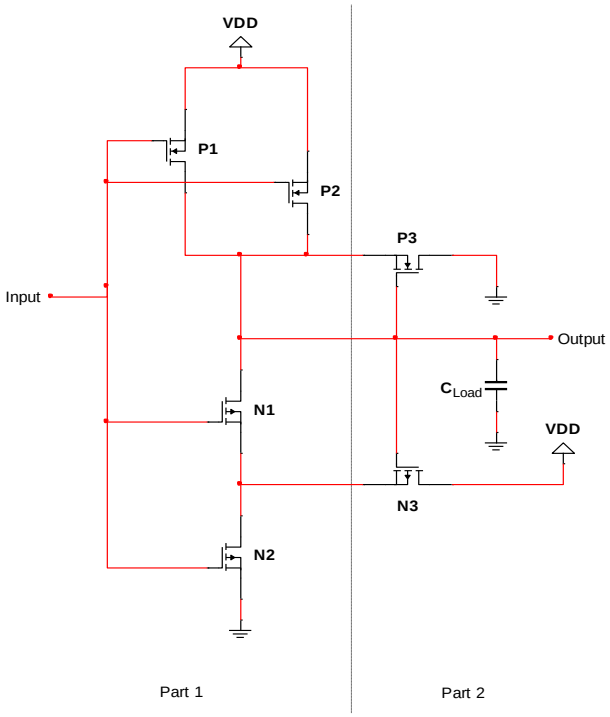

Figure 1: The proposed schmitt trigger circuit

This design has been selected because this circuit will not have static power consumption. It is due to no connection path directly in between of the source voltage and the ground [2]. In order to implement this feature, P sub-circuit has a path connection between output and source voltage path, at the same time the N sub-circuit has a path connection between the ground and output path [2,3]. Then, the result and simulation will be done using Cadence simulation software. This CMOS Schmitt Trigger was confirmed to be able to operate at low voltage of 0.8 V to 1.5 V.

Figure 1 shows the proposed design of Schmitt Trigger which can be divided into two parts which are Part 1 and Part

2 [2]. The proposed design is similar to the conventional circuit Schmitt Trigger, where it combines two sub-circuit, which are P sub-circuit (containing of P3, P2 and P1 PMOS device) and N sub-circuit (containing of N3, N2 and N1 NMOS devices) [4]. In this proposed design the P sub-circuit has a path connection between the output and the source voltage, at the same time the N sub-circuit has a path connection between the ground and output path [5]. Accordingly there will be no direct path between source voltage and ground giving no static power consumption [6, 7].

Part 1 circuit has NAND gates which are designed based on the De Morgan Theorem. Part 1 is formed by P1 and P2 PMOS devices which have parallel connection, while N1 and N2 NMOS devices have series connection. By having this design of PMOS connected in parallel the P sub-circuit resistance is expected to be reduced by halves [8]. It is rather to lower the PMOS noise because noise is more intensive in PMOS as it has high mobility in the PMOS in contrast to the NMOS.

Part 2 circuit has P3 PMOS device and N3 NMOS device. Both MOSFET are connected directly through each gate terminal. As for the output of each case, the P3 will operate as a pull up, in the same time the N3 will operate as a pull down. The size of the transistors can be determined by finding each sub-circuit minimum component path. Furthermore, the size of each transistors are estimated according to their distribution [9]. As for the transistors which are connected in parallel, the scales are by the factor of 1. Whereas the transistors which are in series connection, have a scale by the factor of 2 [10].

$$\left(\frac{W}{L_{eff}}\right)PMOS = r\left(\frac{W}{L_{eff}}\right)NMOS \quad (1)$$

where:

W : Width
Leff : Effective length
R : Ratio

The PMOS and NMOS ratio are set by deriving from equation 1, with the *Leff* (effective length) in considering of 0.18µm CMOS technologies, gives *Leff* = 0.18 µm. It is suggested to extend the PMOS device to permit the resistance that is in line with NMOS device pull down. Table 1 shows the dimensions of respective transistors.

Table 1
The Dimension of Transistors

NMOS	$\frac{W}{L_{eff}}$	PMOS	$\frac{W}{L_{eff}}$
N1	$\frac{0.35}{0.18}$	P1	$\frac{0.55}{0.18}$
N2	$\frac{0.35}{0.18}$	P2	$\frac{0.55}{0.18}$
N3	$\frac{0.22}{0.18}$	P3	$\frac{0.55}{0.18}$

The ratio is set to be three maximize the noise margin and to create a circuit with symmetrical voltage-transfer characteristic (VTC), [11]. Through expanding the PMOS width, it shift the switching threshold voltage further. This will produce the width of hysteresis becomes more rectangles which are preferable in designing a Schmitt Trigger circuit.

On occasion of low input signal, the P sub-circuit alone will be treated and this will make the output signal increases until match the VDD [12]. At this situation both PMOS of P2 and P1 are turned on, while P3 are turned off. Accordingly the output voltage will be pulled to the VDD. Then after it has increased to VDD, both N2 and N1 are switch on while the other is switch off. As a result, the output voltage will be pulled down to the GND. The schematic circuit design is then drawn accordingly in simulation software.

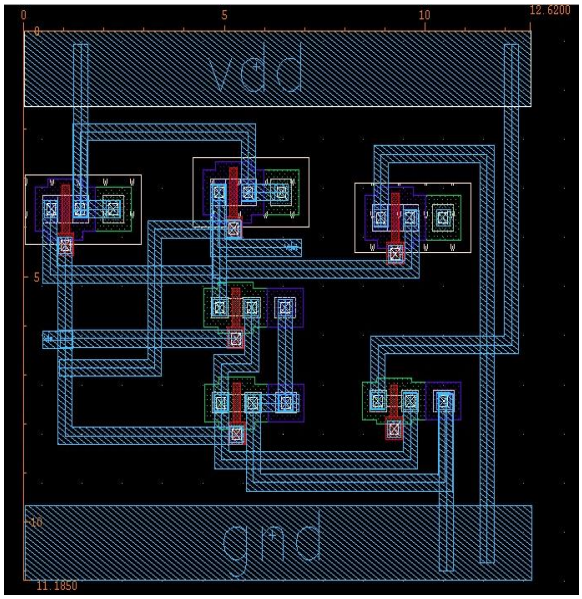

Figure 2: Layout circuit

The layout of the circuit at Figure 2 is the drawn result in Cadence simulation software. This layout is the result of exploiting the distribution of transistors based on the proposed circuit in Figure 1 and the transistors ratio of the width-length followed the dimension in Table 1. The voltage source Vdd is placed at the top and ground GND is placed at the bottom of the layout. Then a few voltage values have been tested in this layout circuit. The optimized value of voltage for this layout was 0.8 V to 1.5 V.

III. Result and Discussion

This proposed design results are compared with another design that have a variation in width-length ratio of PMOS and NMOS. For comparison here, the 1st design is our propose design circuit and the 2nd design [2] is the compared design. The 2nd design is a low voltage Schmitt trigger circuit of 0.18µm but differ in width-length ratio from the 1st design (proposed design). The construction of the circuit is almost the same. The result of this 2nd design is simulated by using Mentor Graphic simulation software [2]. The specification data for both design is tabulated as in Table 2. The difference between these circuits is that they have a different in width length ratio of PMOS and NMOS component.

Table 2
The Specification Data of Compared Design

$\frac{W}{L_{eff}}$	1st design (µm)	2nd design (µm)
P1	$\frac{0.55}{0.18}$	$\frac{0.54}{0.18}$
P2	$\frac{0.55}{0.18}$	$\frac{0.54}{0.18}$
P3	$\frac{0.55}{0.18}$	$\frac{0.54}{0.18}$
N1	$\frac{0.35}{0.18}$	$\frac{0.22}{0.18}$
N2	$\frac{0.35}{0.18}$	$\frac{0.22}{0.18}$
N3	$\frac{0.22}{0.18}$	$\frac{0.18}{0.18}$

The simulation results of 2nd design was compared with the 1st design (proposed design). Figures below are the results of both design. The input signal for 1st design (proposed design) is at the bottom while output signal is at the top. In contrast, the input signal for the 2nd design is at the top, while the output signal is at the bottom. Figures below show the simulation results operation of 0.8 V, 1.0 V, 1.2 V and 1.5 V respectively.

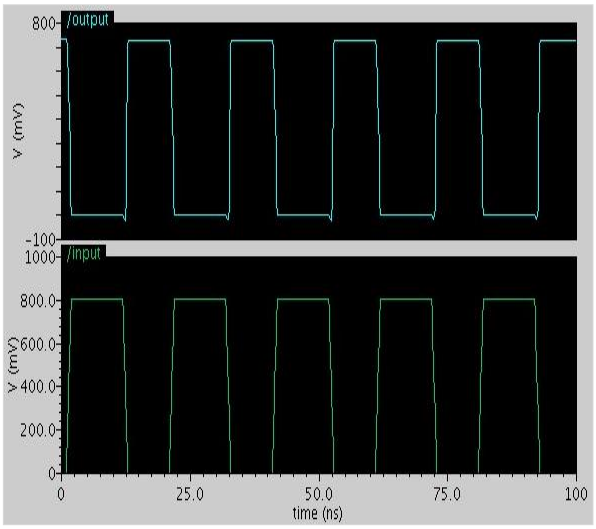

Figure 3: Simulation of 0.8 V for 1st design (proposed design)

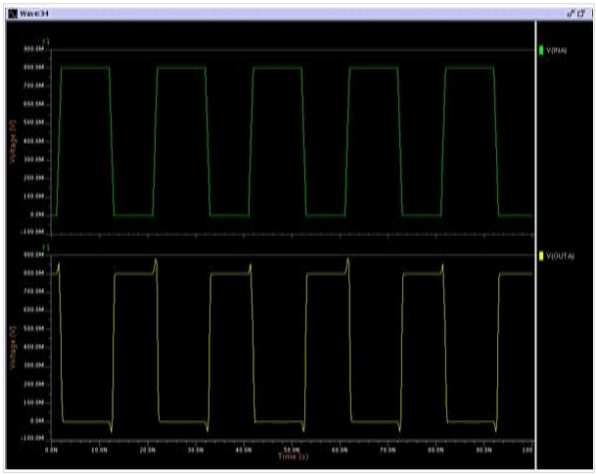

Figure 4: Simulation of 0.8 V for 2nd design [2]

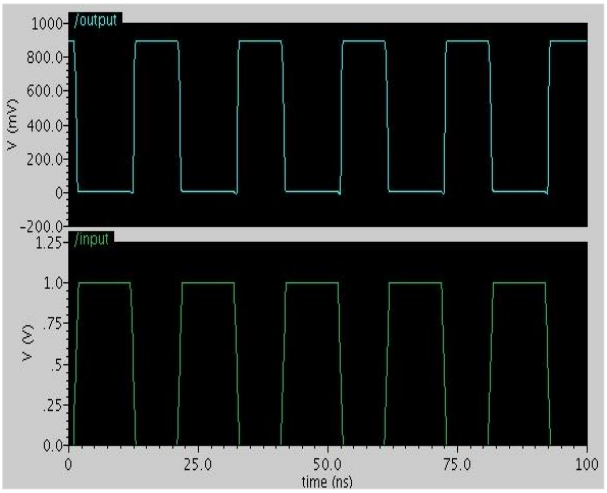

Figure 5: Simulation of 1.0 V for 1st design (proposed design)

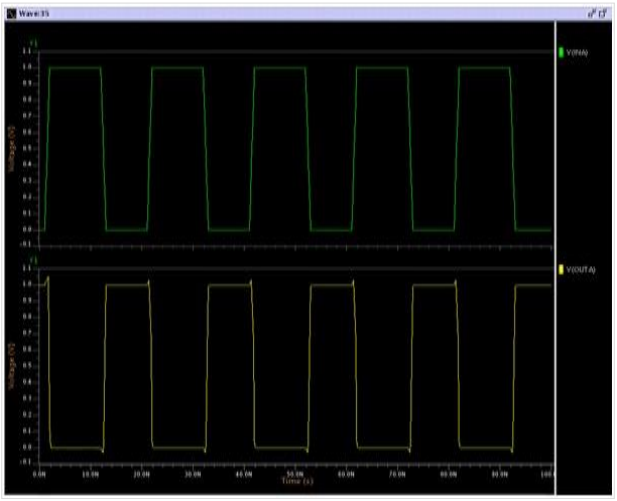

Figure 6: Simulation of 1.0 V for 2nd design [2]

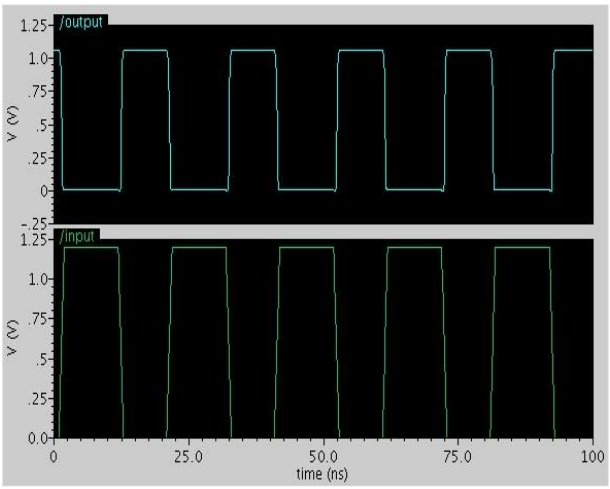

Figure 7: Simulation of 1.2 V for 1st design (proposed design)

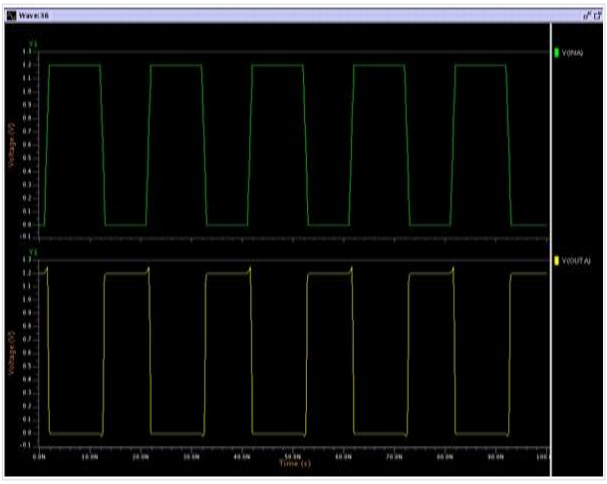

Figure 8: Simulation of 1.2 V for 2nd design [2]

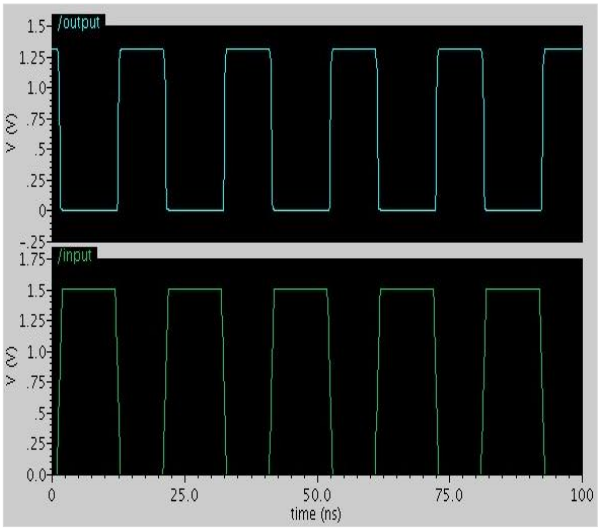

Figure 9: Simulation of 1.5 V for 1st design (propose design)

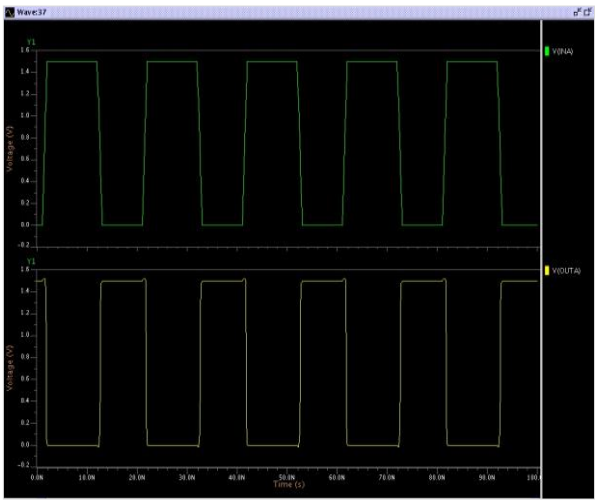

Figure 10: Simulation of 1.5 V for 2nd design

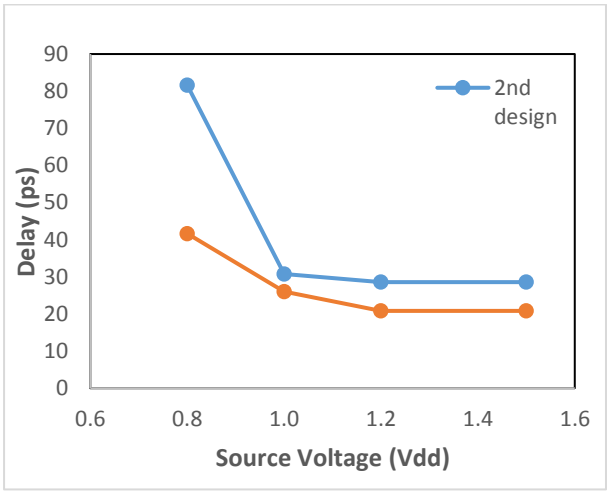

Figure 11: Propagation delay

In order to analyze the performance of the 1st design (proposed design), the speed of the CMOS Schmitt Trigger is analyzed by estimating the propagation delay of an output signal from input signal. Figure 11 shows the comparison of the propagation delay for both 1st design (proposed design) and 2nd design. From this result, we understand that the 1st design (proposed design) has better response. Thus, it shows that the 1st design (proposed design) has better performance compared to the 2nd design for low application. Since the width-length ratio of the 1st design (proposed design) is smaller compared to the 2nd design, it shows that the smaller the width-length ratio can give better performance to the circuit.

IV. CONCLUSIONS

Schmitt triggers are electronic comparators circuit which are generally used to help improve the circuit immunity towards noise and disturbance. They had become significant components of various emerging applications. For this project, the Schmitt trigger circuit was designed and constructed for low voltage application. The proposed design of the Schmitt trigger was successfully constructed by using the Cadence software application. The simulation results showed that this proposed design was able to run at a low voltage which is 0.8 V. The performance of the circuit was determined in term of speed of data processing by finding the propagation delay. Compared to the other design of Schmitt Trigger, this design gave a better response for low voltage application. Therefore, this circuit design is applicable in numerous low voltage analogue as well as digital applications.

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