

# An FPGA Approach for EXP-BET Metrics Computation Using Simulink Blockset

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**Abstract**—This paper proposes the process of simulating the mathematical model of the EXP-BET scheduling algorithm using MATLAB Simulink configured with Xilinx System Generator (XSG). The system generator provides Simulink blockset for several hardware operations that could be implemented on various Xilinx FPGAs. The method describes in this paper involves the calculation of metrics equation for EXP-BET scheduling algorithm and the model is developed using constant values for all the parameters in the equations. Many applications that are DSP based require mathematical modeling for easy understanding and analysis. Furthermore, the need of instant prototyping tools such as MATLAB Simulink and Xilinx System Generator has become increasingly important because of the limitation for time-to-market. This can greatly reduce the process cycle from the algorithm to the hardware implementation. The output of the simulation demonstrated that the EXP-BET metrics computation was successfully accomplished.

**Index Terms**—EXP-BET Scheduling Algorithm; MATLAB Simulink; System Generator.

## I. INTRODUCTION

Matrix Laboratory namely as MATLAB is a numerical computing environment and modern (fourth generation) programming language developed by Math Works. MATLAB integrates computation, visualization, and programming environment that allow matrix manipulations, plotting of functions and data, implementation of algorithms, creation of graphic user interface (GUI) and interfacing with programs [1]. Simulink is an additional package in MATLAB provide platform for Model-Based design besides a good tool to test signals and visualize outputs during simulation.

Model-Based Design is a process that enables faster, more cost-effective development of dynamic systems, including control systems, signal processing and communications systems [2]. The method of Model-Based Design is significantly different from the procedure in the traditional design. The designers can formulate advanced functional characteristics by using continuous-time and discrete-time computational building blocks rather than using complex structures and extensive software code [2].

This paper presents the simulation of the Exponential Blind Equal Throughput (EXP-BET) scheduling algorithm's metrics equation using MATLAB Simulink configured with Xilinx System Generator (XSG). Scheduling mechanism is the process of dynamically allocating radio resources to User Equipment (UE) that transmits different flows at the same

time. The significance of radio resource management algorithms are to elevate the performance of the end user and system capacity in Long Term Evolution Standard (LTE) Network.

Since the implementation of scheduling algorithm is not standardized in LTE, thus the network vendors can design and tune the algorithms according to the needs [3]. Previously, various scheduling algorithm which offered several techniques in handling resources to the users have been developed such as Modified Largest Weight Delay First (MLWDF), Proportional Fairness (PF), and Maximum Rate [4].

In 2016, K. S. Syahidah et al. [5] published a paper which described the performance of the EXP-BET scheduling algorithm towards the Frame Level Scheduler (FLS) [6] and Exponential Proportional Fairness (EXP-PF). The authors summarized that the EXP-BET outperformed the EXP-PF and FLS algorithms for the real time services such as video gaming and video streaming and the non-real time service which includes web browsing and email. EXP-BET has shown 17.72% improvement than FLS and 7.52% for EXP-PF in terms of fairness index.

To the best of our knowledge, none of the researchers have implemented the EXP-BET algorithm for the FPGA implementation using MATLAB Simulink. In a different study conducted by Liyana et al. [7], they have primarily concentrated on the implementation of FPGA for various algorithms used in arbiters. At present, FPGAs have large resources of Look up tables (LUTs) logic gates and RAM blocks to support any complex digital computations. FPGA is called as the field programmable gate array because the FPGA board itself can be configured or programmed by the user. The programming language of the FPGA is coded using Hardware Description Language (HDL) such as Verilog HDL and VHDL.

The researchers in paper [8] proposed a methodology for simulation process of a complex mathematical model. The authors simulated the mathematical model of Differential Phase Shift Keying (DPSK) and Fast Fourier Transform (FFT) using Xilinx System Generator and MATLAB Simulink environments. Due to the complexity of the mathematical algorithm, the authors concluded that the mathematical modeling for DPSK and FFT cannot be simulated using pure HDL code besides; it is costly and time consuming.

Another studies by Mohamed Ali Hajjaji [9] proposed a real time implementation system of numerical watermarking



by the  $i^{\text{th}}$  user

$$\text{Average } D_{HoL} : \frac{1}{N_{RT}} \sum_{i=1}^{N_{RT}} D_{HoL}$$

$N_{RT}$  : Number of active downlink real time flows

$\Gamma_k^i$  : Spectral efficiency for  $i^{\text{th}}$  user over  $k^{\text{th}}$  resource block

### B. Blind Equal Throughput

Accordingly, the BET algorithm [11] provides throughput fairness among all active users irrespective of the user location. The user will be allocated based on the metrics formula:

$$m_{i,k}^{BET} = \frac{1}{R_i(t)} \quad (2)$$

where:

$R_i(t)$  :  $\beta R_i(t-1) + (1-\beta)r_i(t)$

$B$  : Weight factor

$R_i(t-1)$  : Past average throughput of the user at time  $t-1$

$r_i(t)$  : Achievable data rate for user  $i^{\text{th}}$  at time  $t^{\text{th}}$

### III. EXP-BET MODELING

In the Simulink environment, the FPGA frontier is defined in the Gateway In and Gateway Out blocks. The input and output from the FPGA is fed into the Gateway In and the output is produced from the Gateway Out port. In the Gateway In block, the Simulink floating point input is converted to a fixed point format, saturation and rounding modes. The model of the system generator is as illustrated in Figure 3. These ports interface the Simulink double data type and the FPGA fixed point environments.

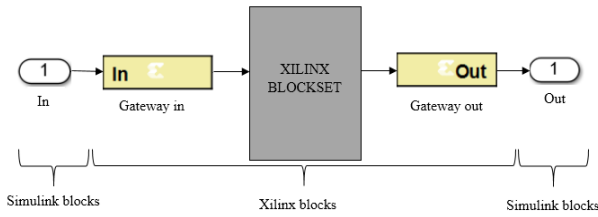


Figure 3: The model of the system generator used in the Simulink

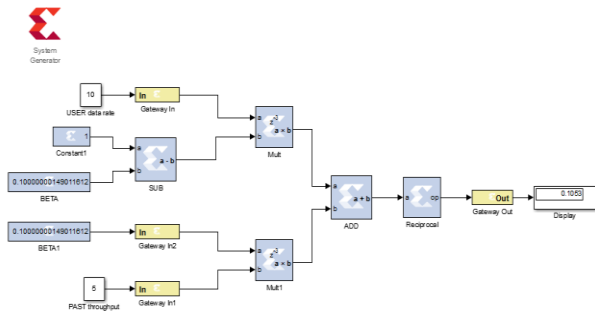


Figure 4: The Simulink model for the BET metrics equation

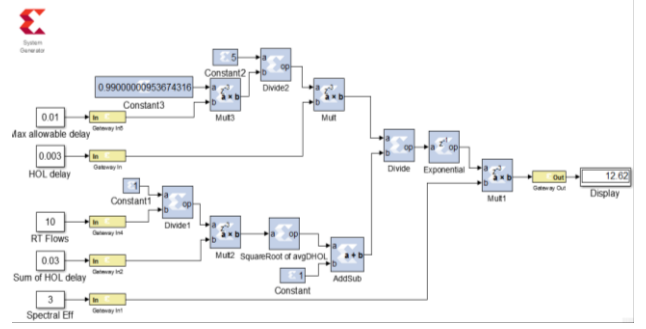


Figure 5: The Simulink model for EXP Rule metrics equation

The metrics equation for EXP and BET using Xilinx Blockset is created using Simulink Blockset. The system is tested by deploying a constant input to the system and the result is displayed on a Simulink's display block. The library used in Simulink environment for both mathematical equation are from the library of Sink, Sources and Xilinx Blockset.

### IV. RESULT AND DISCUSSION

The Simulink is used to verify the functionality of the model after the system is modelled. The testing process for the system is done by giving a constant input to the system so that the output will display a single value. System generator starts to process each block in the model and generate a simulation model according to the specific configuration of each block as depicted in Figures 4 and 5.

Table 1  
EXP-BET Parameter Values

Algorithms	Parameter	Value
Exponential Rule	maximum allowable delay	0.01
	head of line delay	0.003
	sum of Head of line delay	0.03
	Real-time flows	10
	spectral efficiency	3
Blind Equal Throughput	beta	0.1
	User throughput	10
	Past average throughput	5

Table 1 presents the values used for Equations (1) and (2) during the simulation process. Hence, by referring to equation 1 and 2, the expected output of the EXP Rule system should be 12.62 whereas the output of the BET calculation should be 0.1053 respectively. The system for BET is quite simple since it only involves basic mathematical operations such as addition, subtraction, multiplication and division operations. The system can be verified by inspecting the output of the model as can be seen in Figures 4 and 5 generated by System Generator and Simulink.

### V. CONCLUSION

MATLAB Simulink is the platform that provides simple and easy to use tool for developing mathematical computing based algorithm. In terms of hardware implementation to FPGA, the configuration of System Generator with MATLAB Simulink is more suitable and beneficial option compared translated the algorithms using VHDL or Verilog HDL. The EXP-BET is an algorithm which consists of the Exponential Rule (EXP Rule) and Blind Equal Throughput (BET). The work presented was designed and simulated using

the Xilinx System Generator and MATLAB Simulink environment. This resulted in a mathematical modeling of the EXP-BET metric equation using System Generator blocks, simulation and modification of these blocks.

Thus, future research should concentrate on the hardware verification for EXP-BET algorithm into FPGA platform by following the Xilinx System Generator design methodology named hardware co-simulation method.

#### ACKNOWLEDGMENT

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