A Low Voltage Recycling Folded Cascode OTA based on novel CMRR Magnifier

Mohammadreza Farsi, Dr. Khalil Monfaredi
Engineering Faculty, Department of Electrical and Electronic Engineering, Azarbaijan Shahid Madani University, Tabriz, Iran
khmonfaredi@azaruniv.ac.ir

***Abstract*—In this paper, a new recycling folded Cascode Operational Trans-conductance Amplifier (OTA) based on a novel Common Mode Rejection Ratio (CMRR) magnifier block is presented. Further, the principle of its operation is discussed in comparison with the conventional recycling folded Cascode OTA. The supply voltage is decreased in the proposed CMRR Magnifier based Recycling Folded Cascode (CMRFC) OTA, due to the elimination of the Cascode transistors. The common mode current is significantly removed by the CMRR magnifier block, which subsequently yields to a relatively higher CMRR compared with its conventional version. The DC bias voltage of the Cascode stage is also eliminated, incorporating the self Cascode structure. To provide a fair comparison, the CMRFC OTA is simulated along with its conventional version, namely the Double Recycling Folded Cascode (DRFC) OTA structure, at Cadence environment by considering the 180nm CMOS technology. The simulation results for the proposed OTA yield 53.4 dB DC-gain, 80.32 degree phase margin and 86.87 dB CMRR with 1.5 volt supply voltage, making it a suitable choice for low-voltage applications.**

***Index Terms*— CMRFC OTA; CMRR Enhancement; CMRR Magnifier Block; Recycling Folded Cascode.**

I. INTRODUCTION

The recent advances in CMOS technology have essentially promoted the mixed mode empowered portable electronic equipment market [1]. Although realizing an efficient mixed mode system requires successful implementation of complex analog and digital blocks simultaneously on a single chip, minimizing the power consumption is the main criteria for an optimum design [2, 3]. This highlights the importance of OTAs in the integrated circuits.

Operational trans-conductance amplifier (OTA) is a basic and fundamental building block which is used in many analog circuits such as analog-to-digital converters, switched capacitor filters, medical circuits and control systems [4]. In recent years, great efforts have been made to improve the performance of the OTA amplifiers in response to the high DC-gain and high unity gain bandwidth (GBW) requirement of the modern analog circuits and systems. In general, achieving higher operational speed along with lower power consumption in OTA amplifiers is difficult and requires novel design techniques. On the other hand, with the advances in sub-micron technologies, the intrinsic transistor gain factor, $g_m r_{ds}$, decreases, which further limits the DC-gain of amplifiers [5]. Recently, folded Cascode (FC) configuration has gained preference over the telescopic owing to the low voltage nature of present and future CMOS technologies, despite the higher power budget [6-8]. Another reason for this is due to the achievable high gain and the reasonably large output signal swing in single-stage and multi-stage FC structures (on the first stage).

Unfortunately, the bias current amplitude has no role on Folded Cascode amplifiers DC-gain. To solve this problem, Recycling Folded Cascode (RFC) structures have been proposed. The proposed RFC structures make it possible to use bias currents in a current recycling scheme to increase the overall DC-gain [9]. Thus, the RFC amplifier is a better design alternative in comparison to FC amplifier due to their bigger DC gain and trans-conductance [10,11]. By performing relative isolation of the AC path from DC path,

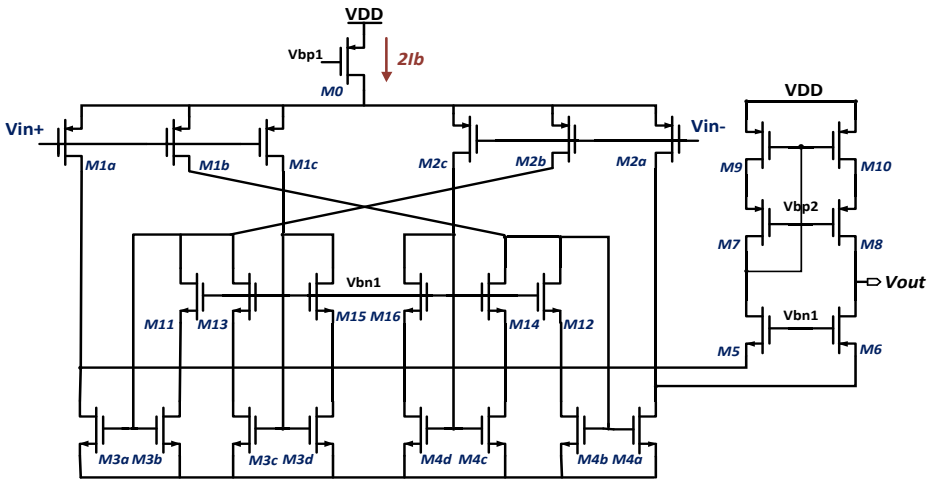


Figure 1: Conventional DRFC OTA

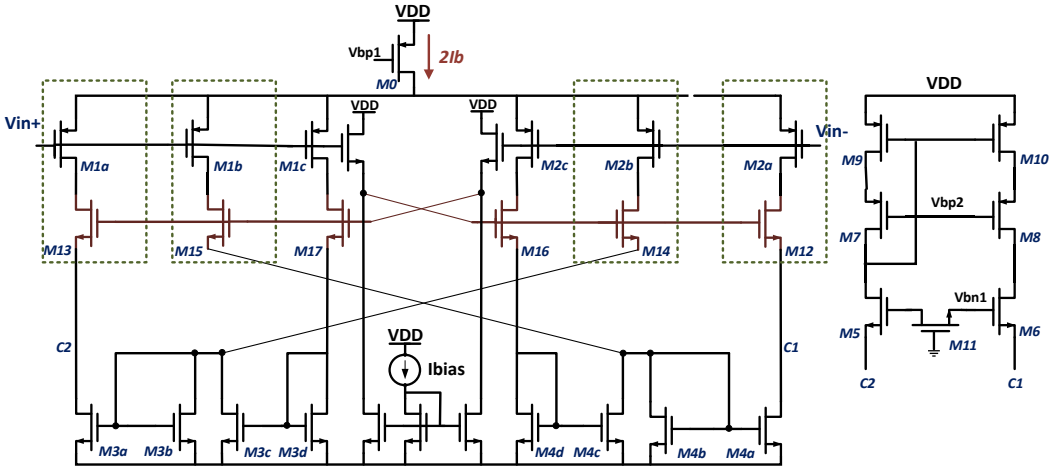


Figure 2: Proposed CMRFC OTA

the RFC structure presented in [12] provides a significant improvement in gain and bandwidth in comparison to the conventional FC structure.

In this structure, the trivial isolation of the AC and DC current paths limits the trans-conductance coefficient of the RFC structure. In [13], the improved RFC structure (IRFC) achieved 230% trans-conductance improvement versus the conventional RFC without increasing the occupied area with no additional DC current. This is mainly due to its capability to obtain a full isolation of AC and DC current paths. The double-recycling folded Cascode (DRFC) structure is presented in [14] and shown in Figure 1. In this structure, transistors M_{15}, M_{16}, M_{3d} and M_{4d} have been added to the IRFC structure in order to reuse the shunt bias currents to achieve better and more acceptable performance. In other words, this allows the circuit to achieve much higher output impedance and trans-conductance resulting in further improvement of the amplifier's DC-gain and bandwidth.

In this paper, a novel RFC structure called CMRFC, based on a proposed CMRR Magnifier block is presented. The performance of this RFC structure is based on the removal of common mode current by NMOS Cascode transistors used in the input stage. In comparison to the conventional DRFC, a larger phase margin is achieved for the proposed CMRFC circuit by incorporating the bandwidth enhancement technique provided in [15] and adding a large resistance between the current mirror transistors gates to separate the parasitic capacitors of NMOS transistors. This article includes the following sections: Section 2 discusses the proposed CMRFC circuit. Simulation results are presented in Section 3 and finally, the conclusion of the paper is presented in Section 4.

II. CMRFC Principle of Operation

In the conventional DRFC, differential input pair and shunt current sources are respectively replaced by triplet transistors and current mirrors M_{3c}, M_{3d} and M_{4c}, M_{d4}. Although reusing the shunt bias currents in this structure can further improve the DC-gain and gain-bandwidth (GBW), this would result in the phase margin being deteriorated.

The proposed CMRFC amplifier is shown at Figure 2. In this structure, utilizing the CMRR Magnifier block, which consist of transistors M_{12}-M_{17}, together with input transistors $(M_1\text{-}M_2)_{a,b,c}$ configured in a cross-connected scheme results in the common mode currents being deleted in the very input stage.

The common mode signals applied to the gates of the input MOS transistor $(M_1\text{-}M_2)_{a,b,c}$, which generate a common mode signal at the OTA output, which is also the opposite reaction of stacked transistors of M_{12}-M_{17} opposes the initially encouraged common mode signal that yields to a very high

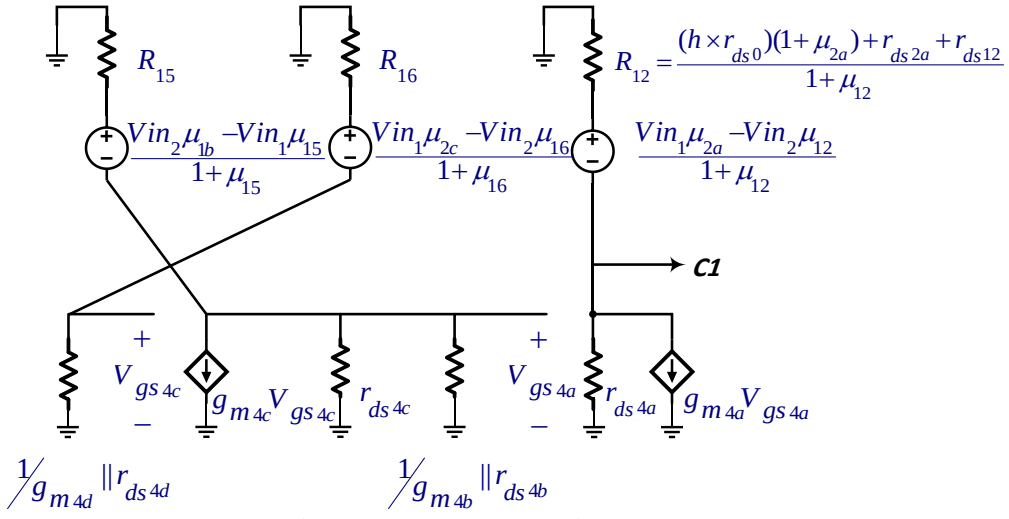


Figure 3: Half circuit small signal equivalent for CMRFC OTA input stage

CMRR specification.

Even though using NMOS transistors for input stage can increase the DC-gain [16], the proposed circuit input stage that consists of PMOS input pairs provides PMOS transistors with lower flicker noise, input with common mode voltage, and larger non-dominant pole [17]. In the conventional RFC structures, Cascode current mirrors are used to increase the accuracy of signal transmitted by current mirror, while improving the CMRR at the cost of higher supply voltage. Due to the significant role of the CMRR Magnifier blocks (shown in Figure 2 with dashed rectangle) that function to eliminate the common mode signals, simple current mirrors are used at the proposed CMRFC structure to reduce the required supply voltage. The lower supply voltage in the proposed circuit makes it suitable for low voltage applications. It should be noted that DC bias voltage of CMRFC circuit is eliminated due to the use of self Cascode stages.

The small-signal equivalent circuit, as shown in Figure 3 and 4 are used for CMRFC OTA ac analysis.

Considering the small signal equivalent circuit represented in Figure 3 for CMRFC OTA input stage, it is clear that an adequately large input stage, which is equivalent to resistance at node C_1 will result in the current being delivered to the output stage with a minor error. From Figure 3, we have:

$$I_x = g_{m4a}V_{gs4a} + \frac{Vin_1\mu_{2a} - Vin_2\mu_{12}}{(h \times r_{ds0})(1+\mu_{2a}) + r_{ds2a} + r_{ds12}} \quad (1)$$

and

$$V_{gs4a} = [\frac{1}{g_{m4b}} \parallel r_{ds4b} \parallel r_{ds4c} \parallel R_{15}](g_{m4c}V_{gs4c} + \frac{Vin_2\mu_{1b} - Vin_1\mu_{15}}{(h \times r_{ds0})(1+\mu_{1b}) + r_{ds1b} + r_{ds15}}) \quad (2)$$

$$V_{gs4c} = [\frac{1}{g_{m4d}} \parallel r_{ds4d} \parallel R_{16}](\frac{Vin_1\mu_{2c} - Vin_2\mu_{16}}{(h \times r_{ds0})(1+\mu_{2c}) + r_{ds2c} + r_{ds16}}) \quad (3)$$

where R_{15} and R_{16} are equal to

$$R_{15} = \frac{(h \times r_{ds0})(1+\mu_{1b}) + r_{ds1b} + r_{ds15}}{1+\mu_{15}} \quad (4)$$

$$R_{16} = \frac{(h \times r_{ds0})(1+\mu_{2c}) + r_{ds2c} + r_{ds16}}{1+\mu_{16}} \quad (5)$$

$1/gm$ is very small and dominates in Equations (2) and (3). Meanwhile, considering the opposite signs of Vin+ and Vin- in Equation (1) with these equations it is clear that they will be cancelled out for the common mode signals, while amplifying differential mode signals. The parameter 'h' is considered to generalize the derived equations to both common mode and differential mode signals for which 'h' is one and zero, respectively.

$$\begin{cases} h = 0 \quad for\ A_d \\ h = 1 \quad for\ A_c \end{cases} \quad (6)$$

Further simplifying I_x considering the differential and common mode signals, we have:

$$I_x = Vin_1(F) - Vin_2(G) \quad (7)$$

where

$$F = [\frac{g_{m4a}}{g_{m4b}}(\frac{g_{m4c}\mu_{2c}}{g_{m4d}(h \times r_{ds0})(1+\mu_{2c}) + (r_{ds0}(1+\mu_{2c}) + r_{ds2c} + r_{ds16}} - \frac{\mu_{15}}{r_{ds0}(1+\mu_{1b}) + r_{ds1b} + r_{ds15}}) + \frac{\mu_{2a}}{r_{ds0}(1+\mu_{2a}) + r_{ds12} + r_{ds2a}}] \quad (8)$$

$$G = [\frac{g_{m4a}}{g_{m4b}}(\frac{g_{m4c}\mu_{16}}{gm_{4d}(h \times r_{ds0})(1+\mu_{2c}) + r_{ds2c} + r_{ds16}} - \frac{\mu_{1b}}{r_{ds0}(1+\mu_{1b}) + r_{ds1b} + r_{ds15}}) + \frac{\mu_{12}}{r_{ds0}(1+\mu_{2a}) + r_{ds12} + r_{ds2a}}] \quad (9)$$

Considering Equations (8) and (9), it can be seen that if 'F' is adjusted to be equal to 'G', I_x will be zero for common mode signals yielding infinite CMRR and at the same time, it will provide a double boost for differential mode signals. This condition will be satisfied, if we have:

$$\begin{cases} \mu_{16} = \mu_{2c} \\ \mu_{15} = \mu_{1b} \\ \mu_{12} = \mu_{2a} \end{cases} \quad (10)$$

The same steps can be taken to analyze the other half of the circuit as below:

$$I_y = g_{m3a}V_{gs3a} + \frac{Vin_2\mu_{1a} - Vin_1\mu_{13}}{(h \times r_{ds0})(1+\mu_{1a}) + r_{ds1a} + r_{ds13}} \quad (11)$$

$$V_{gs3a} = [\frac{1}{g_{m3b}} \parallel r_{ds3b} \parallel r_{ds3c} \parallel R_{11}](g_{m3c}V_{gs3c} + \frac{Vin_1\mu_{2b} - Vin_2\mu_{14}}{(h \times r_{ds0})(1+\mu_{2b}) + r_{ds2b} + r_{ds14}}) \quad (12)$$

$$V_{gs3c} = [\frac{1}{g_{m3d}} \parallel r_{ds3d} \parallel R_{17}](\frac{Vin_2\mu_{1c} - Vin_1\mu_{17}}{(h \times r_{ds0})(1+\mu_{1c}) + r_{ds1c} + r_{ds17}}) \quad (13)$$

and finally:

$$I_y = Vin_2(N) - Vin_1(M) \quad (14)$$

where

$$M = [\frac{g_{m3a}}{g_{m3b}}(\frac{g_{m3c}\mu_{17}}{g_{m3d}(h \times r_{ds0})(1+\mu_{1c}) + (r_{ds1c} + r_{ds17})} - \frac{\mu_{2b}}{r_{ds0}(1+\mu_{2b}) + r_{ds2b} + r_{ds14}}) + \frac{\mu_{13}}{r_{ds0}(1+\mu_{1a}) + r_{ds1a} + r_{ds13}}] \quad (15)$$

$$N = [\frac{g_{m3a}}{g_{m3b}}(\frac{g_{m3c}\mu_{1c}}{g_{m3d}(h \times r_{ds0})(1+\mu_{1c}) + (r_{ds1c} + r_{ds17})} - \frac{\mu_{14}}{r_{ds0}(1+\mu_{2b}) + r_{ds2b} + r_{ds14}}) + \frac{\mu_{1a}}{r_{ds0}(1+\mu_{1a}) + r_{ds1a} + r_{ds13}}] \quad (16)$$

Again considering Equations (15) and (16), it can be seen that if 'M' is adjusted to be equal to 'N', satisfying Equation (17), I_y will be zero for the common mode signals yielding infinite CMRR, while providing double boost for differential mode signals.

$$\begin{cases} \mu_{17} = \mu_{1c} \\ \mu_{14} = \mu_{2b} \\ \mu_{13} = \mu_{1a} \end{cases} \quad (17)$$

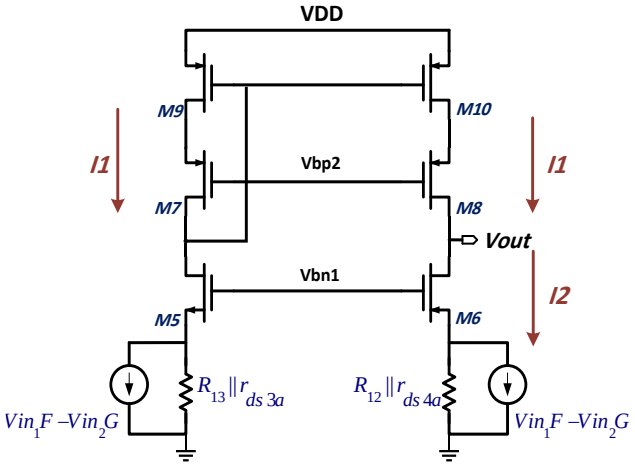


Figure 4: Output stage analysis of proposed RFC structure

Figure 4 shows the output stage of the proposed amplifier along with the small signal equivalent of input stage. Considering the aforementioned equations and this figure, we have:

$$I_1 = \frac{(Vin_1M - Vin_2N)(R_{13} \| r_{ds\,3a} \| \frac{1}{g_{m9}(1+\mu_5)})}{\frac{1}{g_{m9}(1+\mu_5)}} \quad (18)$$

$$\equiv (Vin_1M - Vin_2N)$$

$$I_2 = \frac{(-Vin_1F + Vin_2G)(R_{12} \| r_{ds\,4a} \| \frac{1}{g_{m10}(1+\mu_6)})}{\frac{1}{g_{m10}(1+\mu_6)}} \quad (19)$$

$$\equiv (-Vin_1F + Vin_2G)$$

The output voltage can be written as:

$$I_{out} = I_2 - I_1 = -V_{in_1}(F+M) + V_{in_2}(G+N) \quad (20)$$

$$V_{out} = (I_2 - I_1)R_{eq} = (-V_{in_1}(F+M) + V_{in_2}(G+N))R_{eq} \quad (21)$$

Input voltages can be written as follows:

$$V_{in_1} = V_c - \frac{V_d}{2}, \quad V_{in_2} = V_c + \frac{V_d}{2} \quad (22)$$

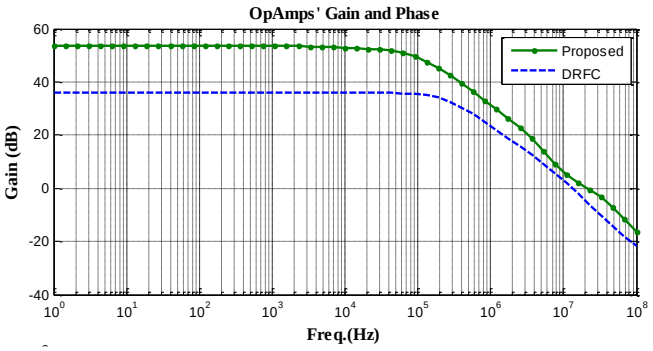
$$A_d = \frac{V_{od}}{V_d} = \frac{R_{eq}}{2}(F + M + N + G) \quad (23)$$

$$A_c = \frac{V_{oc}}{V_c} = R_{eq}(F + M - G - N) \quad (24)$$

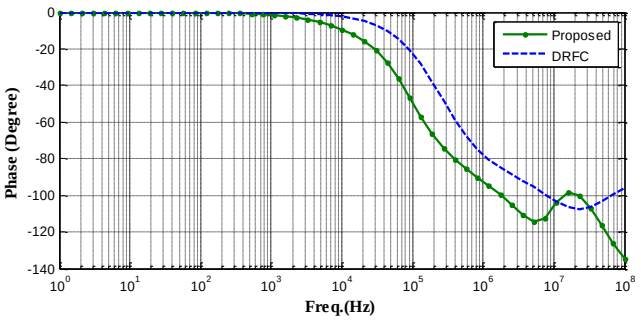
Finally we can calculate the CMRR as follow:

$$CMRR = \frac{A_d}{A_c} = 1 + \frac{2}{\frac{F+M}{N+G} - 1} \quad (25)$$

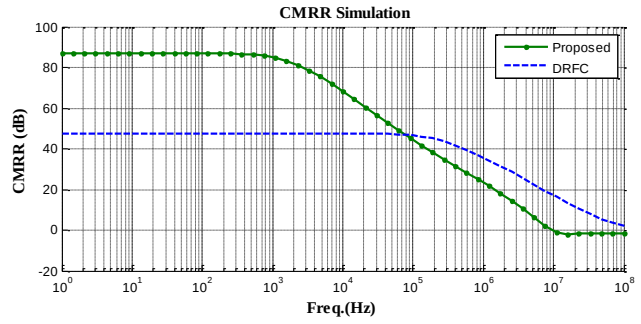
Replacing Equations (23) and (24) in Equation (25), it is clear that V_{in1} and V_{in2} appear with different signs in the output current equation. This shows that despite of eliminating Cascode transistors for current mirrors and using the CMRR Magnifier block, more attenuation in common mode signal is obtained, resulting in yielding relatively higher Common mode rejection ratio. For $F + M = N + G$, the denominator of CMRR equation is zero and CMRR will theoretically approach infinite. To achieve this situation, Equations (10) and (17) must be satisfied at the design phase.



(a)



(b)



(c)

Figure 5: Simulated (a) Gain, (b) Phase and (c) CMRR versus DRFC OTA.

III. Simulation Results

The conventional DRFC and the proposed CMRFC OTAs were simulated in 180 nm CMOS Technology. For a fair comparison, similar conditions and transistor aspect ratios were considered. In the proposed structure, the Cascode transistors of the conventional RFC amplifiers require a higher voltage supply for proper operation of the circuit to increase the power consumption of the circuit. These transistors were replaced by M_{12}-M_{17} transistors.

Hence, the voltage supply of the proposed CMRFC amplifier can be reduced to half the amount required for the conventional DRFC. The proposed structure was simulated considering a voltage supply of 1.5 volts. The proposed CMRFC amplifier achieved approximately 18dB higher gain and about 6-degree higher phase margin compared to its conventional counterpart, as shown in Figure 5a and 5b. Utilizing the new scheme, 39dB improvement was obtained for CMRR in comparison to the conventional circuit, while requiring supply voltage as low as 1.5 volt. The results of the CMRR and Monte Carlo simulation are shown in Figures 5c and 6, respectively. The results prove the qualitative operation of the CMRFC OTA in comparison to its counterpart.

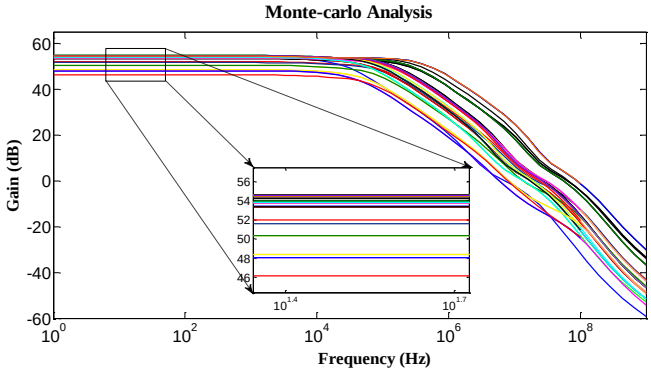


Figure 6: Monte Carlo analysis of the proposed CMRFC OTA with 40 runs

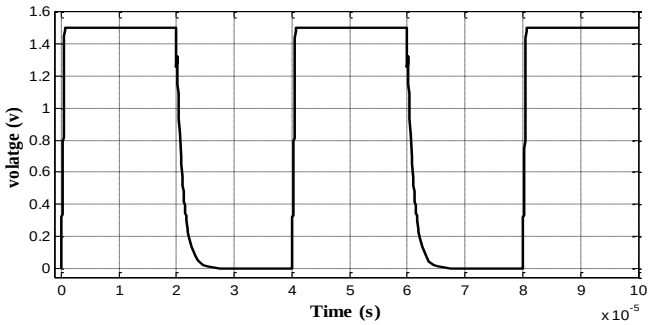


Figure 7: Transient response of the proposed structure applying a pulse voltage as high as 1.5 volt to its input.

Transient response of the proposed structure, which applies a pulse voltage as high as 1.5 volt to its input is shown in Figure 7.

The comparative results of the proposed CMRFC structure versus DRFC and some other similar works are summarized in Table 1. The most distinguishing features of the proposed structure are the ultra-low power consumption and the very small bias current.

IV. CONCLUSION

In this paper, a new recycling folded Cascode OTA based on a novel CMRR magnifier block (CMRFC) was presented. The principle of its operation compared to the conventional recycling folded Cascode OTA was discussed. In the proposed structure, the supply voltage significantly decreased due to the elimination of Cascode transistors. Common mode current was strictly eliminated by CMRR magnifier block, which yielded to a relatively high CMRR compared to the conventional structure. The DC bias voltage of the Cascode stage was also eliminated due to the utilization of the self Cascode structure.

The lower supply voltage and the elimination of the bias voltage in the CMRR amplifier block have significantly decreased the power consumption of the circuit, which makes the circuit suitable for many low-voltage low-power applications. Using the CMRR block and eliminating the Common Mode Current have also resulted in an increase in the CMRR.

The CMRFC OTA was simulated in 180nm CMOS technology along with the conventional DRFC OTA structure for a fair comparison. The simulation results yielded 53.4 dB DC-gain, 80.32-degree phase margin and 86.87 dB CMRR with 1.5 volt supply voltage for the proposed OTA, which made it suitable for low-voltage applications.

Table 1
The Performance Summary and Comparison with Other Works

Reference	CMRFC	DRFC [14]*	[18]	[12]	[19]
Technology [nm]	180	180	65	180	180
supply voltage [v]	1.5	3	2	1.8	1.8
Bias current [µA]	37.6	173.4	-	-	-
Capacitive load [pF]	1	1	1	5.6	5.6
DC Gain [dB]	53.4	35.3	48.4	69.2	71
Phase-margin [deg]	80.32	74.33	61.1	70.6	58.1
CMRR [dB]	86.87	47.5	-	-	-
DC power [µw]	49.59	520.2	1240	1440	2180
Input referred noise $[\mu V/Hz^{1/2}]$	53.12	16.9	30.8	48.5	48.2

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