High-Speed Low Power CMOS Comparator Using Forward Body Bias Technique in 0.13 µm Technology

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***Abstract*—This paper presents the design of high speed and low power CMOS comparator using a forward body bias technique in 0.13-µm technology. Three types of CMOS comparators' topologies have been designed in order to compare the performances of speed and power with the conventional comparator. Based on the analysis, the double-tail dynamic comparator is chosen since it shows better performance for high speed and low power. Therefore, a modified high-speed, low power double-tail dynamic comparator is proposed by using a forward body bias technique in order to reduce the supply voltage. The proposed dynamic comparator is implemented in Silterra 0.13-µm CMOS technology with the supply voltage of 1.2 V and sampling frequency of 500 MHz using Cadence EDA tool. The simulation results show that the total power of 152.67 µw with the delay of 72.5 ps is obtained. It can be seen that the proposed dynamic comparator has significantly reduced both the power and delay time compared to the previous design.**

***Index Terms*—CMOS; Analog Design; Comparator; High Speed; Low Power.**

I. INTRODUCTION

In the modern digital world, the analogue-to-digital converters (ADCs) play a major role in every hardware device [1]. The speed and power consumption are the two main factors for today portable applications [2-4]. For the past several years, the CMOS technology scaling is the most important procedure for the improvement of circuit performances such as speed, delay and power. Besides, one of the ways to minimise power consumption is by supply voltage reduction technique as power relation to the square of supplying voltage. However, one cannot simply reduce the supply voltage as it will cause the delay problem becoming critical.

Comparators are the most important circuit to control the performance and the accuracy of ADCs. There are various types of comparator architecture have been proposed for high speed [5-10]. The most popular architecture is CMOS dynamic comparators [10]. The dynamic comparators are often called as a clocked comparator due to the clock sensitive, and output is responding only to the trigger of the clock. In [11], a regenerative stage and interface stage of the dynamic comparator is proposed. The interface stage includes all the transistors without cross-coupled inverters with two cross-coupled inverters of the regenerative stage. These two cross-coupled inverters are invented to supply the latching in order to force a fast decision making from the input terminal. The major drawback of the dynamic latch comparator is the unwanted power consumption caused by the circuit when the clock is low since both the outputs are pre-charged to VDD. A low power and high-speed dynamic latch comparator in 0.18 µm CMOS process by using charge sharing technique are proposed in [12]. The latch circuit with high input impedance is employed in dynamic charge sharing topology. Besides, the static power dissipation is avoided by using a rail to rail output swing. Furthermore, this topology has the advantage of high immune to the parasitic capacitances of the input transistors to the output nodes [13]. However, the main problem of this circuit topology is large power consumption during reset mode in the resistive dividing circuit which causes undesired power dissipation due to charge sharing and charge leakage from the circuit. Further, in [14], the conventional double-tail comparator is proposed. The main advantage of this comparator is that it can work at low voltages compared to the conventional dynamic comparator due to the less stacking of this topology. The operation of the double tail comparator is divided into two phases which are reset and comparison (decision making) phases. However, the delay is still higher even though the speed is high.

In this paper, a comprehensive study about the speed and power of the double-tail comparator has been presented. Two types of the double-tail comparator of high speed and low power high speed based on the architecture in [14] are proposed and simulated using 0.13-µm CMOS technology. Furthermore, high-speed low power double-tail comparator using a forward body bias technique is proposed to improve delay and speed with low power. This paper is organised as follows: in Section 2, the design implementation of three architectures of the double-tail comparator is discussed. Section 3 presents the design specifications of input and the transistors' dimension. The simulation results achieved from the proposed comparators are presented in Section 4. Finally, Section 5 concludes the overall achievement.

II. DESIGN IMPLEMENTATION

Three types of CMOS comparators' topologies have been designed in order to compare the performances of speed and power with the conventional comparator. The first comparator is a high-speed double-tail comparator. The schematic of the high-speed dynamic double-tail comparator

is depicted in Figure 1 (not include dash line box). The double-tail structure has advantages for low-voltage applications. The high-speed comparator can be achieved by speeding up the latch regeneration that can be done by increasing the rate of voltage change of nodes F+ and F-. Two control transistors of MC1 and MC2 are added in a cross-coupled manner and parallel with M3 and M4 transistors. The operation of the comparator is explained in [14].

In the previous high-speed double-tail comparator structure, when the control transistors of MC1 or MC2 is turned ON, static power consumption is existed due to current from VDD is flew to the ground through input and tail transistors of MC1, M1, and MTAIL1. This issue can be solved by implementing a power gating technique. Therefore, the second comparator of low power high-speed double-tail comparator is redesigned with two additional NMOS switches. The NMOS switches of MSW1 and MSW are added under the input transistors M1 and M2 as shown in Figure 1 (see dash line box). The operation of the circuit is discussed in [14].

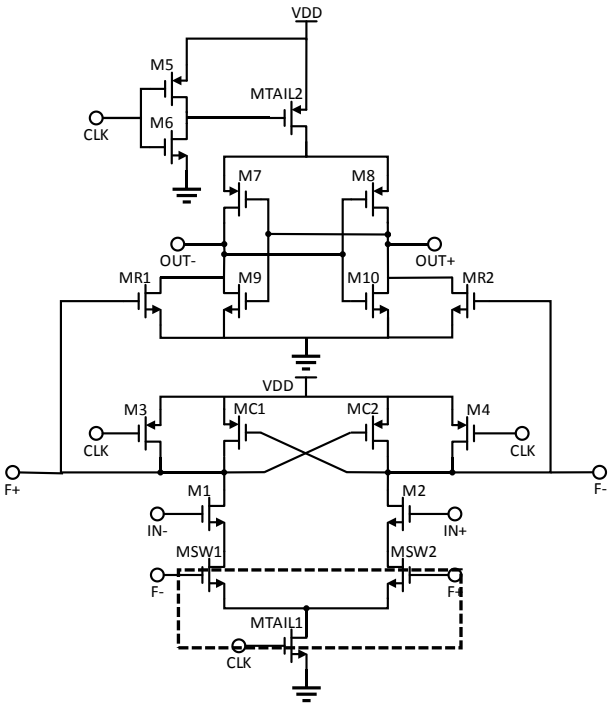


Figure 1II: High speed and low power high-speed double-tail comparator

In a low power design, voltage supply reduction is the most effective method for reducing the power consumption due to the CMOS power formula which implies a square relation with the supply voltage. However, one cannot simply reduce the supply voltage because it will also reduce the voltage across the gate and the source of a MOS transistor. Thus, the low threshold is strongly desired in order to operate at the low supply voltage. All of these can achieve by implementing the forward body bias technique. Therefore, the third type of comparator is proposed by modifying the low power high-speed double-tail comparator with another two additional NMOS switches as shown in Figure 2. The two additional NMOS switches MSW3 and MSW4 are added to the switching transistors MSW1 and MSW2. Furthermore, the body terminal of input transistors M1 and M2 and the switching transistor MSW3 and MSW4 are connected to VBIAS source. These additional switches MSW3 and MSW4 use the power gating technique to reduce the standby power of the circuit that works similar to the previous design.

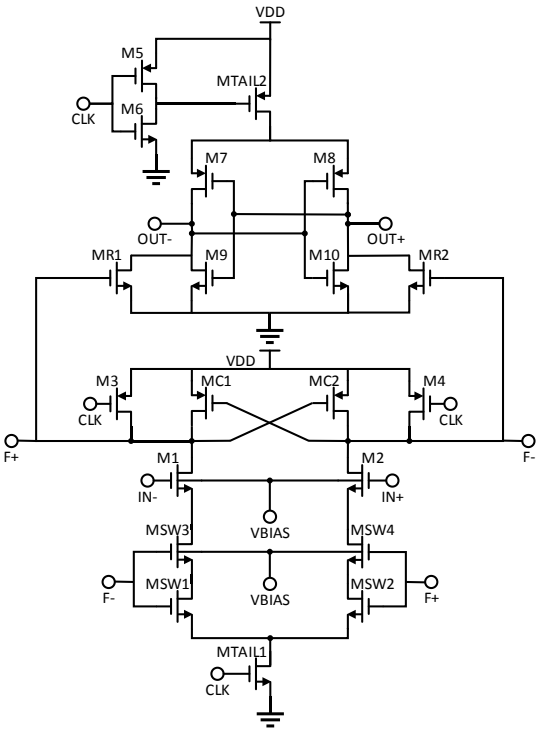


Figure 2: High-speed, low power double-tail comparator using a forward body bias technique

Besides, the body bias involved here is by connecting the body of the transistor to a voltage source instead of using the conventional way which is connecting it to the source terminal of the transistor. By supplying a positive voltage source, the transistor body works under the forward body-bias mode, and the threshold voltage is reduced. This forces the transistor to operate in a saturation region allowing the supply voltage to be reduced. Consequently, the proposed design is able to operate at a low supply voltage with better performance.

III. Simulation Result

The proposed circuit has been simulated in Cadence Analog Design Environment using Spectre Simulator. The supply voltage (VDD) of the circuit is set at 1.2 V. The negative input terminal (IN-) is connected to piece-wise linear (PWL) voltage source to allow the transient voltage waveform to be swept according to the defined time. The input (IN-) is set to be swept from 0 V to 1.2 V throughout the time interval of 10 ns. While the positive input terminal (IN+) is connected to a 0.6 V DC voltage source functioning as a reference voltage. The comparator output offset voltage is determined by performing a DC analysis. While the measurements of all comparators' rise time, fall time, propagation delay, speed, slew rate and power consumption are done in transient analysis. In the DC response, the offset is determined by the voltage of the comparator output terminal when both the input terminals are shorted to the ground. The speed of the comparator is determined by the factors of signal rise time, fall time, propagation delay [15]. There are two components determine the power consumption of designed comparator which is static power consumption

and also dynamic power consumption. The static power consumption of the comparators is calculated by multiplying the total bias current (Ibias) which is the result of leakage current with the total VDD. Meanwhile, the calculation of comparators' dynamic power consumption is based on the current flow when transistors are switching from ON to OFF [16]. The rise time and fall time of the input signal plus the frequency of comparator during switching, as well as the internal nodes of the circuit, have an effect on the duration of the current spike during dynamic power analysis.

Figure 3 shows the DC analysis of the designed high speed, low power high speed and the proposed low power high speed using a forward body bias technique double-tail dynamic comparator. In this analysis, both the input positive and negative voltage is connected to the ground in order to observe the output offset voltage of the device. From the simulated result shown in Figure 3, the output offset voltage of the high-speed, low power double-tail comparator using forward body bias is further reduced to 29.18 mV. The output offset voltage obtained is the lowest compared to the other two designs.

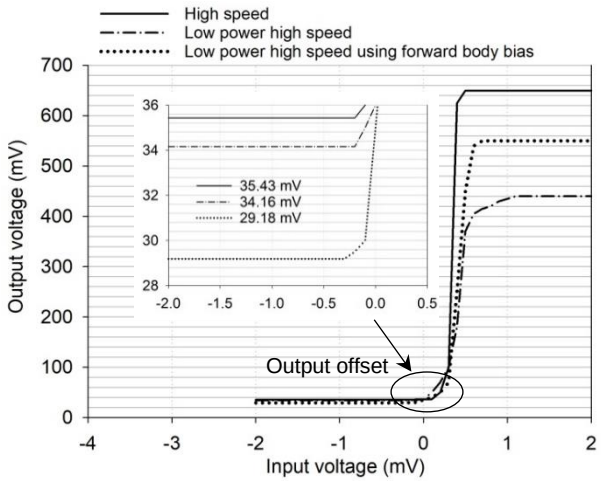
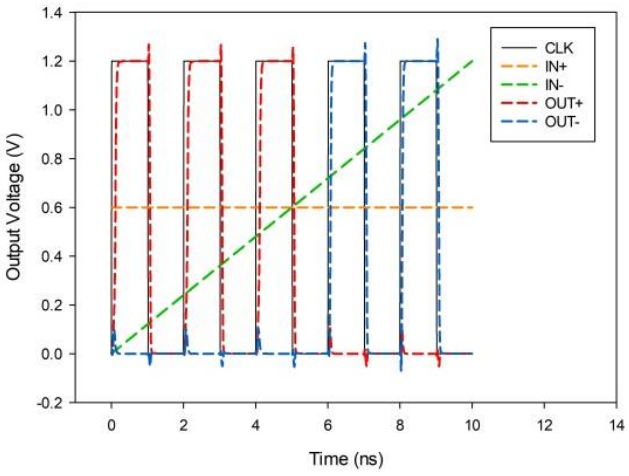


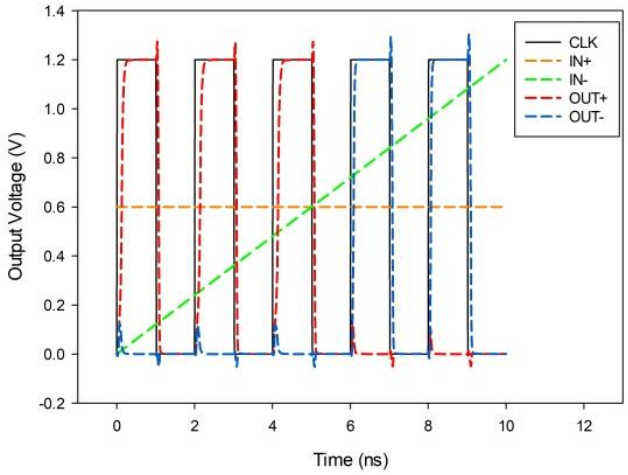
Figure 3: DC response of high speed, low power high speed and low power high speed using a forward body bias technique double-tail comparator

Figure 4 shows the transient response of the proposed double-tail dynamic based comparator. For the transient response, the input voltage source is a piece-wise linear voltage source, and the reference voltage source is a DC voltage source. From the transient response shown in Figure 4, it is observed that the output of the design has met the targeted operation. All the input and output operations are the same as the previous design.

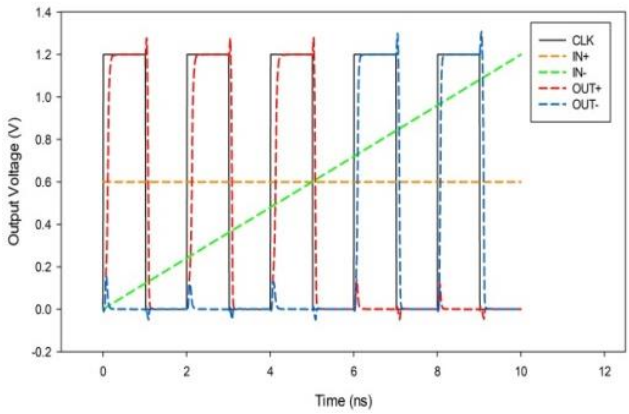
Figure 5 shows the layout of the proposed high-speed, low power double-tail comparator using a forward body bias technique. The proposed layout is designed using Cadence Virtuoso® XL layout using Silterra 0.13-µm CMOS technology. The layout consists of 3 metal layer process. The proposed layout chip occupied 14.90 µm widths multiply by 14.50 µm length. The total area of the chip is 216.05 µm2. The input port VDD and GND are delivered using a metal 2 layer while other inputs and output port are drawn by using the metal 1 layer. A total of 20 transistors are occupied in the layout design which consists of 12 NMOS transistors and the remaining of 8 PMOS transistors.



(a)



(b)



(c)

Figure 4: Transient response of double-tail comparator, (a) High speed, (b) Low power high speed, (c) Low power high speed using forward body bias technique

Table 1 shows the summary of the proposed three types of high-speed double-tail comparator with a conventional double-tail comparator. The proposed double-tail comparator using a forward body bias technique shows significant improvement of the total power and slightly improves the speed and offset voltage. The power is decreased 10.5 % as compared to the conventional double-tail comparator.

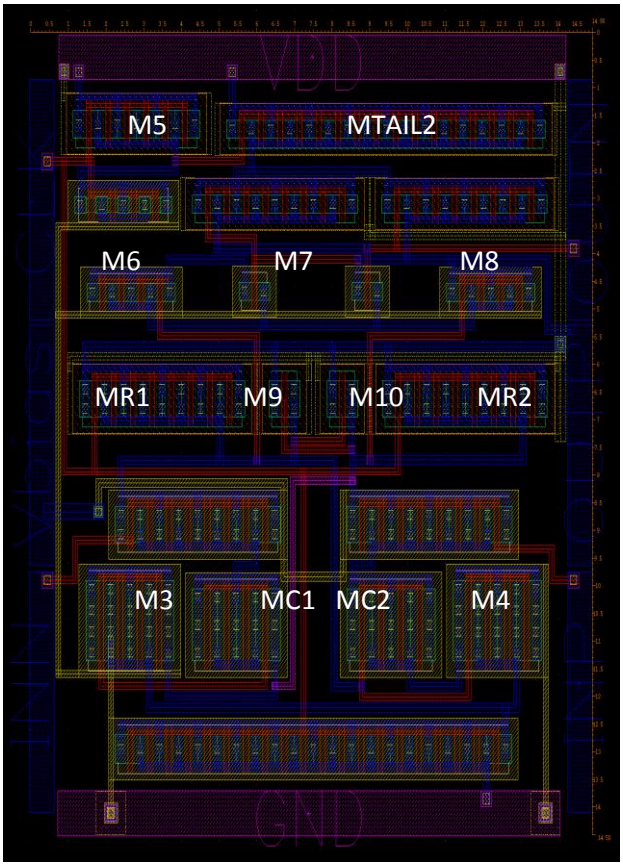


Figure 5. The layout of a proposed high-speed low power dynamic based comparator using forward body bias technique

The proposed design performance with the previously published works is shown in Table 2. In [15], the CMOS comparator using a dynamic latch is proposed by combining the good features of the resistive dividing comparator and the differential current sensing comparator. The delay demonstrates significant improved with slightly lower the power consumption. Two stages dynamic comparator is presented in [8] in order to reduce the power consumption by a factor of two and improves speed. The power obtained is similar as proposed in [15]. Furthermore, the method proposed in [14] is modified from a conventional double comparator for low power and fast operation by adding a few transistors to strengthen the regeneration of positive feedback. The proposed design can operate at 1.2 V to 0.6 V supply while consuming 1.4 mW and 153 µW, respectively. Unfortunately, the proposed method obtains a high delay. The proposed two-stage dynamic comparator consists of a pre-amplifier of the first stage and a dynamic latch of the second stage that increases the total power consumption about 50% as compared to [15] and [7]. In [19], the comparator benefits from two stages and two operational phases to reduce the offset voltage which produces positive feedback. Therefore, low power consumption is obtained and slightly increased the delay of the circuit.

As can be seen, the proposed comparator in this work obtains low power with the improvement of speed. This proves that the proposed design is suitable to be used for high speed and low power ADC applications where battery life is a critical issue.

Table 1
Summary of the High-Speed Double-Tail Comparator with Conventional Double-Tail Comparator Based on the Author Simulations

Comparator	Conventional Double-Tail	High speed	Low power high speed	Low power high speed using forward body bias
Technology (µm)	0.13	0.13	0.13	0.13
Number of transistor	14	16	18	20
Sampling Frequency (MHz)	500	500	500	500
Supply Voltage (V)	1.2	1.2	1.2	1.2
Total Leakage Current (µA)	50.16	175.02	91.50	69.15
Offset Voltage (mV)	595.3	35.43	34.16	29.18
Slew rate (GV/ns)	16.08	21.98	21.21	20.17
Rise Time (ps)	59.68	43.67	45.26	47.59
Fall Time (ps)	46.02	37.17	38.16	41.47
Delay (ps)	79.09	70.12	69.53	72.5
Speed = 1/Delay (GHz)	12.64	14.26	14.38	13.79
Static Power Consumption (µW)	60.19	210.02	109.80	82.98
Average Dynamic Power Dissipation (µW)	110.3	84.14	63.89	69.69
Total Power (µW)	170.49	294.16	173.69	152.67

Table 2
Performance Comparison with Previously Published Works

Reference	[5]*	[7]	[14]*	[15]	[19]	This Work
Technology (µm)	0.18	0.18	0.18	0.18	0.18	0.13
Supply Voltage (V)	N/A	N/A	1.2 / 0.6	1.8	1.0	1.2
Total Power (µW)	420	230	1400(1.2V) 153(0.6V)	242.6	51	152.67
Delay (ps)	220	150	550	66.59	152	72.5
Speed (GHz)	4.55	6.67	1.82	15.01	6.58	13.79
Offset voltage (mV)	2.5	2.5	7.8	N/A	33	29.18
Clock (GHz)	0.5	3.7	2.5	N/A	1	0.5
Area (μm^2)	486	N/A	392	528	N/A	216

*Post-layout simulation

IV. CONCLUSION

In this work, three types of comparator topology are presented in order to analyses the best performance of speed and power. Based on the analysis, the double-tail dynamic comparator is chosen since it has better performance compared to other architectures. The proposed technique increases the latch regeneration speed of comparator since speed is the first priority in designing a high-speed

comparator. Besides four control transistors are added to emulate the operation of the latch which helped to reduce the static power consumption of the comparator. The novelty of the design is that the proposed design has employed forward body bias technique; it mainly reduces the supply voltage in which consequently reduces the power consumption. The proposed dynamic comparator is implemented in Silterra 0.13-µm CMOS technology with the supply voltage of 1.2 V and a sampling frequency of 500 MHz. The simulation results indicate that the total power of 152.67 µw with the delay of 72.5 ps is obtained. It can be seen that the proposed comparator using forward body bias has significantly improved both the speed and power consumption compared to the previous works.

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