RF/Analog Performances Enhancement of Short Channel GAAJ MOSFET using Source/Drain Extensions and Metaheuristic Optimization-based Approach

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Abstract— **This paper presents a hybrid strategy combining compact analytical models of short channel Gate-All-Around Junctionless (GAAJ) MOSFET and metaheuristic-based approach for parameters optimization. The proposed GAAJ MOSFET design includes highly extension regions doping. The aim is to investigate the impact of this design on the RF and analog performances systematically and to show the immunity behavior against the short channel effects (SCEs) degradation. In this context, an analytical model via the meticulous solution of 2D Poisson equation, incorporating source/drain (S/D) extensions effect, has been developed and verified by comparing it with TCAD simulation results. A comparative evaluation between the proposed GAAJ MOSFET structure and the classical device in terms of RF/Analog performances is also investigated. The proposed design provides RF/Analog performances improvement. Furthermore, based on the presented analytical models, Genetic Algorithms (GA) optimization approach is used to optimize the design of S/D parameters. The optimized structure exhibits better performances, i.e., cut-off frequency and drive current are improved. Besides, it shows superior immunity behavior against the RF/Analog degradation due to the unwanted SCEs. The insights offered by the proposed paradigm will help to enlighten designer in future challenges facing the GAAJ MOSFET technology for high RF/analog applications.**

Index Terms— **Analytical Model; GAAJ MOSFET; GA Optimization; Short Channel Effects.**

I. Introduction

Continuous downscaling of the classical MOS devices makes them more prominent for RF/Analog applications. Nevertheless, the principal challenges that CMOS technology is confronting are the SCEs. Harsh scaling of MOSFET dimensions leads to several SCEs in terms of drain induced barrier lowering (DIBL), velocity saturation and series resistance. The SCEs degrade device RF/Analog performance and increase power dissipation [1, 2].

As a result, the exploration of novel designs and architectures is under deep investigation in order to reduce the unwanted SCEs and to enhance the device performances. In order to overcome the SCEs problems, a range of engineering structures is suggested and approved experimentally [3-5]. Among these schemes, GAAJ MOSFET constitutes the superlative structure and is an attractive candidate for high RF/Analog applications because of their perfect gate controllability, outstanding scalability, small leakage, and improved carrier transport property [6, 7]. However, at the nanoscale level, we are confronted to the challenging task of creating junctions in conjunction with costly thermal and doping techniques [8]. Besides, in order to preserve random dopant fluctuation, ultrafast annealing techniques are necessary. It is worthy to note that these techniques are complicated and costly. To surmount these drawbacks, GAAJ MOSFET is suggested [9, 10]. Since the device switching is controlled from all its faces, the GAAJ design is very appropriate for manufacturing devices. In contrast with conventional device manufacturing process, the junctionless (JL) one is better [11, 12]. However, in case of high-performance applications, many enhancements are needed because of imperfect performance. In order to push further this device, on the basis of analytical models, the novel customized paradigm can also be explored to enhance the drain current ability and to reduce SCEs drawbacks. When the high drain current value is in demand, essentially for RF/Analog applications, the GAAJ including S/D extensions has been found as an attractive technology to alleviate the SCEs [13, 14].

For long channel GAA MOSFET, authors of [15, 16] showed that S/D extensions permit a lower series resistance value and better RF/Analog performances. Within this framework, numerous works are made to explore and to enhance the performance of this device [7-14, 16-19].

However, no investigations are carried out for short channel GAAJ MOSFET. Higher channel doping concentration for short channel GAAJ MOSFET without S/D extensions causes a Carrier Mobility Degradation (CMD) [17, 18] that dramatically decreases the RF/Analog performances.

To deal with this problem, we propose a GAAJ MOSFET with highly doped S/D extensions regions and uniformly lesser channel doping concentration. In addition, no investigation based on short channel drain current model and device optimization parameters has been explored to enhance the RF/Analog device performances. In this context, numerous optimization methods have been reported in the literature to improve the performance of GAAJ MOSFET. These methods are generally based on empirical computations and numerical simulations [20, 21]. This paper aims to propose a novel compact model is permitting geometrical optimization to design S/D extensions leading to high RF/Analog technical capabilities by increasing the device immunity against the SCEs.

II. MODELING METHODOLOGY

A. Device structure

In this paper, an analytical modeling of short channel GAAJ MOSFET including extension regions is proposed to calculate the drain current and the RF/Analog parameters. 3-D and cross-sectional views of the investigated device are shown in Figures 1a and 1b, respectively.

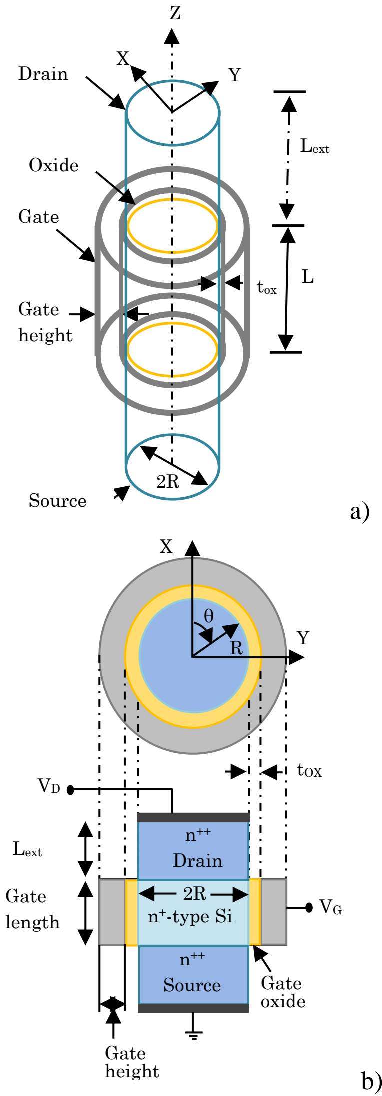

Figure 1: (a) Schematic structure of the cylindrical GAAJ MOSFET showing different directions (b) Schematic cross sectional 2-D structure of the cylindrical GAAJ MOSFET showing the related variables

In the case of classical GAAJ MOSFET without S/D extensions, the channel body doping is homogeneous in concentration and type. In contrast, the proposed GAAJ MOSFET has S/D extensions with high proportion doping than the channel body.

B. Model development

In this section, first, we develop a basic long channel model by solving 1D Poisson equation, and then we incorporate the short channel effects into our model.

According to Figure 1, by accounting for the long channel model [22], the 2-D Poisson equation that governs the channel electrostatics potential reduces to its 1-D form. Furthermore, the quantum confinement impacts become insignificant when the silicon film thickness is superior than 5 nm; consequently, they can be ignored in this study [22].

The considered GAA device has N_d doping impurities concentration. By applying cylindrical coordinates to this model, Poisson equation is expressed as follows:

$$\frac{\partial^2\phi}{\partial r}+\frac{1}{r}\frac{\partial\phi}{\partial r}=\frac{qN_d}{\varepsilon_{Si}}\left(e^{\frac{\phi(r)-V}{V_T}}-1\right) \quad (1)$$

$\phi(r)$ and q represent, respectively, the silicon film potential distribution and the electron charge, N_d is donor concentration, ε_{Si} is the silicon dielectric permittivity, V and V_T are, respectively, the potential shift (quasi-Fermi level) and the thermal voltage.

Boundary conditions for 1-dimentional Poisson equation can be written as:

i. For zero radius, the potential is

$$\phi(0)=\phi_0 \quad (2)$$

and the corresponding electric field:

$$\left.\frac{d\phi}{dr}\right|_{r=0}=0 \quad (3)$$

ii. At Source/Channel junction

$$V(0)=V_i \quad (4)$$

ii At Drain/Channel junction

$$V(L)=V_i+V_{ds} \quad (5)$$

Here ϕ_0 is the channel body center potential; V_i denotes the built-in potential and V_{ds} is the S/D voltage biasing. V_i can be written as

$$V_i=V_T\ln\left(\frac{N_{dext}}{N_d}\right) \quad (6)$$

N_{dext} denotes the doping concentration of the S/D extension.

Supposing the same parabolic potential profile according to [22], the potential can be obtained by taking into account the above formulated conditions (i, ii, iii):

$$\phi(r)=\frac{\phi_S-\phi_0}{R^2}r^2+\phi_0 \quad (7)$$

At the Si/SiO$_2$ limit, ϕ_S is the surface potential and R is the radius of the cylindrical channel.

To obtain the mobile charge density Q_{mob} expression, the application of the Gauss theorem to the semiconductor circumference is required; the relationship between the potential and the mobile charge is obtained by

$$\left.\frac{\partial\phi}{\partial r}\right|_{r=R} = \frac{Q_{mob} - Q_{fix}}{\varepsilon_0\varepsilon_{Si}} \quad (8)$$

The use of the mentioned boundary conditions (i, ii, iii) leads to the equation of mobile charge density Q_{mob} as follows:

$$Q_{mob} = Q_{fix}Q_{cp}\frac{1-\exp\left(\dfrac{R(-Q_{mob}+Q_{fix})}{2\varepsilon_0\varepsilon_{Si}V_T}\right)}{Q_{mob}-Q_{fix}}\exp\left(\frac{\phi_S - V}{V_T}\right) \quad (9)$$

Q_{fix} refers to the fixed charges density calculated from $Q_{fix} = qN_dR/2$, and Q_{cp} is a charge deduced from basic parameters $Q_{cp} = 2\varepsilon_0\varepsilon_{Si}V_T/R$.

The surface potential equation, in terms of mobile charge Q_{mob}, can be obtained by combining Equations (2-5), (8) and (9):

$$\phi_S = V_{gs} - V_{fb} - \frac{Q_{mob}-Q_{fix}}{C_{OX}} \quad (10)$$

V_{gs} and V_{fb} denote, respectively, the gate-source biasing voltage and the flat band voltage. This latter is defined as:

$$V_{fb} = \phi_{ms} + V_T\ln(N_d/n_i) \quad (11)$$

and

$$C_{OX} = \varepsilon_{OX}/R\ln\left(1+\frac{t_{OX}}{R}\right) \quad (12)$$

represents the oxide capacitance of GAA structure, where t_{OX} and ε_{OX} are the thickness and the permittivity of the oxide, respectively.

To investigate the device behavior accurately, we need to estimate the channel charge Q_{mob} for both accumulation and depletion modes. Its expression is found by using Equation (9) and the mathematical Lambert-W function:

$$Q_{mob}(V) = C_{OX}V_T LW(\xi)\exp(v(V)) \quad (13)$$

The parameter ξ is given by the following expression:

$$\xi = \frac{Q_{fix}Q_{cp}}{C_{OX}V_T}\frac{\left(1-\exp\left(\dfrac{Q_{fix}-Q_{m1}(V)}{Q_{cp}}\right)\right)}{Q_{m1}(V)-Q_{fix}}$$

According to [22], the Lambert function is:

$$LW(z) = \ln(1+z)\left(1-\frac{\ln(1+\ln(1+z))}{2+\ln(1+z)}\right) \quad (14)$$

and

$$Q_{m1}(V) = \frac{Q_{cp}C_{OX}V_T}{(Q_{cp}+C_{OX}V_T)}LW(z) \quad (15)$$

z is defined as follows:

$$z = \frac{(Q_{cp}+C_{OX}V_T)Q_{fix}Q_{cp}}{Q_{cp}C_{OX}V_T}\frac{\exp\left(\dfrac{Q_{fix}-Q_{m2}(V)}{Q_{cp}}\right)}{Q_{m2}(V)-Q_{fix}}\exp(v(V))$$

$$Q_{m2}(V) = 2C_{OX}V_T LW\left[\frac{\sqrt{Q_{fix}Q_{cp}}}{C_{OX}V_T}\exp(v(V)/2)\right] \quad (16)$$

where $v(V) = (V_{gs}+V_{fb}+Q_{cp}/C_{OX}+V)/V_T$.

To facilitate the investigation of the SCEs on the GAAJ MOSFET and to give more insight on the degradation of the device performances, an improvement of the accuracy of the model around the threshold voltage is necessary. According to [23], final and further accurate expression of the mobile charge density Q_{mob} is:

$$Q_{mob} = \frac{Q_{cp}C_{OX}V_T}{(Q_{cp}+C_{OX}V_T)}LW(z) \quad (17)$$

where z is as follows:

$$z = \frac{(Q_{cp}+C_{OX}V_T)Q_{fix}Q_{cp}}{Q_{cp}C_{OX}V_T}\frac{\exp\left(\dfrac{Q_m^0-Q_{fix}}{Q_{cp}}\right)-1}{Q_m^0-Q_{fix}}\exp\left(v+\frac{Q_{fix}}{fQ_{cp}}\right)$$

with $f = 1+0.2\dfrac{Q_m^0}{Q_{fix}}\exp\left(-\dfrac{Q_m^0}{Q_{fix}}\right)$

Q_m^0 is given by Equation (13). f is the fitting parameter.

Taking into account the modeling scheme based on the drift-diffusion transport formalism, the straightforward approach to calculate drain current is to simply integrate the mobile charge between the biasing voltage S/D:

$$I_{ds} = \frac{R\mu_n V_T}{L}\int_{V_1}^{V_2} Q_{mob}dV \quad (18)$$

where $V_1 = V_i$

$V_2 = V_{ds} + V_i$

By integrating Q_{mob} from V_1 to V_2 in Equation (18), the drain current that takes into consideration the high doped extended S/D regions, can be expressed by the following:

$$I_{ds} = \frac{R\mu_n V_T}{L}(F(V_{bi}) - F(V_i+V_{ds})) \quad (19)$$

and

$$F(V)=\frac{(Q_{cp}+C_{OX}V_T)Q_{mob}(V)^2}{2Q_{cp}C_{OX}V_T}+2Q_{mob}(V)-CQ_{mob}(V)\ln(1+\exp(\frac{Q_{mob}(V)-Q_{fix}}{2CQ_{cp}}))+Q_{fix}\ln\left[\frac{Q_{mob}(V)-Q_{fix}}{2Q_{cp}{}_{(\exp(\frac{Q_{mob}(V)-Q_{fix}}{2Qcp})-1)}}\right] \tag{20}$$

$$\mu_n=\mu_{\min}+\left(\frac{\mu_{\max}-\mu_{\min}}{1+\left(\frac{N_d}{N_{crit}}\right)^{\alpha}}\right) \tag{21}$$

where: μ_n = Semiconductor electron mobility.

The higher and the lower values of the silicon mobility are $\mu_{\max}=1400\,cm^2/Vs$ and $\mu_{\min}=688\,cm^2/Vs$. α and N_{crit} are two parameters having the following values $\alpha=0.71$ and $N_{crit}=10^{18}\,cm^3$.

The mobility degradation μ_{eff} is caused principally by the velocity saturation and the pinch-off effect that reduces the effective channel length dramatically. According to [24], this degradation is incorporated into the long channel model by substituting L with $L-\Delta L$, and μ_n with μ_{eff} in the drain current Equation (19),

Hence, our model implements the mobility degradation as:

$$\mu_{eff}=\frac{\mu_n}{\left(1+\left(\frac{\mu_n V_{deff}}{V_{sat(L-\Delta L)}}\right)^{\alpha}\right)^{\frac{1}{\alpha}}} \tag{22}$$

where: α = 2 for electrons
V_{deff} = effective drain voltage

V_{deff} saturates at the saturation voltage V_{sat} and is given as [25]:

$$V_{deff}=V_{sat}-V_{sat}\frac{\ln\left(1+\exp\left(A\left(1-\frac{V_d}{V_{sat}}\right)\right)\right)}{\ln(1+\exp(A))} \tag{23}$$

where: A = Parameter of smoothness

A guarantees a soft transition from V_d to its maximum value V_{sat}. We took $A=3$.

According to [24, 26], the saturation voltage can be expressed as:

$$V_{sat}=\frac{V_s}{\frac{V_s}{V_{\max}}+1} \tag{24}$$

with $V_s=\frac{Q_{mob}(0)}{C_{OX}}+\frac{V_{\max}}{\frac{V_{\max}}{V_{\min}}-1}$

Since the velocity saturation affects the characteristics above threshold voltage harshly, the maximum and minimum values of the saturation voltage that takes into consideration the electron carriers case are given as [24]:

$$V_{\max}=\alpha\frac{v_{sat}}{\mu_n}L \tag{25}$$

$$V_{\min}=2V_T \tag{26}$$

where: V_{sat} = Saturation velocity
L = Channel length

V_{sat} is considered in our paper as a fitting parameter ($v_{sat}=2\times10^7\,cm/s$). The pinch-off phenomenon affects drain current significantly in GAAJ MOSFET in terms of effective channel length. In the saturation region, the reduction in the effective channel length ΔL was calculated using a quasi 2D solving of Poisson equation. For our considered device, we used cylindrical coordinates (see Figure 1):

$$\frac{\partial^2\phi}{\partial r^2}+\frac{1}{r}\frac{\partial\phi}{\partial r}+\frac{\partial^2\phi}{\partial z^2}=\frac{qN_d}{\varepsilon_{SC}}\left(\exp(\frac{\phi-V}{V_T})-1\right) \tag{27}$$

where: $\phi(R,Z)$ = Potential
V = Quasi-Fermi level

Taking into consideration the fully depleted device and the parabolic potential profile form along the channel thickness, Equation (27) can be more practical as [27]:

$$\frac{\partial^2\Delta\phi(0,z)}{\partial z^2}=\frac{\Delta\phi(0,z)}{\lambda^2} \tag{28}$$

For the case of surface potential ($r=R$):

$$\frac{\partial^2(\phi(0,z)-\phi(R,L-\Delta L))}{\partial z^2}=\frac{\phi(R,z)-\phi(R,L-\Delta L)}{\lambda^2} \tag{29}$$

with

$$\lambda=R\sqrt{\frac{C_{Si}}{2C_{OX}}}$$

$$C_{Si}=\frac{\varepsilon_0\varepsilon_{Si}}{R}$$

Taking into account that

$$\left.\frac{\partial\phi(R,z)}{\partial z}\right|_{z=L-\Delta L}=\alpha\frac{v_{sat}}{\mu_n} \tag{30}$$

equation (29) is solved in a similar way as [23]:

$$\phi(R,z)-\phi(R,L-\Delta L)=\alpha\frac{\upsilon_{sat}}{\mu_n}\lambda\sinh\left(\frac{L-\Delta L-z}{\lambda}\right) \quad (31)$$

Notwithstanding the fact that the left side of the previous equation is $\phi(R,z)-\phi(R,L-\Delta L)=V_d-V_{deff}$, the effective channel length decrease ΔL can be expressed as [28]

$$\Delta L=\lambda\ln\left(\frac{(V_d-V_{deff})\left(1+\sqrt{1+\left(\frac{\alpha\frac{\upsilon_{sat}}{\mu_n}\lambda}{V_d-V_{deff}}\right)^2}\right)}{\alpha\frac{\upsilon_{sat}}{\mu_n}\lambda}\right)S \quad (32)$$

The fitting parameter S (empirical fitting parameter) was added to ensure that ΔL tends to 0 below the threshold voltage:

$$S=\sqrt{1-\frac{1}{1+\beta\frac{Q_{mob}(0)}{C_{eq}V_T}}} \quad (33)$$

$Q_{mob}(0)$ refers to the mobile charge at the source obtained from the long channel model. β is a parameter permitting the smoothness adjustment of the transition and C_{eq} is the equivalent gate capacitance,

$$\frac{1}{C_{eq}}=\frac{1}{C_{OX}}+\frac{1}{2C_{Si}} \quad (34)$$

The threshold voltage shift ΔV_{Th} which characterizes the DIBL effect is expressed as [22]:

$$\Delta V_{Th}=\frac{\sqrt{\Delta\phi_S e^{\frac{L}{\lambda}}-\Delta\phi_D}\sqrt{\Delta\phi_D-\Delta\phi_S e^{-\frac{L}{\lambda}}}}{Sinh\left(\frac{L}{\lambda}\right)} \quad (35)$$

The boundary conditions are as follows:

$$\Delta\phi_S=V_{bs}-\varphi_0^K \quad (36)$$

$$\Delta\phi_D=V_{bd}-\varphi_0^K+V_d \quad (37)$$

$\Delta\phi_S$ and $\Delta\phi_D$ represent the barrier height at the channel extremities, $\varphi_0^K=V_G-V_{Th}$ refers to the potential at the channel center, and V_{Th} represents the threshold voltage expressed by :

$$V_{Th}=V_{fb}-\frac{qN_DR}{4}\left(\frac{R}{\varepsilon_{SC}}+\frac{2}{C_{OX}}\right) \quad (38)$$

V_{bs} and V_{bd} represent the effective potential barrier height at the extended S/D regions, and are given by the following [23]:

$$V_{bs}=V_{bi}-\Delta\phi_S^b-\frac{qN_{dext}\lambda}{\varepsilon_0\varepsilon_{Si}}\left(1-\sqrt{1+2\varepsilon_0\varepsilon_{Si}\frac{\Delta\phi_S^b}{qN_{dext}\lambda}}\right) \quad (39)$$

$$V_{bd}=V_{bi}-\Delta\phi_D^b-\frac{qN_{dext}\lambda}{\varepsilon_0\varepsilon_{Si}}\left(1-\sqrt{1+2\varepsilon_0\varepsilon_{Si}\frac{\Delta\phi_D^b}{qN_{dext}\lambda}}\right) \quad (40)$$

with:

$$\Delta\phi_S^b=V_T\ln\left(1+\exp\left(\frac{V_{bi}-\varphi_0^k}{V_T}\right)\right) \quad (41)$$

$$\Delta\phi_D^b=V_T\ln\left(1+\exp\left(\frac{V_{bi}-\varphi_0^k+V_d}{V_T}\right)\right) \quad (42)$$

V_{bi} represents the junction equivalent built-in voltage given as follows

$$V_{bi}=V_{bi0}-\phi_F+V_T\ln\left(\frac{N_{dext}}{N_d}\right) \quad (43)$$

and

$$\phi_F=V_T\ln\left(\frac{N_d}{n_i}\right) \quad (44)$$

is the Fermi voltage in the channel. V_{bi0} is the barrier height relatively to the intrinsic level at the channel-source side.

In order to enhance the proposed model accuracy outside the sub-threshold regime, we consider that the rigorous DIBL and the degradation of the sub-threshold slope are essentially caused by the capacitive coupling between the S/D regions and the virtual cathode; so we can rewrite Equation (35) as a function of C_S and C_D as follows:

$$\Delta V_{Th}=\frac{C_S\Delta\phi_S+C_D\Delta\phi_D}{C_{eq}} \quad (45)$$

C_D and C_S refer to the capacitive coupling with the drain and source, respectively, and are given as follows [23]:

$$C_D=C_{eq}\frac{\Delta\phi_S\cosh(\frac{L}{\lambda})-\Delta\phi_D}{\sinh(\frac{L}{\lambda})\sqrt{2\Delta\phi_S\Delta\phi_D\cosh(\frac{L}{\lambda})-\Delta\phi_S^2-\Delta\phi_D^2}} \quad (46)$$

$$C_S = C_{eq} \frac{\Delta\phi_D \cosh(\frac{L}{\lambda}) - \Delta\phi_S}{\sinh(\frac{L}{\lambda})\sqrt{2\Delta\phi_S \Delta\phi_D \cosh(\frac{L}{\lambda}) - \Delta\phi_S^2 - \Delta\phi_D^2}} \quad (47)$$

In order to revoke this capacitive coupling above the threshold, we multiply $C_{S(D)}$ by a screening function; we obtain the threshold voltage shift as follows:

$$\Delta V_{th} = \frac{C_S^* \Delta\phi_S^* + C_D^* \phi_D^*}{C_{eq} V_T} \quad (48)$$

with:

$$C_{S(D)}^* = C_{S(D)} \frac{2\exp(-\frac{Q_{mob}(0)}{\gamma Q_{fix}})}{1+\exp(-\frac{Q_{mob}(0)}{\gamma Q_{fix}})} \quad (49)$$

Q_{mob} was obtained from Equations (13) and (19). The parameter γ adjusts the smoothness of the transition ($\gamma = 3.33$). So, the DIBL effect can be brought to the core model by substituting the v parameter in Equations (13), (15) and (16) with V_{dibl} [22]:

$$V_{dibl} = \upsilon + \frac{C_S^* \Delta\phi_S^* + C_D^* \phi_D^*}{C_{eq} V_T} \quad (50)$$

Moreover, we used the following smoothing function

$$\Delta\phi_{S(D)}^* = V_T \ln(1+\exp(\frac{\Delta\phi_{S(D)}}{V_T})) \quad (51)$$

so that $\Delta\phi_{S(D)}^*$ does not become negative and takes 0 V above the threshold.

The series resistance R_S is one of the parameters that affects the RF/Analog performance severely. This parameter can be different in JL and inversion mode devices; it is caused by the dissimilarity in the S/D doping concentration and the absence of junctions in the GAAJ MOSFET.

In this study, we investigate a decrease in saturation drain current caused by the series resistance in GAAJ MOSFET. In this context, to enhance the model accuracy and have an insight into the physical meaning of this effect, series resistance effect can be introduced in the drain current expression I_{ds0} [24, 29]:

$$I_{ds} = \frac{I_{ds0}}{1+2\pi\frac{R}{L}\mu_{eff} R_s (Q_{mob}(0) - n(Q_{mob}(0) - Q_{mob}(V_{deff}))} \quad (52)$$

with I_{ds0} is given by Equation (19). n is a fitting parameter. Q_{mob} (0) and Q_{mob} (V_{deff}) mean the long channel mobile charges at the S/D sides (pinch-off points) of the channel.

III. RESULTS AND DISCUSSIONS

In order to validate the suggested models, SILVACO [21] is used to perform the corresponding simulations. To offer RF/Analog designers, some flexibility in the choice of their circuit and device topologies and achieve high performances, it is necessary to investigate the scaling capability and the device immunity behavior under SCEs and to show how the device degradation can be suppressed using highly doped S/D extensions.

A. *DC characteristics*

The analytical characteristics *I*(*V*) of the proposed and the conventional devices are depicted in Figures 2, 3 and 4. The conventional device with homogeneous channel doping profile (1×10^{19} cm^{-3}) necessitates gate work-function with high value ($\phi_m = 5.6\,eV$) for channel depletion. However, this work-function value is not easy to obtain [30]. In contrast, the proposed GAAJ MOSFET requires a lower value ($\phi_m = 4.95\,eV$).

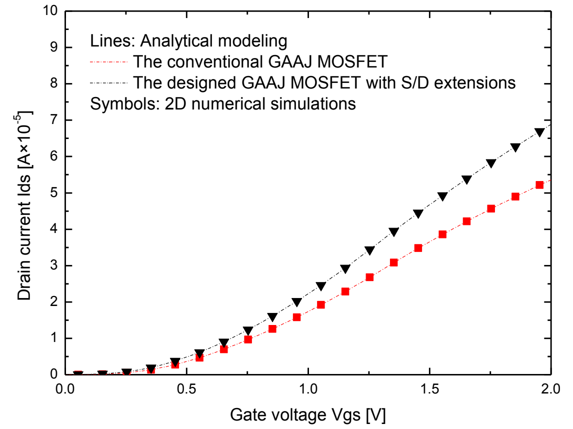

Figure 2: Transfer characteristics $I_{ds}(V_{gs})$ in linear scales $V_{ds} = 1V$, $N_d = 10^{19}$, $N_{dext} = 5.10^{19}$, $T_{ox} = 2nm$, $L = 30nm$, $R = 7.5nm$, $\phi_m = 5.27$.

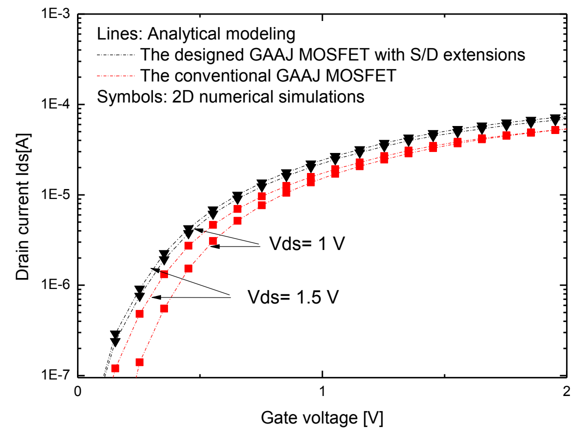

Figure 3: Transfer characteristics $I_{ds}(V_{gs})$ in logarithmic scales $V_{ds} = (1V, 1.5V)$, $N_d = 10^{19}$, $N_{dext} = 5.10^{19}$, $T_{ox} = 2nm$, $L = 30nm$, $R = 7.5nm$, $\phi_m = 5.27$.

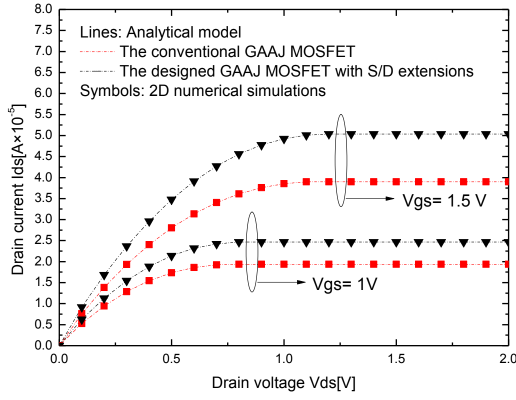

Figure 4: Variation of the drain current as a function of the drain voltage, $V_{gs} = (1V, 1.5V)$, $N_d = 10^{19}$, $N_{dext} = 5.10^{19}$, $T_{ox} = 2nm$, $L = 30nm$, $R = 7.5nm$, $\phi_m = 5.27$.

As expected, from Figures 2, 3 and 4, by introducing the high doped extended S/D regions, the drain current is enhanced for the designed device in comparison to the conventional one. The cause of the decrease for the conventional GAAJ MOSFET is principally due to the carrier mobility degradation and the series resistance effect. It is obvious that the designed device, in comparison with the conventional one, has superior current above the threshold voltage. The reason for the improvement in current beyond the threshold is mainly due to the high immunity of the proposed GAAJ MOSFET including high doped extended S/D regions against the combined effects of velocity saturation and series resistances. This amelioration is essentially caused by the increase of the channel potential barrier.

In order to inspect the scaling capability of the designed device under the influence of SCEs, Figure 5 shows the variation of the ON-current as a function of the channel radius for both designed and conventional GAAJ MOSFETs. As evident from Figure 5, an enhancement in ON-current in the designed GAAJ MOSFET is obvious, where the ON-current has a fast monotone rising tendency for GAAJ MOSFET including high doped extensions compared to the conventional device.

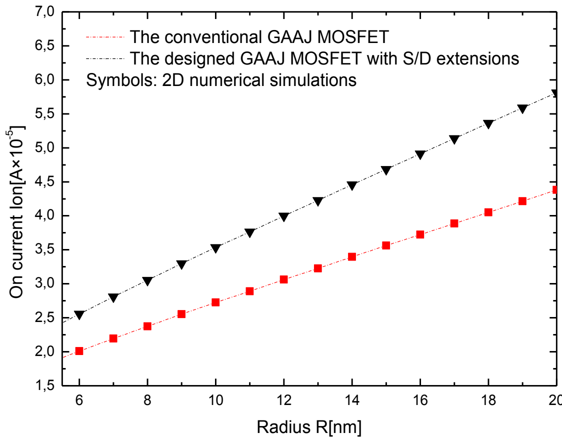

Figure 5: Variation of the ON-current as a function of the channel radius (R), $V_{ds} = 1V$, $V_{gs} = 1V$, $N_d = 10^{19}$, $N_{dext} = 5.10^{19}$, $T_{ox} = 2nm$, $L = 30nm$, $\phi_m = 5.27$.

This significant improvement is due mainly to the reduction of the SCEs giving, thus, best immunity to the device. This investigation makes the proposed GAAJ MOSFET with a highly doped extensions suitable candidate for digital applications. In order to inspect the scaling capability of the designed device under the influence of SCEs, Figure 5 shows the ON-current versus the channel radius for both designed and conventional devices. An ON-current enhancement in the designed device is obvious where it has a steep slope compared to the conventional device one. This significant improvement is caused mainly by the reduction of the SCEs. This fact proves that the device has better immunity. In this context, the proposed GAAJ MOSFET with highly doped extensions can be considered as an appropriate device for RF/Analog applications.

B. *Analog performance*

This section focuses on analog figures of merit in terms of transconductance. This parameter is expressed as follows

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \tag{53}$$

The transconductance is a fundamental figure of merit. The more transconductance is high, the more is cut-off frequency. It is obvious from Figure 6 that the conventional GAAJ MOSFET has faintly lower g_m than that of the designed GAAJ MOSFET; it is mainly due to the mobility degradation caused by the saturation velocity and the high S/D resistances effects. The situation gets worse with increasing the drain voltage. In our opinion, this result emphasizes the potency of the proposed design. This fact is clarified by the improved electrostatic control provided by the proposed device.

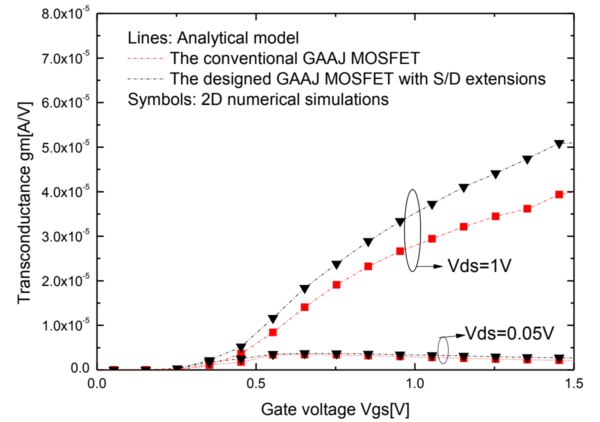

Figure 6: Variation of transconductance g_m as a function of the gate voltage, $V_{ds} = (0.05V, 1.5V)$, $N_d = 10^{19}$, $N_{dext} = 5.10^{19}$, $L = 30nm$, $R = 7.5nm$, $\phi_m = 5.27$.

A further significant parameter is the Transconductance Generation Factor (TGF). TGF is defined as:

$$TGF = \frac{g_m}{I_d} \tag{54}$$

From Figure 7, for a set of channel radius values, the model expected TGF characteristics are compared with the numerical TCAD simulation results. The comparison makes

obvious the accuracy of the proposed model. In addition, the proposed structure provides conspicuous TGF values when compared to the classical device. However, it is worth mentioning that as channel radius R increases, SCEs governs and TGF decreases significantly.

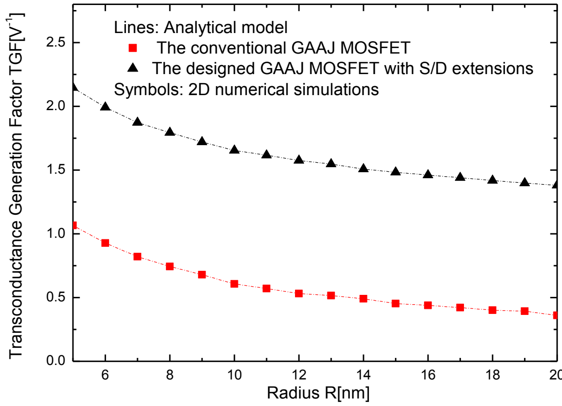

Figure 7: TGF versus channel radius (R) for: $V_{ds}=1V$, $V_{gs}=1V$, $N_d=10^{19}$, $N_{dext}=5.10^{19}$, $T_{ox}=2nm$, $L=30nm$, $\phi_m=5.27$.

Assuming that an output conductance load of r=105 Ω affects each of the conventional and the proposed devices, the intrinsic gain voltage can be expressed as:

$$A_V = rg_m \tag{55}$$

This gain constitutes a useful parameter to quantify the device performances. From Figure 8, the proposed device exhibits an apparent improvement in this figure of merit in contrast to the conventional one for a large set of channel radius values under SCEs. This betterment shows the efficacy of our designed device in decreasing the SCEs.

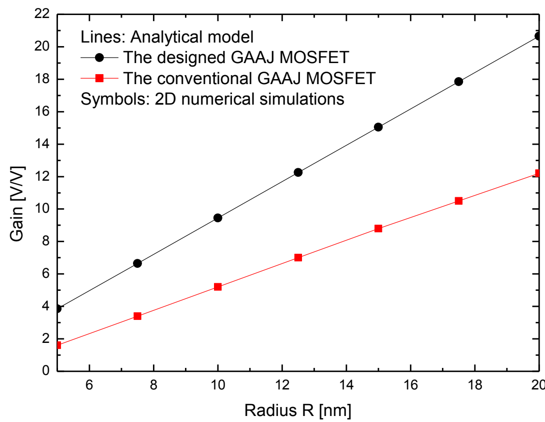

Figure 8: Variation of gain as a function of the channel radius, for load resistance $r=10^5\,\Omega$, $V_{ds}=1V$, $V_{gs}=1V$, $N_d=10^{19}$, $N_{dext}=5.10^{19}$, $T_{ox}=2nm$, $L=30nm$, $\phi_m=5.27$.

C. RF performance

Higher performance, lower cost, and greater functionality for ultra-low power circuit applications present a new challenge because of the meticulous downscaling in CMOS technology.

In the subsequent development, in order to assess the RF performances, analytical expressions are exploited and analysed. The more the cut-off frequency f_c is high, the more performances (in terms of rise time and bandwidth) are better. Figure 9 depicts f_c versus the biasing voltage V_{gs} for both conventional and proposed devices. f_c can be computed as:

$$f_c = \frac{g_m}{2\pi \times C_{OX}} \tag{56}$$

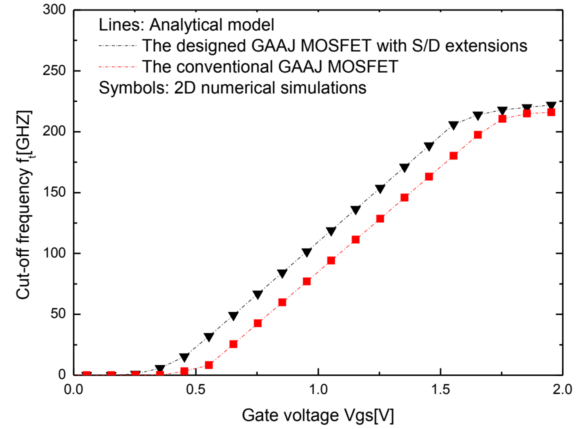

Figure 9: Variation of the cut-off frequency f_c as function of the gate voltage $V_{ds}=1V$, $N_d=10^{19}$, $N_{dext}=5.10^{19}$, $T_{ox}=2nm$, $L=30nm$, $R=7.5nm$, $\phi_m=5.27$.

Figure 9 shows that the discordance of curves related to both devices is noteworthy exclusively at the interval of 0.5V-1.6V. In the above-mentioned range, the designed GAAJ MOSFET including S/D extensions surpasses the conventional device. It is worthwhile to state that both TCAD simulation results and our analytical model are in great matching.

D. Optimization of GAAJ MOSFET performance

Due to the complex behavior of the GAAJ MOSFET including S/D extensions, it seems typical to exploit a metaheuristic-based approach to search the combination that leads to the highest GAAJ MOSFET RF/Analog performances.

Genetic algorithms are a vigorous and flexible approach that can be useful for a broadband range of knowledge and optimization problems [31-34]. They are mainly appropriate to problems where customary optimization methods break down when the search becomes computationally obdurate. Moreover, GAs provide a particular strength with a huge quantity of information and allow some latitude in the choice of the suitable solution. No metaheuristic paradigms have been proposed to ameliorate the immunity behavior of the GAAJ MOSFET against SCEs; therefore, the purpose of this section is to investigate intensively the impact of the high doped extended S/D regions, and formulate novel design criteria with two consistent objectives (f_c, I_{dmax}) to improve the immunity behavior of the proposed design against the SCEs.

This investigation aims to find optimal design parameters for the proposed device. The optimization framework based on GA approach necessitates the statement of objective

functions; therefore, the optimization of the device under study will take into account the following criteria:

- Maximization of the derived drain current $I_{dmax}(X)$.
- Maximization of the cut-off frequency $f_c(X)$.

X is a vector containing the parameters to optimize:

$$X = (R,\ L,\ L_{ext},\ T_{ox},\ N_d,\ N_{dext}, V_{gs},\ V_{ds},\ \phi_m).$$

The constraint is: $g_1(x): x \in [x_{i\min}, x_{i\max}],\ x_i \in X$ (each design parameter should be limited within a particular range).

- $g_2(x): R$ >5nm (to avoid quantum effects)
- $g_3(x): N_d > 10^{18}$ cm^{-3}

For the implementation of our metaheuristic approach based on genetic algorithms, individuals are evaluated using the computation of the objective function. To evolve during consecutive generations, our parameters values used for the genetic algorithm are summarized in Table 1. The best fitness function value achieved during a succession of evolving generations corresponds to the optimal combination that provides the highest GAAJ MOSFET RF/Analog performances.

Table 1
GA parameters setting for classical and designed structures.

GA Parameter	Value
Number of variables	9
Population size	50
Maximum number of generations	1000
Selection	Tournament
Crossover	Constraint dependent
Mutation	Scattered
Crossover fraction	0.8

In the following, based on weighted sum approach method, the two considered objective functions are incorporated in a mono-objective function:

$$F(X) = w_1 f_c + w_2 I_d \tag{57}$$

Weights setting with the no articulating preferences w_i (i = 1, 2) can be given as 0.5. The final optimized GAAJ MOSFET parameters, including the impact of the S/D extensions, are summarized in Table 2.

Based on the optimized design parameters shown in Table 2, a GAAJ including highly doped S/D extensions has been designed. I_{ds}–V_{gs} curves of the proposed and conventional devices are plotted.

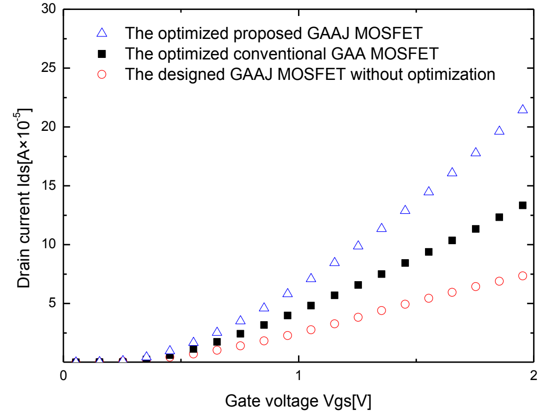

Figure 10: Curves of the proposed design, with and without optimization compared to the optimized conventional GAAJ MOSFET design.

From Figure 10, it is clearly demonstrated that our optimized GAAJ MOSFET including S/D extension yields 46.7 % and 54.8 % improvement in $I_{d\max}$ and cut-off frequency, respectively, in comparison with the conventional device; this is due to the immunity of the proposed device against the SCEs via the highly doped regions. It is obvious from Figure 10 that the hybrid methodology combining both S/D extensions engineering and GA-based approach optimization appears as an attractive strategy to suppress the impact of the short channel effects which dramatically decrease the drain current. Results show that the drain current increases until it attains a maximum around 36%. Device parameters are required to be equal to: $R = 28\,nm$, $N_{dext} = 9.5\times10^{19}\,cm^{-3}$, $L_{ext} = 8.6\,nm$, $\phi_m = 4.6\,eV$. It is to note that this metal work-function value can be concretized by using chromium as gate material instead of polysilicon. Hence, the use of chromium as a gate material allows the designer to avoid the unwanted polysilicon depletion width and dopant penetration effects [35].

Table 2
Performance comparison between our GAAJ devices and optimized conventional device.

Design parameters	Proposed design without optimization	Conventional design with optimization	Proposed design with optimization
S/D extensions design parameters:			
N_{dext} [cm^{-3}]	5×10^{19}	/	9.5×10^{19}
L_{ext} [nm]	10	/	8.6
GAAJ MOSFET design parameters			
Radius R [nm]	7.5	30	28
Channel length L[nm]	10	10	20
Oxide thickness T_{ox} [nm]	2	2	2
Gate voltage V_{gs} [V]	2	2	2
Drain voltage V_{ds} [V]	1	4	1.5
Metal work function ϕ_m [eV]	5.27(polysilicon)	4.6(Chromium)	4.6(Chromium)
Channel doping concentration N_d[cm^{-3}]	1×10^{19}	1×10^{19}	1×10^{18}
Objective function			
Cut-off frequency f_c[GHz]	150	357	790
Drived drain current I_{dmax}[A]	2.5×10^{-5}	6.3×10^{-5}	11.8×10^{-5}

IV. CONCLUSION

In this paper, a new design methodology using both comprehensive analytical modeling and metaheuristic-based optimization was suggested. The impact of S/D extensions on the RF/Analog performances is investigated.

In addition, the suggested strategy allows the investigation of the GAAJ MOSFET immunity behavior under SCEs. In contrast to the conventional device, the RF/Analog improvement occurred in the proposed design is caused by the ability to decrease SCEs. The developed analytical model accuracy is validated by TCAD numerical simulation results. In order to push further the designed short channel GAAJ MOSFET, a GA-based approach using developed analytical formulations was proposed to deal with parameters optimization and to enhance the RF/Analog performances. In this context, the cut-off frequency and saturation current improvements are, respectively, about 120% and 87% in comparison to the conventional design with optimization. The obtained results prove that the suggested strategy is a practical tool to design high-performance junctionless MOSFETs.

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