# Design and Analysis of 2oo3 Static Voter for SMT function in an Adjustable Speed Electrical Power Drive System

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***Abstract*— In fail-safe systems, a 2-out-of-3 voter is responsible for processing the monitoring of failures of the sensor unit in the system. When a failure has occurred and the outputs directly drive the vital units, there may be some injuries, loss or damages, such as in a nuclear reactor shutdown, railway signalling systems, industrial compression systems, or electric motor drive systems. This paper presents an innovatively designed and developed 2-out-of-3 static voter that detects the signal with a window comparator circuit related to the safety system for the detection of false signals. The voting function is mainly one diode and four optoelectronic switches, which reduces the number of devices, resulting in a lower failure rate. Failure of the voter is detected and corrected by the window comparator with digital switching levels, which is a very simple circuit that is used with low voltage and fast varying input. Furthermore, the analysis of the performance was conducted for IEC 61800-5-2 in an adjustable speed electrical power drive system, with the simulation of the failure rate of electronic equipment, mean time to failure, failure mode and effects analysis (FMEA), and the experimental circuit.**

***Index Terms*— 2-out-of-3; Fail-Safe; FMEA; Static Voter.**

## I. INTRODUCTION

During the processing of fail-safe systems, such as railway signalling systems, nuclear reactor shutdowns, industrial compression systems, and electric motor drive systems, when a failure happens, there will likely be some injuries, loss or damage. Thus, these systems demand high detection of accuracy and thus require 2-out-of-3 (2oo3) processing, or Triple Module Redundancy (TMR), that detects the error of the 2 out of 3 detectors that shuts down the systems. From the previous research, the 2-out-of-3 voter has been studied and applied in critical security tasks such as the application of transistor circuits for the shutdown of a nuclear reactor, in which the major factor responsible for the design was the use of transistor trip circuit [1]. In the application of the triplicated majority voting to integrated circuits [2], a hardware voter can be implemented with logic gates as two-level AND-OR in CMOS VLSI technology [3-5]. Triple-Modular Redundancy is the simplest and most effective fault tolerant design method for ICs, in which the systems can multiply in series [5-6]. The 2oo3 architecture can be used in fault diagnosis on the basis of vital computer systems [7]. This article summarises the major methods to control the effects of single random faults: composite fail-safe, reactive fail-safe, and inherent fail-safe. The detection of faults is one of the key factors during fail-safe design to avoid the effects of single faults [8]. In paper [9], two novel voting circuits, a dynamic voter and a static voter, with reliability and safety that satisfy the EN 50129 standards are proposed.

A window comparator is a safety circuit that checks the DC signal level from the input with voltage hysteresis properties that has an upper limit and a lower limit, in which the level is between both limits. The design uses a transistor that is based on AND logic [10-13], which is an application used in fail-safe information processing. The circuit prevents faulty signals from various problems and detects the voltage level, in which only the voltage inside the window will operate. Moreover, a window comparator with op-amp or module ICs is comprised of two separate comparators and the AND gate, which features two different threshold inputs, an upper threshold and a lower threshold [14]. The output is "high", and the input signal is between the upper and the lower threshold voltage, which is "low" in contrast. The paper [15] proposed the technique of logic gates with input hysteresis for a Schmitt trigger circuit for the window comparator, which used eight transistors for construction and is very compact. In paper [16], a window comparator circuit with an XOR gate and potential divider circuit, which can be used in low voltage and fast varying input, was proposed. In paper [17], a window comparator circuit with digital ICs, which used the properties of the threshold voltage characteristics, was presented. For the analysis of the performance results for a 2-out-of-3 voter, there are two preferred approaches. Markov's method is IEC 61165, which uses sequences of random variables in the future, which are determined by the present variable. The other method is the IEC 60812 [18] failure mode and effects analysis (FMEA), which is a procedure for the analysis of a system that is used to identify the potential failure modes as well as their causes and effects on system performance.

This paper proposes the design and implementation of a 2-out-of-3 static voter with a digital window comparator for an adjustable speed electrical power drive system and analysis of its performance with the simulation of the failure rate of electronic equipment, mean time to failure, failure mode and effects analysis (FMEA), and the experimental circuit.

## II. CONCEPTS AND DESIGN

### *A. The adjustable speed electrical power drive system*

This research was applied to an adjustable speed electrical power drive system suitable for use in safety-

related applications described in this research and includes the safe motor temperature (SMT) safety function [19]. Three PTC sensors are attached to the motor windings in each phase triggered by three redundancy feedback signals through an electronic processing and the 2oo3 voter. The fail-safe relay drive based on the ISO 13849-2 [20] was required. Also, this system required safety integrity level 3 (SIL3) [21-22], in which the SMT safety function prevents the motor temperature from exceeding a specified upper limit, as shown in Figure 1.

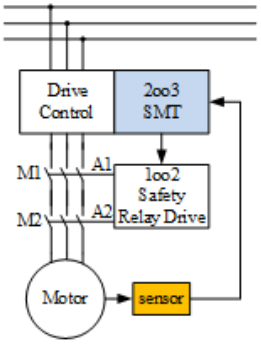


Figure 1: The adjustable speed electrical power drive system

In this paper, the SMT safety function is implemented with the 2-out-of-3 voter to achieve the hardware fault tolerance. This consists of three main parts: three electronic processing circuits, the 2oo3 voter and the window comparator circuit, as shown in Figure 2.

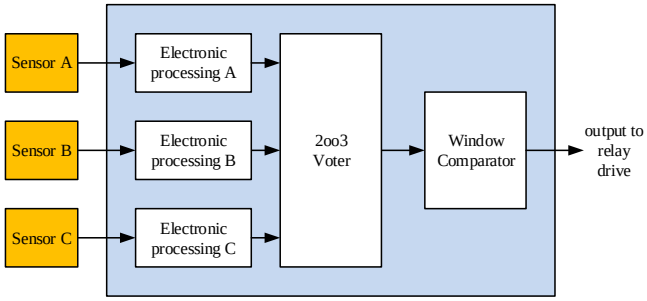


Figure 2: The SMT function implemented with the 2-out-of-3 voter

### B. *The 2oo3 voting logic design*

The 2oo3 voting logic design comprises three AND logics and OR logics based on Equation 1. For detecting the error of 2 out of 3 detectors, the voter consists of six switches and the system shutdown, following the logic equations.

$$OUT = AB + BC + CA \quad (1)$$

The likelihood of errors and failures increases as more components are used. Therefore, reducing the number of devices will result in decreased errors and failures. Therefore, in order to improve the reliability of the voting circuit, the criteria for voting should be simplified, as shown in Equation 2.

$$OUT = AB + C(A + B) \quad (2)$$

In Equation 2, the voter consists of two AND logics and one OR logic, which is fewer logics than those in (1), so there are few components and simpler circuits. The voter can be designed, as shown in Figure 3.

The proposed voter consists of one diode and four switches to carry out the logic operation function. In this design, the AND logic is achieved by cascade, and the OR logic is designed by connecting the two networks in parallel connected diodes. The logic is controlled by the states of the switches.

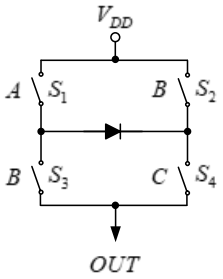


Figure 3: The 2oo3 voting logic design comprises two AND logics and one OR logic

The condition of 2oo3 for error detection of 2 out of 3 detectors is shown in Figure 4. The $S_1$, $S_2$, $S_3$ and $S_4$ are controlled by the electronic processing circuits A, B and C. In the case of only the A or B or C process, the output signal is not generated. In the case of the AB or AC or BC process, the output signal is generated. These cases are as follows: AB $V_{DD}$ through $S_1$ and $S_3$, AC $V_{DD}$ through S1 and S4, and BC $V_{DD}$ through $S_2$ and $S_4$, respectively. The $V_{DD}$ can be delivered through all switches to OUT in the case that all input signals are correct and the voting result is accurate.

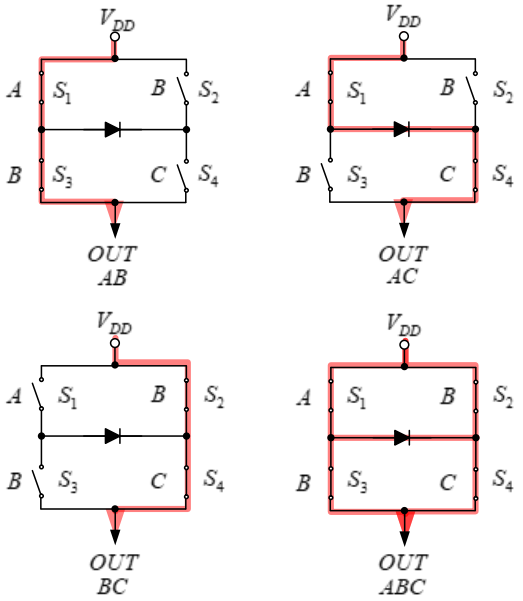


Figure 4: The condition of 2-out-of-3 voter to generate the output signal

### C. *The window comparator circuit with digital switching levels*

The window comparator circuit with digital switching levels uses differential threshold voltages. The input value is in the range between the threshold levels; therefore, the output logic is “1”. If the input voltage is higher or lower than the range, the output logic is “0”. The proposed circuit consists of a Schmitt trigger inverter and the AND gate as shown in Figure 5.

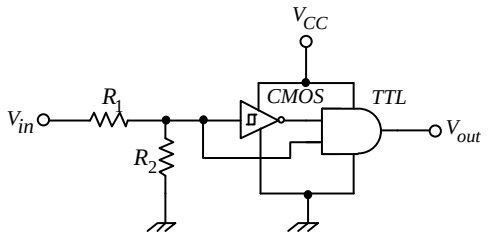


Figure 5: The window comparator circuit with digital switching levels

If the input logic is "0" or "1", it can make the output logic "0" only and cannot generate the signal logic "1" under such conditions. If the input logic "1" through the inverter is logic "0", the AND gate will receive a signal that both legs are "0" and "1", respectively, and the $V_{out}$ is logic "0". If the input logic "0" through the inverter is logic "1", the AND gate receives a signal that both legs are logics "1" and "0", respectively, and the $V_{out}$ is logic "0".

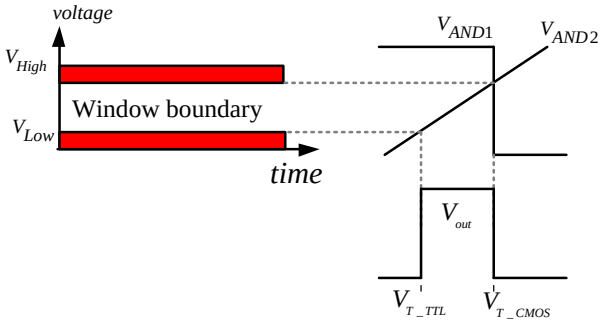


Figure 6: The voltage waveforms and window boundary

The CMOS Schmitt trigger inverter and TTL AND gate have different switch levels, and the circuit has a window boundary between both threshold voltages, The threshold voltages in fact operate when CMOS is $0.5V_{CC}$ and TTL is 1.5V. The window boundary can be defined by Equation 3 and the voltage waveforms are shown in Figure 6.

$$V_{T\_TTL} < V_{in} < V_{T\_CMOS} \quad (3)$$

In the application, the voltage level can be expanded by using the voltage divider, which has the voltage range as shown in Equation 4.

$$V_{T\_TTL}\left(\frac{R_1 + R_2}{R_2}\right) < V_{in} < V_{T\_CMOS}\left(\frac{R_1 + R_2}{R_2}\right) \quad (4)$$

### *D. The 2-out-of-3 static voter with digital window comparator for safe motor temperature function of an adjustable speed electrical power drive system*

From the above mentioned, we can design the 2-out-of-3 static voter with a digital window comparator circuit for a safe motor temperature function by dividing the design into three parts. The electronic processing uses the comparator to compare the voltage rating given to the voltage, which varies with the PTC resistance. The 2oo3 voter in the application uses an Opto-coupler switch to reduce the problem of mechanical switches and facilitate easy calculation of reliability values. Signal detection failure of the voter guessing by the window comparator circuit guessing that application, the resistance of the transistor represents the resistance $R_1$. By setting the 5V supply voltage to the voltage level of the Schmitt trigger inverter input at 1.8V, the resistance $R_1$ is 150 ohms. The 2-out-of-3 static voter with digital window comparator for safe motor temperature function of adjustable speed electrical power drive system is shown in Figure 7.

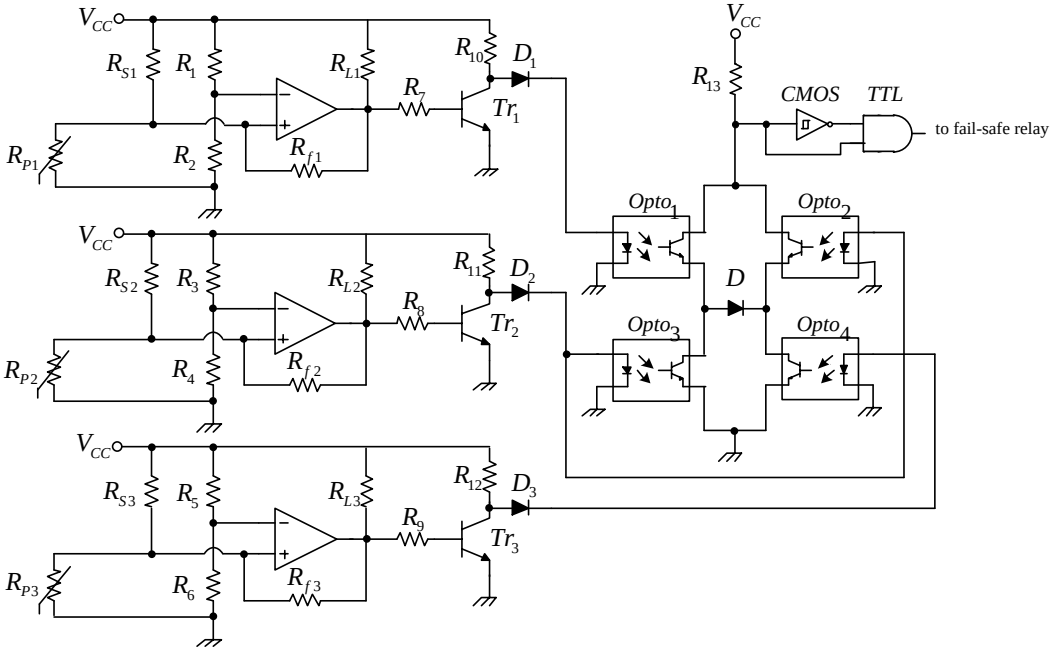


Figure 7: The 2-out-of-3 static voter with digital window comparator for safe motor temperature function in an adjustable speed electrical power drive system.

## III. RESULTS AND DISCUSSION

The performance analysis for IEC 61800-5-2 of the adjustable speed electrical power drive system was conducted with the simulation of the failure rate of electronic equipment, mean time to failure, failure mode and effects analysis (FMEA) and the experimental circuit.

This system consists of individual components, thus to attempt to derive the failure characteristics of the system from the characteristics of the components and the system structure, a model of computation and model verification are required. The models are based on inspection of the system and on assumptions about system behaviour.

For the difference of how the design compares to the original method regarding calculated failure rate value, this paper focuses on comparison of an older voter and the new 2oo3 voter. The finding of a failure rate of electronic equipment can use the Military Handbook "Reliability Prediction of Electronic Equipment" (MIL-HDBK-217F) [23], as shown in Table 1.

Table 1
The Failures of Electronic Equipment

| No | Notation | Components | Failure rate ($10^{-6}$h) |
|---|---|---|---|
| 1 | $\lambda_P$ | Opto-coupler | 0.08160 |
| 2 | $\lambda_D$ | Diode | 0.01213056 |

The number and type of equipment affects the failure rate. The old 2oo3 voter used six opto-couplers, the new 2oo3 voter used four opto-couplers and one diode. The failure rate of the 2oo3 voter device can be calculated by the sum of the failure rate, as shown in Equation 5 and 6:

$$\lambda_{old\_2oo3} = 0.4896 \times 10^{-6}\ hr \quad (5)$$

$$\lambda_{new\_2oo3} = 0.3385 \times 10^{-6}\ hr \quad (6)$$

The overall failure rate, as shown in Equation 7 and 8, shows that the decrease in the number of devices results in a lower failure rate. The mean time to failure [24] is the approximation of reliability at a time or inverse of failure rate, as shown in Equation 7 and 8:

$$MTTF_{old\_2oo3} = 2{,}042{,}483\ hr = 233.16y \quad (7)$$

$$MTTF_{new\_2oo3} = 2{,}953{,}947\ hr = 337.2y \quad (8)$$

The MTTF is an inverse of the failure rate, so that when the failure rate is lower, the average time to failure will increase. The proposed method has a reliability value that is 1.446 times that of the original model.

Failure of semiconductor devices [25] in storage or dormant operations is a result of latent manufacturing defects that have not been detected during the semiconductor device screening tests. Failure is a result of manufacturing defects such as wire connections, contamination, contact material, loss of compression or slipping, resulting in an open circuit. Interpretation of failure data by the Reliability Analysis Center (RAC) includes the failure of the following failure modes: General purpose diode short, 49%, open 36%, parameter change 15%, Optoelectronic sensor short 50%, and open 50%.

The international standard IEC 60812 [18] (Analysis techniques for system reliability – Procedure for failure mode and effects analysis, or FMEA) is a systematic procedure for the analysis of a system to identify the potential failure modes, their causes, and their effects on system performance. Regarding the adjustable speed electrical power drive systems that the FMEA accepted by IEC 61800-5-2 [19], the simulation tests should be carried out to determine the worst case. The express fault models, fault exclusions and rationale in this paper are based on IEC 61800-5-2 Annex D (Fault lists and fault exclusions).

The IEC 61800-5-2 Annex D.12-Discrete semiconductors used two faults considered as an open-circuit of any connection and as a short-circuit between any two connections. The IEC 61800-5-2 Annex D.13-Optocouplers used three faults considered as an open-circuit of an individual connection, and as a short-circuit between any two input connections and a short-circuit between any two output connections. This test used a computer simulation program and the experimental circuit is as shown in Table 2 and 3.

As shown in Table 2, the results of the single failure test of the proposed circuit according to the aforementioned standard indicate that no fail-dangerous occurred. Table 3 provides the results of the double failure test, which show that no fail-dangerous occurred.

In Table 2 and 3, it can be seen that the output of the circuit must pass through a window comparator circuit, which will detect the voltage level in the range of 1.3 - 2.5 v. Failure in any voter, if it is a short circuit, indicates that the voltage at the input side of the windows comparator circuit is lower than 1.3 v. If the open circuit failure of the window comparator is higher than 2.5 v, then no serious consequences occurred. Any of the voter failures will not affect the output of the window comparator.

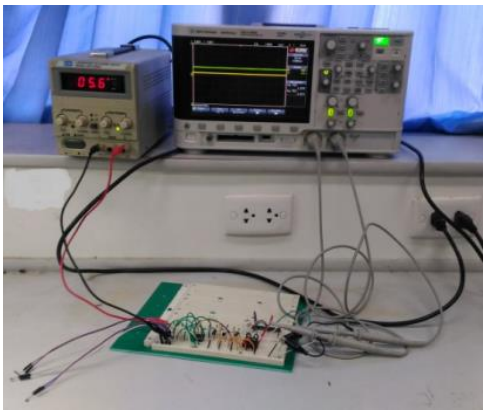

Figure 8: The experimental circuit

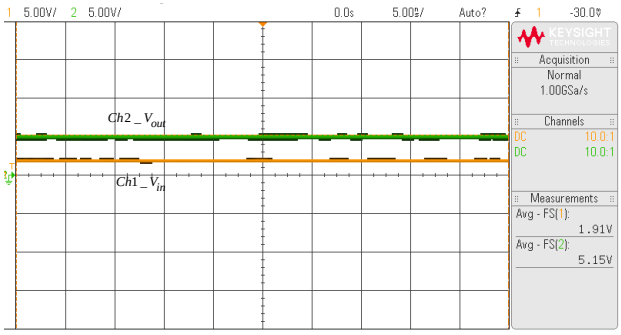


Figure 9: The signal measurements of the windows comparator circuit under normal conditions

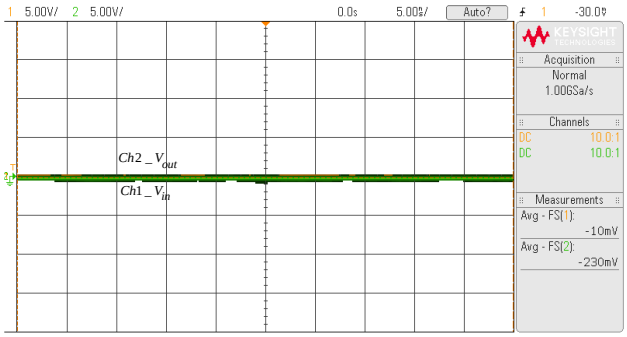


Figure 10: The signal measurements of the windows comparator circuit under fail conditions

Table 2
FMEA of Single Failures in the 2oo3 Voter Circuit

| Devices | Failure mode | Effect of failure | Potential effects |
|---|---|---|---|
| $Opto_1$ | Open-circuit | The voter changed to 2oo2 | Δ |
| | Short-circuit between input connections | The voter changed to 2oo2 | Δ |
| | Short-circuit between output connections | OUT = B + C | Δ |
| $Opto_2$ | Open-circuit | The voter changed to 2oo2 | Δ |
| | Short-circuit between input connections | The voter changed to 2oo2 | Δ |
| | Short-circuit between output connections | OUT = C + AB + AC | Δ |
| $Opto_3$ | Open-circuit | The voter changed to 2oo2 | Δ |
| | Short-circuit between input connections | The voter changed to 2oo2 | Δ |
| | Short-circuit between output connections | OUT = A + AC + BC | Δ |
| $Opto_4$ | Open-circuit | The voter changed to 2oo2 | Δ |
| | Short-circuit between input connections | The voter changed to 2oo2 | Δ |
| | Short-circuit between output connections | OUT = B + A | Δ |
| D | Open-circuit | The voter changed to 2oo2 | Δ |
| | Short-circuit | OUT = B + AC | Δ |

Remark: Δ: no significant consequences ▲: abnormal condition

Table 3
FMEA of Double Failures in the 2oo3 Voter Circuit

| Devices | | $Opto_1$ | | | $Opto_2$ | | | $Opto_3$ | | | $Opto_4$ | | | D | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Failure mode | Open-circuit | Short-input | Short-output | Open-circuit | Short-input | Short-output | Open-circuit | Short-input | Short-output | Open-circuit | Short-input | Short-output | Open-circuit | Short-circuit |
| $Opto_1$ | Open-circuit | | | | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y |
| | Short-circuit input | | | | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y |
| | Short-circuit output | | | | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y |
| $Opto_2$ | Open-circuit | Y | Y | Y | | | | Y | Y | Y | Y | Y | Y | Y | Y |
| | Short-circuit input | Y | Y | Y | | | | Y | Y | Y | Y | Y | Y | Y | Y |
| | Short-circuit output | Y | Y | Y | | | | Y | Y | Y | Y | Y | Y | Y | Y |
| $Opto_3$ | Open-circuit | Y | Y | Y | Y | Y | Y | | | | Y | Y | Y | Y | Y |
| | Short-circuit input | Y | Y | Y | Y | Y | Y | | | | Y | Y | Y | Y | Y |
| | Short-circuit output | Y | Y | Y | Y | Y | Y | | | | | Y | Y | Y | Y |
| $Opto_4$ | Open-circuit | Y | Y | Y | Y | Y | Y | Y | Y | Y | | | | Y | Y |
| | Short-circuit input | Y | Y | Y | Y | Y | Y | Y | Y | Y | | | | Y | Y |
| | Short-circuit output | Y | Y | Y | Y | Y | Y | Y | Y | Y | | | | Y | Y |
| D | Open-circuit | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | | |
| | Short-circuit | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y | | |

Remark: Y = Output $V_{DD}$ absent (fail-safe), N = Output $V_{DD}$ present (fail-dangerous)

A fail-safe window comparator was proposed as shown in Figure 5, and its design concept is based on an AND logic circuit dependent on the digital switching levels, which are determined by the values of resistances and input voltages of each AND input. When AND inputs are within the predefined voltage width, the output of the AND gate is provided as the output of the fail-safe window comparator. This digital fail-safe window comparator can be applied to 2oo3 static voters in the safe motor temperature function, with testing of circuits by simulation in various failure modes as shown in Figure 8. Figure 9 shows the signal measurements of the input and output sides of the windows

comparator circuit under normal conditions. In Figure 10, signal measurements of the input and output sides of the windows comparator circuit under fail conditions can be seen.

## IV. CONCLUSION

This paper presents a new 2-out-of-3 static voter with a digital window comparator for an adjustable speed electrical power drive system suitable for use in safety-related applications described in this paper, which includes the safe motor temperature safety function. The new voter circuit has fewer components and is more reliable than the original voter. Furthermore, the reliability results of the proposed voter show that its MTTF is approximately 337 years, which is a reliability value 1.446 times that of the original model. Furthermore, the analysis of its performance with failure mode and effects analysis (FMEA), showed that in the single failure test of the proposed circuit according to the IEC 16800-5-2 standards, no fail-dangerous occurred. In the double failure tests, it was also seen that no fail-dangerous occurred. When the motor temperature is higher than the predetermined temperature and no parts of the electronic processing circuit malfunction, the output signals with the window comparator are provided to the filter and a DC signal is eventually output as the 2oo3 temperature detection results in a fail-safe manner.

## ACKNOWLEDGMENTS

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