Bandwidth Enhancement Technique with Low Group Delay Variation CMOS Power Amplifier for UWB System

Rohana Sapawi[1], Siti Kudnie Sahari[1], Dayang Nur Salmi Dharmiza Awang Salleh[1], Dayang Azra Awang Mat[1] and Sohiful Anuar Zainol Murad[2]

[1]*Department of Electrical and Electronic Engineering, Faculty of Engineering, Universiti Malaysia Sarawak, 94300 Kota Samarahan, Sarawak, Malaysia.*

[2]*School of Microelectronic Engineering, Universiti Malaysia Perlis (UniMAP), Malaysia.*

srohana@unimas.my

***Abstract*—This paper introduced a bandwidth enhancement technique for ultra-wideband (UWB) transmitter design with low group delay variation for CMOS power amplifier (PA). Three stages of cascade common source topology are implemented to provide high gain with good gain flatness. Shunt peaking inductor is introduced at every stage of the introduced PA to improve the bandwidth and to achieve low group delay variation simultaneously. A resistive shunt feedback method is implemented at the first stage to acquire good input matching. The first and second stages attain gain at lower corner and upper-end frequency respectively, whilst the third stage smoothed the gain flatness curve. In addition, the theoretical analysis of group delay is investigated to determine the important design factor for low group delay variation in 3.1 to 10.6 GHz CMOS PA for UWB transmitters. The outcome of the research shows that a gain about 11.48 ± 0.6 dB at average, S11 less than -10 dB, and S22 less than -14 dB is achieved. Moreover, excellent group delay variation is acquired throughout the entire band, measuring about ±85.8 ps.**

***Index Terms*—Bandwidth Enhancement; Cascade Topology; CMOS PA; Group Delay Variation; UWB.**

I. INTRODUCTION

Ultra-wideband (UWB) system has become more popular compared to narrowband system due to its capability to provide short-range wireless personal area networks [1] that can offer low microwave power radiation. Besides, the transmission data rate is notably higher compared to hundreds of megabits per second. One of the challenges in UWB module design is to improve the overall group delay performance characteristic in complex RF module. A minor variation in group delay is required to retain the original identity of the output whilst the time domain does not distort, particularly for UWB system employing impulse signal [2]. Several different approaches have been proposed to enhance bandwidth with low group delay for UWB application. Even though the fabricated UWB power amplifier (PA) in [3] can cover frequency from 3.1 - 10.6 GHz but it deteriorates the group delay of the PA design. Another fabricated PA forming different reported work has shown that low group delay is achieved but the frequency only covers from 5 - 10.6 GHz [4, 5]. Hence, bandwidth enhancement techniques frequently sacrifice the group delay variation and it shows that this is a trade-off characteristic that needs to be compromised. By revisiting previous authors' publication [6], only low group delay variation is being focused. Thus, here a design method is proposed to enhance the bandwidth and at the same time able to achieve low group delay variation simultaneously. The bandwidth extension using shunt peaking technique, a few results that have yet been discussed are explained while centering on the low group delay variation.

II. TOPOLOGY REVIEW

There are many power amplifier topologies that have been reported for wideband communication application with CMOS technology. Ever since multiband orthogonal frequency division multiplexing (MB-OFDM), as well as direct-sequence code division multiple access (DS-CDMA), become two main solutions for UWB transceiver, various UWB for such frequency bands of 3.0 - 5.0 GHz [7], 3.0 - 6.0 GHz [8, 9], 3.0 - 7.0 GHz [10], 6.0 - 10.6 GHz [4, 11], and 3.1 - 10.6 GHz [3, 6] have been implemented with numerous topologies.

The distributed amplifier is one of the well-known topologies for a broadband circuit that provides high-speed communication and good linearity. However, this topology requires a large area and high-power consumption due to several stages active transistor connected in tailored transmission lines to obtain the desired frequency behavior [12]. Improved distributed amplifier by means the combination of both low and high pass filters has been professed to produce artificial transmission line that achieves high output power and spectrum pre-shaping for UWB signal [3]. Nevertheless, it does not solve the problems of the large area resulted from the consumption of many inductors to perform signal delay. Moreover, high group delay is attained in the devised UWB PA.

The shunt feedback topology is typically used to achieve a stable circuit with flat gain, as well as 50 Ω input matching. However, the resulted process variation causes the load resistor to suffer, whereas the power consumption is high. Besides, it is difficult to compromise between gain and bandwidth in this topology [12]. An RLC matching topology was proposed to solve the issue of the wideband matching and power consumption. Unfortunately, several reactive elements like the inductor employed in this topology to form the wideband pass filter cause it to consume a considerable area of the chip [13].

To realize low power consumption, the current-reused

technique is widely used especially in UWB PA, consisting of common gate amplifier and common source amplifier. The advantage of the current-reused structure is its ability to amplify the input signal from the original input signal twice. However, it is a challenge to achieve high gain and notable wide range between 3.1 to 10.6 GHz in this technique [10].

III. Circuit Design

Another approach involves cascade topology employed in low noise amplifier (LNA) circuit [14], however in using this method the good gain flatness could not be achieved. The proposed PA implements three cascade transistors that offer wide-ranging bandwidth feature and gain flatness, in addition to low group variation [6]. Figure 1 shows the proposed UWB PA design with three stages of amplifiers. Stage one involves straightforward construction of common source M_1 and inductive peaking made of L_2 and R_2 that realizes high gain at lower end of the frequency range of interest (i.e. 3.1 GHz). Meanwhile, stage two aims to obtain high gain at high frequency (i.e. 10.6 GHz). The gain of both stages is kept high enough (i.e. above 0 dB) at all frequency of interest. The diagram of Figure 2 appears to show that the passband gains of individual stages are added to produce a total passband. Remember that the stages are in series, so the gains and losses (in dB) are accumulated. As an example, at frequency of 3.1 GHz, the gain at stage 1, stage 2 and stage 3 are 11 dB, 7 dB and -7 dB, respectively as shown in Figure 2.

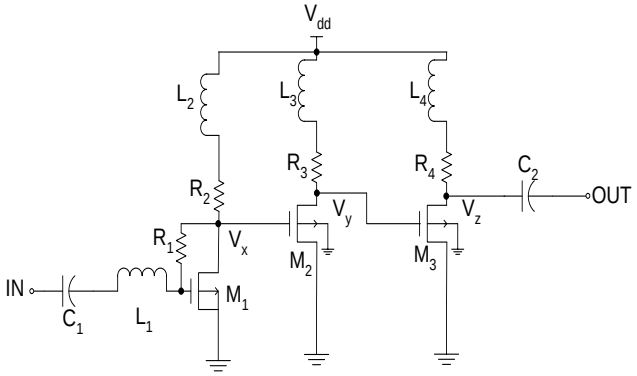

Figure 1: Proposed UWB PA schematic

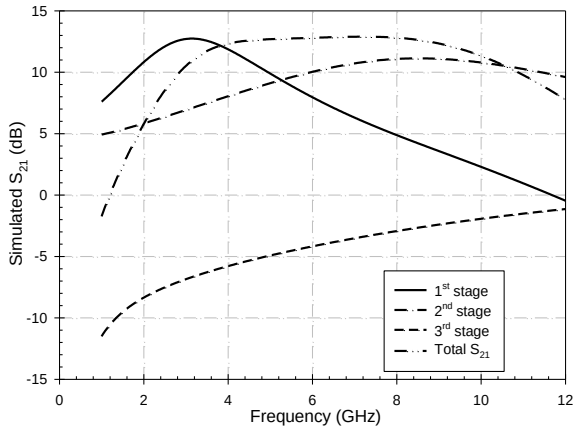

Figure 2: Proposed UWB PA passband gains of individual stages and total passband

On the other hand, stage three is intended with low gain at low frequency and high gain at high frequency, which enhances the gain flatness between the frequency band. For instance, if stage one lacks gain at a frequency, the other two stages will not make up for that to flatten the band. In other words, in cascade of gain and/or loss elements, the passbands are not additive in the simple sense. Therefore, by employing three-stage cascade, wide bandwidth can be achieved. To make up for the constraint of the bandwidth and to enhance the gain flatness of the output stage bandwidth, every single of the shunt peaking load method, including L_2, L_3, L_4, R_2, R_3 and R_4 in the introduced PA are required. Hence, all stages are designed with optimised shunt peaking value of inductor and resistor so that an expansion of bandwidth up to 60% with an ideal group delay can be obtained, that is necessary to optimise pulse fidelity in a broadband system [15]. At stage one, resistive shunt feedback is employed with the aim of achieving a good input impedance above the desired bandwidth. Therefore, this design chooses the optimal value for the feedback resistance, R_1 so that the desired matching and bandwidth can be achieved. A straightforward assembly of LC filter comprising of C_1 and L_1 is applied to give 50 Ω of input matching network. Furthermore, C_1 functions as DC blocking, whereas C_2 helps to enhance the wideband output impedance of 50 Ω matching above all bandwidth of range 3.1 to 10.6 GHz.

IV. Bandwidth Extension Using Shunt Peaking Technique

The inductor is once commonly used in narrowband circuit. Now, it is widely used in broadband circuit. This section will provide an explanation on bandwidth extension by using an inductor in place of shunt peaking for the broadband amplifier.

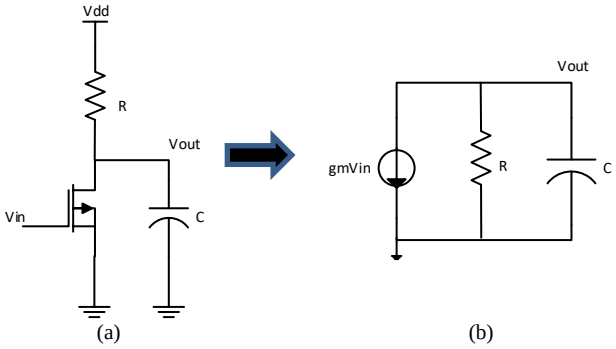

Figure 3: Simple common source amplifier shunt peaking

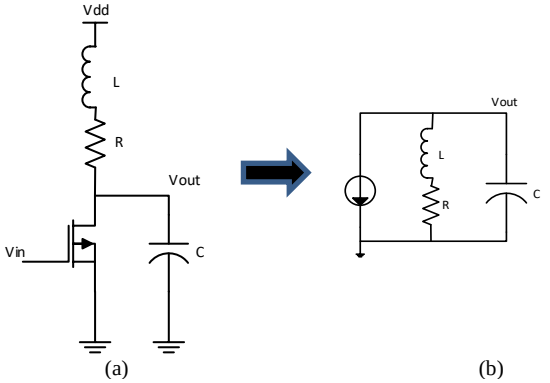

Figure 4: Simple common source amplifier with inductive shunt peaking

Figure 3 (a) shows the basic concept of simple common source amplifier. Figure 3 (b) illustrates the details of the structure as well as its corresponding small signal circuit. The small signal circuit frequency response is stated as (1):

$$\frac{V_{out}}{V_{in}}(\omega) = \frac{g_m R}{1 + j\omega RC} \tag{1}$$

The equation indicates that the single dominant pole is determined by combination output load resistance R and the load capacitance C. Since that only single pole is existed, the combination of parasitic capacitance and resistive load will cause limitation of high-frequency performance [16]. Figure 4 shows the introduction of load resistance series with inductor L. The small signal circuit frequency response can be expressed as (2):

$$\frac{V_{out}}{V_{in}}(\omega) = \frac{g_m(R + j\omega L)}{1 + j\omega RC - \omega^2 LC} \tag{2}$$

From Equation (1) and (2), it can be seen clearly that through the frequency response, the single pole system changes to a system with two poles and a zero. The L/R time constant for the bandwidth improvement indicates this zero. This technique is known as shunt peaking which helps to improve the amplifier bandwidth. Each of the shunt peaking load technique, including L_2, L_3, L_4, R_2, R_3 and R_4 in the introduced PA are compulsory to attain 60% bandwidth extension with an optimal group delay, that is needed in enhancing the pulse fidelity of a broadband system [15].

V. TRANSFER FUNCTION ANALYSIS

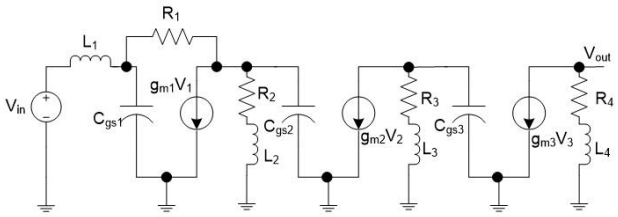

Figure 5: Small-signal circuit of proposed PA

Considering the UWB PAs are designed with the aim of transmitting signal at short distance with minimal power, thus the transfer function of the circuit can be resolved by small signal equivalent. Figure 5 illustrates the details of the structure as well as its corresponding small signal circuit of the three-stage amplifier. If output resistance, r_o is ignored as it is too small, the transfer function for stage one, $H_1(s)$, stage two, $H_2(s)$, and stage three, $H_3(s)$ amplifier are stated respectively in Equation (3), (4) and (5):

$$H_1(s) = -\frac{g_{m2}(g_{m1}R_1 - 1)(R_2 + sL_2)}{s^3 L_1 L_2 C_{gs1} + \left[L_1 L_2 g_{m1} + L_1 C_{gs1}(R_1 + R_2)\right]s^2 + +[L_2 + L_1(1 + R_2 g_{m1})]s + R_1 + R_2} \tag{3}$$

$$(s) = -g_{m2} s C_{gs2}(R_3 + sL_3) \tag{4}$$

$$H_3(s) = -g_{m3} s C_{gs3}(R_4 + sL_4) \tag{5}$$

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = -\frac{B(R_2 + sL_2)(R_3 + sL_3)(R_4 + sL_4)}{s^3 L_1 L_2 C_{gs1} + \left[L_1 L_2 g_{m1} + L_1 C_{gs1}(R_1 + R_2)\right]s^2 + +[L_2 + L_1(1 + R_2 g_{m1})]s + R_1 + R_2} \tag{6}$$

where $B = {g_{m2}}^2 g_{m3}\, s^2 C_{gs2} C_{gs3}(g_{m1}R_1 - 1)$. The overall transfer function H(s) is expressed as (6). From (6), high gain can be obtained by horizontal addition of number of gain stages.

VI. GROUP DELAY ANALYSIS

It is necessary to obtain small group delay in the passband. It indicates that all frequency pass through the amplifier will be delayed relatively in equal amount. Dispersion will occur and the resulted output does not maintain its original input if the group delay is not delayed equally. Generally, the group delay variation is very important in high-speed wireline equalizer as well as for UWB purposes. Both applications have distinctive design consideration. In UWB applications, the group delay expands the signal energy throughout the whole band. Whereas the group delay in high-speed equalizer consists of primary signal energy about the dc region [16]. Group delay is characterized as the derived phase of the transfer function regarding angular frequency. Basically, a transfer function is expressed by a general gain function H(s) with s = jω in a product as (7),

$$H = H_1(s)H_2(s) \ldots H_n(s) \tag{7}$$

where H (s) is gain. Group delay is expressed in (8).

$$G_d(\omega) = -\frac{\partial\theta(\omega)}{\partial\omega} \tag{8}$$

where θ is the phase delay. Since CMOS has high parasitic capacitance in drain, the performance of overall transfer function H(s) should be considered. The overall group delay in a circuit is typically difficult to study; hence assumptions are taken to abridge the transfer function, offering a better understanding of the suggested design. These assumptions include:

i. gain in stage 2 and stage 3 are almost the same.
ii. $R_1 >> R_2$
iii. $1 + R_2 g_{m1} \approx 1$

Illustrated in Figure 5, small signal equivalent is used to find the overall transfer function of the circuit. In equation (6), the total transfer function, H(s) is stated and approximated as (9).

$$H(s) = \frac{B_1(R_2 + sL_2)(R_3 + sL_3)}{s^3 L_1 L_2 C_{gs1} + (L_1 L_2 g_{m1} + L_1 C_{gs1} R_1)s^2 + (L_1 + L_2)s + R_1} = \frac{\left(\frac{s}{\omega_o}\right)^2 + \left(\frac{\omega_o}{Q}\right)s + R_2 R_3}{(\frac{s}{k})^3 mn + (\frac{s}{k})^2 mp + \frac{s}{k} + R_1} \tag{9}$$

where:

$B_1 = -(g_{m1}R_1 - 1)$,
$\omega_o = 1/\sqrt{L_2L_3}$,
$Q = 1/\sqrt{L_2L_3}(L_2R_3 + L_3R_2)$,
$k = 1/L_1+L_2$,
$m = L_1/(L_1+L_2)^2$,
$n = \frac{L_2C_{gs1}}{L_1} + L_2$,
$p = L_2g_{m1} + R_1C_{gs1}$.

Shown in (2), the numerator has two zeros on the imaginary section at the ωo=1 rad/s and Q = 0.577, causing the peaking of the group delay [16, 17]. Whereas one real pole s1=σ_1 and two complex poles$s_2, s_3 = \sigma_2 \pm j\omega_2$ are found at the denominator, which is a third order polynomial. The derivation of the group delay performance of the total transfer function is shown as follows;

$$G_d(\omega) = \frac{\partial\theta(\omega)}{\partial\omega}_{numerator} - \frac{\partial\theta(\omega)}{\partial\omega}_{denominator} \quad (10)$$

$$G_d = \frac{Q\omega^3(R_2R_3+1)}{Q^2R_2^2R_3^2\omega^2 - 2Q^2R_2R_3\omega_o^2 + Q^2\omega^2 + \omega_o^6} - \frac{k(k^4R_1 + k^2\omega^2mp - 3\omega^2mnR_1k^2 + \omega^4m^2np)}{k^6R_1^2 - 2k^4R_1\omega^2mp + k^2\omega^4m^2p^2 + \omega^2k^4 - 2\omega^4k^2mn + \omega^6m^2n^2} \quad (11)$$

Based on Equation (3), small group delay variation can be obtained by setting large value on denominator of the group delay. Therefore, as shown in (11), minimisation of group delay value can be done by decreasing the value of k. When the value of L_1 and L_2 is amplified to maximum, smallest conceivable group delay variation can be obtained, due to the number of k being inversely proportional to both L. Nevertheless, this will upset the gain, input matching and output matching performances. On contrary, the value of L_1 and L_2 are optimised to the preferred gain value, group delay, and both input and output matching. The post-layout simulation of L_1 and L_2 towards group delay variation is shown in Figure 6.

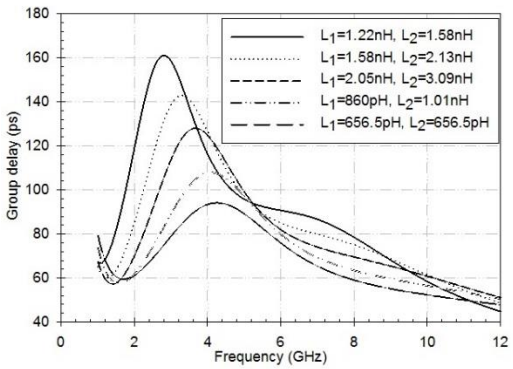

Figure 6: Comparison of inductor, L_1 and L_2 on the group delay variation

V. Linearity Analysis

Designing power amplifier with good linearity has become a challenge, particularly in UWB as the permitted frequency band overlapped other presented application which is conceivably close to the full range of the UWB system [18]. The linearity bounds the power that should be able to drive the load by the PA. Particularly in linear region operations, the PA is able to propel the desired signal with no excessive harmonic terms. Hence, through reducing the gain and power consumption, the linearity is enhanced.

Figure 2 shows the gain partitioning in for each stage of the proposed PA design. It clearly can be seen that the first stage of 13 dB, the second stage of -3 dB and third stage of 11 dB is achieved. Stage two suitable for input third-order intermodulation point (IIP3) due to low gain available. The IIP3 of suggested UWB PA is estimated by means of the equation follows [18];

$$\begin{aligned} \text{IIP3 (in dBm)} &= \frac{4V_T^2}{R_{s2}}\text{(in dBm)} - G_1 \cdot G_2 \cdot G_3\text{(in dB)} \\ &= \frac{4V_T^2}{R_{s2}}\text{(in dBm)} - G_T \end{aligned} \quad (12)$$

where G_1, G_2, G_3 and G_T are the gain for stage one, stage two, stage three and the overall gain, correspondingly, whilst R_{S2} is the real part of the input impedance. From the Equation (12), it shows that high linearity can be achieved with gain trade-off.

VIII. Results And Discussions

The proposed PA design is executed and tested with supply voltage of 2.5 V using 0.18 µm CMOS technology. Figure 7 illustrated the micrograph of the suggested PA with 0.88 mm x 0.78 mm chip dimension, whilst the S-matrix measurements have been operated via the HP8722C vector network analyzer.

The measured and simulated S-parameter is demonstrated in Figure 8. It is shown that the suggested PA produces high gain of 11.48 dB, and 0.6 dB-flatness of 3.1 – 10.6 GHz, whilst retaining a 3 dB-bandwidth of 2.2 – 11.86 GHz. Meanwhile, a stimulated gain of 12.4 dB ± 1.1 dB is obtained. It shows the small difference between simulated and measured gain of 1 dB instigated by the losses due to the parasitic element of the chip and the substrate losses of the testing board. This achieves an input return loss, S_{11} between -10 to -26 dB and an output return loss, S_{22} between -14 to -22 dB, denoting wide characteristic of the input matching and output matching are obtained over the frequency range. The suggested PA accomplishes an optimized reverse isolation, S_{12} of -42 dB above the range of 3.1 - 10.6 GHz as shown in Figure 9. The more negative value achieved will give better reverse isolation. Good reverse isolation, S_{12} indicates that there is no signal reflected from the output to the input. If this happens, it will cause interference along the preferred primary signal going in the onward course. Additionally, Figure 10 portrays that the constancy K-factor of over 24.3 has been realized, with overall power consumption of 100 mW.

Figure 11 illustrates the group delay variation. It is computed by the S-matrices, then decoded to trans-impedance group delay with an Agilent Advanced Design System (ADS) simulator tool. Outstanding phase linearity characteristic such as the group delay variation of 101.2±85.8 ps is attained throughout the entire frequency range. Figure 6 further proves that by optimising the inductor L_2, good group delay is realized. To simultaneously enhance the group delay

and flatness of the gain, the inductor L_2 is fixed to 2.25 nH. Furthermore, the input and output matching is refined to enhance the variations in group delay. Nevertheless, the nonconformities of the model parameters and the fabricated components resulting in variation between the simulated and the measured outcomes. There are two common advantages of linearity, such as output 1dB compression point (OP1dB) and input third-order intercept point (IIP3), that presented the nonlinear gain compression and intermodulation effect correspondingly. Figure 13 shows the two-tone measurements made at 6 GHz whilst measuring the overall linearity of the proposed PA. 12.1 dBm of IIP3 is attained at 6 GHz while the measured 1 dB compression point, P1dB is shown in Figure 12. At 5 GHz and 6 GHz, good P1dB is achieved, which are 4.3 dBm and 3.3 dBm correspondingly. Figure 14 portrays the power added efficiency (PAE) measurement of 16% at P1dB.

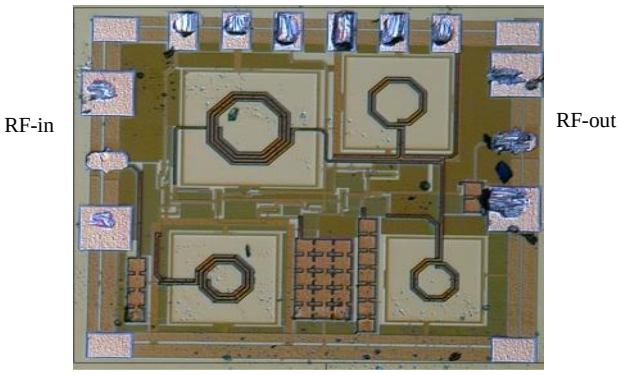

Figure 7: Proposed PA chip micrograph

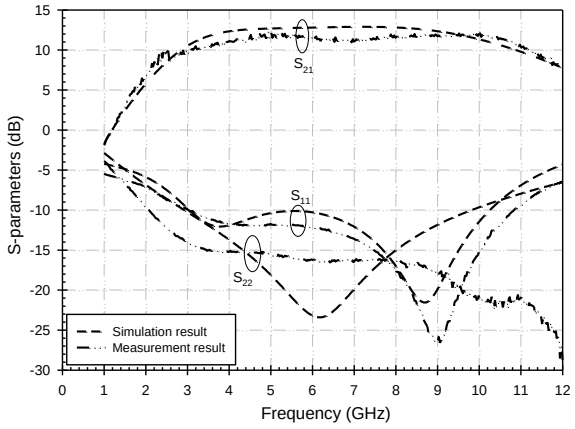

Figure 8: Measured and simulated S-parameters.

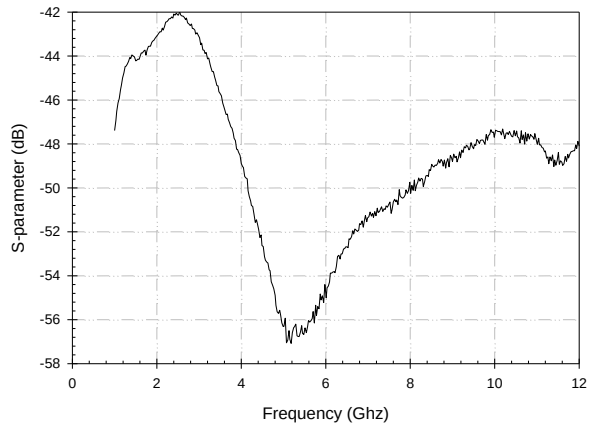

Figure 9: Measured reverse isolation (S_{12}).

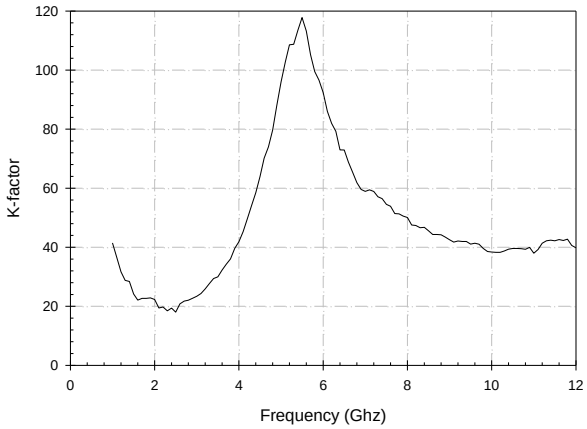

Figure 10: Measured stability factor (K-factor).

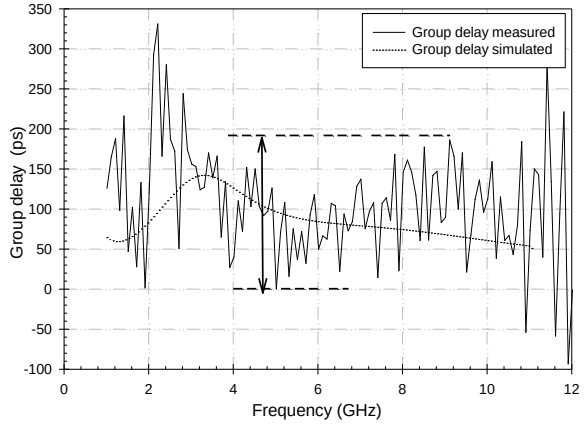

Figure 11: Measured and simulated group delay

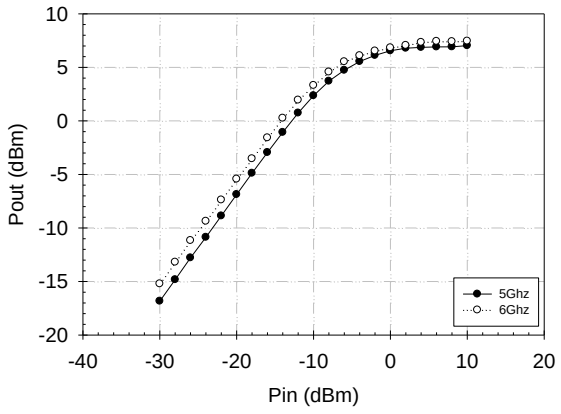

Figure 12: Measured P1dB

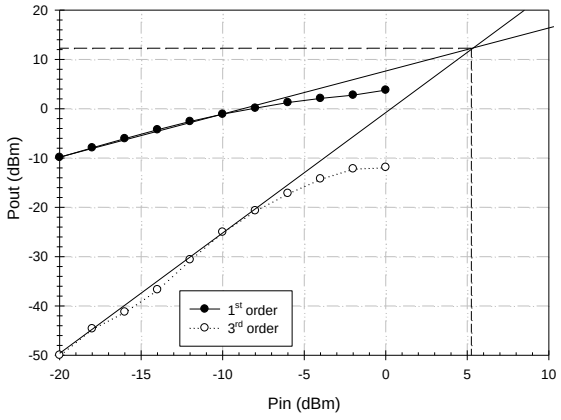

Figure 13: Measured IIP3

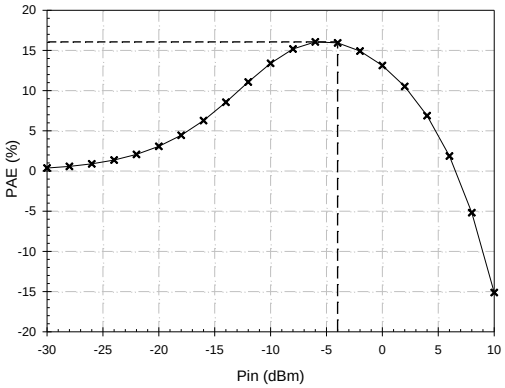

Figure 14: Measured power added efficiency (PAE)

Table 1 synopsizes the performance of newly published PAs. It shows that the suggested UWB PA accomplishes a broad span of frequency from 3.1 to 10.6 GHz, with lowest group delay variation of ±85.8 ps, a satisfactory gain of 11.48 dB and tolerance in gain flatness about ±0.6 dB over the UWB PA frequency. Additionally, this PA design chip area is the smallest of all the reported works on the UWB Pas thus far. Other properties including linearity and PAE of the suggested design are presumed to be consistent with other researchers' work and deemed satisfactory for UWB transmitter. Therefore, these attributes reckon the suggested design the most suitable for UWB application.

Table 1
Wideband CMOS PA Performances in Comparison

Reference	[3]	[5]	[7]	[8]	[10]	[11]	[21]	[22]	[23]	Proposed PA
CMOS technology	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.18
Frequency (GHz)	3.0-10	5-10.6	2.6-5.4	3.0-6.2	3.0-7.0	6-10	3.7-8.8	3.1-4.8	3.0-5.0	3.1-10.6
OP_{1dB}(dBm)	5.6	2	11.4	-5	7.0	5.0	15.6	8	6.6	5
Gain (dB)	10.46 ±0.8	14±1	15.8	11±0.6	14.5 ±0.5	8.5	7.15 ±1.15	10.3±0.8	16±0.5	11.48 ±0.6
S_{11} (dB)	<-10	<-5	<-5	<-14	<-6	<-7	N/A	<-5	<-11	<-10
S_{22} (dB)	<-10	<-7	<-6	<-12	<-7	<-7	<-8	<-8	<-8.5	<-14
Power (mW)	84	20	25	13	24	18	154	24	23.2	100
PAE (%)	N/A	10	34	N/A	N/A	14.4	25	40.5	16.4	16
Group Delay (ps)	±250	±40	N/A	N/A	±178.5	N/A	N/A	±135	N/A	±85.8
Area (mm^2)	1.76	0.77	1.65	0.69	0.88	1.08	2.8	0.97	0.75	0.69

VI. CONCLUSION

A UWB PA of 3.1 to 10.6 GHz frequency has been devised and employed in 0.18 µm CMOS technology. Minimisation of group delay variation over a broad range of desired bandwidth was analyzed. From the hypothetical group delay assessment, we verify that high inductance at the input stage is paramount to attain the lowest group delay. In addition, by using shunt peaking inductor technique, wide bandwidth and low group delay are achieved. Furthermore, average gain flatness, minimal chip area and decent linearity are achieved throughout the overall desired band.

ACKNOWLEDGEMENT

This research has been sustained by the Fundamental Research Grant Scheme (FRGS) from Ministry of Higher Education, Malaysia. The authors are keen to acknowledge UNIMAS for providing financial support to publish the paper.

REFERENCES

[1] R.J. Fontana, "Recent system applications of short-pulse ultra-wide-band (UWB) technology," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 9, pp. 2087-2104, Sep. 2004.

[2] K. Murase, R. Ishikawa and K. Honjo, "Group delay equalized monolithic microwave integrated circuit amplifier for ultra-wideband based on right/ left-handed transmission line design approach," *IET Microwave, Antenna & Propagation*, vol. 3, pp. 967-973, 2009.

[3] C. Lu, A-V. Pham, and M. Shaw, "A CMOS power amplifier for full-band UWB transmitters", in *Proc. IEEE Radio Frequency Integrated Circuit (RFIC) Symposium 2006*, pp.400, 11-13 Jun. 2006.

[4] R. Sapawi, S.A.Z Murad, and D.A.A Mata, "5–11 GHz CMOS PA with 158.9±41 ps group delay and low power using current-reused technique", *International Journal of Electronics and Communications (AEÜ), Elsevier*, pp. 928-932, 2012.

[5] H. Mosalam, A. Allam, H. Jia, A. Abdelrahman, T. Kaho, and R.K. Pokharel, "5.0 to 10.0 GHz 0.18µm CMOS Power Amplifier with Excellent Group Delay for UWB Applications", *Microwave Symposium (IMS)*, pp.1-4, 17-22 May 2015.

[6] R Sapawi, R K. Pokharel, S.l A. Z. Murad, A. Anand, N. Koirala, H. Kanaya, and K. Yoshida, "Low Group Delay 3.1–10.6 GHz CMOS Power Amplifier for UWB Applications", *IEEE Microwave and Wireless Components Letters*, vol. 20, no. 9, pp. 510-512, Jan. 2012.

[7] S. K. Wong, S. Maisurah, M. N. Osman, F. Kung, and J. H. See, "High efficiency CMOS power amplifier for 3 to 5 GHz Ultra-Wideband (UWB) Application," *IEEE Transaction on Consumer Electronics*, vol. 55, no. 3, pp. 1546-1550, Aug. 2009.

[8] L. Y. Wang, B. Li, and Z. H. Wu, "A low-power CMOS power amplifier for implanted biomedical ultra-wideband (UWB) applications," *Solid-State and Integrated Circuit Technology (ICSICT)*, pp. 1-3, 2012.

[9] R. Sapawi, R. K. Pokharel, D. A. A. Mat, H. Kanaya, and K. Yoshida, "A 3.1-6.0 GHz CMOS UWB power amplifier with good linearity and group delay variation", *Proceeding of the Asia Pacific Microwave Conference*, pp. 9 – 12, 2011.

[10] S. Z. Murad, R. K. Pokharel, A. Galal, R. Sapawi, H. Kanaya and K. Yoshida, "An excellent gain flatness 3.0-7.0 GHz CMOS PA for UWB applications", *IEEE Microwave and Wireless Component Letters*, vol. 20, no. 9, Sep. 2010.

[11] H-W Chung, C-Y. Hsu, C-Y. Yang, K-F. Wei, and H-R. Chuang, "A 6-10 GHz CMOS power amplifier with an inter-stage wideband impedance transformer for UWB transmitters," in *proc 38th European Microwave Conference*, pp. 305-308, 27-31 Oct. 2008.

[12] S. Jose, H. J Lee, and D. Ha, "A low power CMOS PA for UWB applications", *IEEE Int, Symposium on Circuit and Systems*, vol. 5, pp. 5111-5114, 23-26 May 2005.

[13] H. C. Hsu, Z. W. Wang, and G. K. Ma, "A low power CMOS full-band UWB power amplifier using wideband RLC matching method", *IEEE Conference on Electron Devices and Solid-State Circuit*, pp. 233-236, 19-21 Dec. 2005.

[14] Y-L. Wang, M-L. Her, and H-H. Lin, "Design and implementation of LNA with high gain and low power consumption for UWB system,"

Asia-Pacific conference on communication, pp 422-425, 2009.

[15] S. Mohan, M. Hershenson, S. Boyd and T. Lee, "Bandwidth extension in CMOS with optimized on-chip inductor," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 346-355, Mar. 2000.

[16] Y. Park, C-H. Lee, J. D. Cressler, and J. Laskar, "The analysis of UWB SiGe HBT LNA for its noise, linearity, and minimum group delay variation," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 4, pp. 1687-1698, Apr. 2006

[17] C.S. Lindquist, "Delay characteristic of second-order bandpass filter," *Proc. IEEE*, vol. 58, pp. 826-828, May 1970.

[18] P. Lerouz and M. Steyaert, LNA-ESD co-design for fully integrated CMOS wireless receivers, T. Dordrecht; New York: Springer, 2005.

[19] C. Grewing, K. Winterberg, S.V Waasen, M. Friedrich', G.L. Puma', A. Wiesbaue, C. Sandne, "Fully Integrated Distributed Power Amplifier in CMOS Technology optimized for UWB Transmitters," In *Radio Frequency Integrated Circuits (RFIC) Symposium, 2004. Digest of Papers. 2004 IEEE*, pp. 87-90. IEEE, 2004..

[20] C. Lu, A-V. Pham, M. Shaw, and C. Saint, "Linearization of CMOS broadband power amplifier through combined multigated transistors and capacitance compensation," *IEEE Trans. Microwave Theory Tech.*, vol.55, no. 11, pp. 2320-2328, Nov. 2007.

[21] S. Z. Murad, R. K. Pokharel, R. Sapawi, H. Kanaya and K. Yoshida, "High Efficiency, Good Linearity, and Excellent Phase Linearity of 3.1-4.8GHz CMOS UWB PA with a Current-Reused Technique", *IEEE Transactions on Consumer Electronics*, vol. 56, no. 3, Aug. 2010.

[22] Z. Qian, X. Cui, B. Wang, X. Zhang, and C-L. Lee, "A folded current-reused CMOS power amplifier for low-voltage 3.0-5.0 GHz UWB application", *International Conference on ASIC (ASICON)*, pp.1-4, 2013.