Electrical Tests for Capacitive Open Defects in Assembled PCBs

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***Abstract*— Nowadays, Ball Grid Array (BGA) becomes a major packaging type due to its high bulk for input/output (I/O) pins. However, there are defects such as voids and cracks occurring between a BGA IC and a PCB which may result in an electrical failure in the circuit. This paper presents electrical tests for capacitive open defects occurring at an interconnection between an IC and a PCB. Feasibility of the electrical test with the test circuit is evaluated by SPICE simulation and experiments. Capacitive open defects occurring at interconnects are detected by the test method. Both simulation and experimental results showed that capacitive open defects generating no logical errors can be detected by the test method at a test speed of 1kHz and 1MHz.**

***Index Terms*—Design for Testability; Electrical Test; Open Defects.**

I. INTRODUCTION

Recently, Ball Grid Array (BGA) has received a lot of attention because of higher assembling density, better electrical and mechanical performances as well as higher reliability than other package styles. The BGA ICs are widely used in printed circuit board (PCB) due to their high bulk for input/output (I/O) pins, easy to mount to the surface of PCB, capable to self-alignment during reflows process and lesser space on the PCB [1-2]. Although BGA owns a lot of advantages, there are several defects occurring at interconnect between a BGA IC and PCB, such as voids and cracks. Those defects are due to electro migration in the solder balls that formed the balls to be a weak contact of interconnect and may result in an electrical failure in the circuit [3-4].

The interconnect defects can be classified into short and open defects. A short defect occurs between metal lines or two nodes due to several factors such as oxide surface conduction while an open defect is caused by a gap due to missing conducting material or extra insulating material [5]. In an assembled PCB, a fracture usually occurs simultaneously at the package and the board interface. It initially occurs on one side, then grew to another edge of the joint, and causes a complete fracture. However, direct inspection of the solder joint is difficult because they are hidden under the IC packages. Boundary scan test method based on IEEE 1149.1 standard has been introduced in many logic ICs to detect defective interconnects between ICs [6]. However, an open defect at interconnect may not always be detected by a boundary scan test method. These problems have attracted much attention from researchers into the BGAs packages reliability in the past few years since the requirements of product quality and production efficiency has become more demanding. Thus, in this direction, several electrical test methods for detecting open defects have been proposed as stated in [7-10].

We proposed an electrical interconnect test method for open defects occurring at interconnect between an IC and a PCB [11]. A hard and resistive open defect can be detected by the test method that was proved by some experiments. Nevertheless, details of a capacitive open defect by the test method were not clear yet [11]. In fact, it is believed that fully disconnecting interconnect can still provide adequate performance for high speed logic signal transfer [12]. Thus, we examined by circuit simulations and experiments of the capacitive open defect by the test method.

This paper presents the simulation and experimental results that are organized as follows: Section 2 presents the principle of our electrical tests. Simulation and experimental on the circuit architecture as well as the evaluation results are discussed in Section 3. Finally, the conclusion of this paper is presented in Section 4.

II. PRINCIPLE OF ELECTRICAL INTERCONNECT TEST

The electrical interconnect test method proposed in [11] is based on quiescent supply current that is made to flow only in the tests. An IC on a PCB circuit is designed so as for quiescent supply current to flow. Thus, Design for Testability (DfT) is necessary for the IC design. Figure 1 shows the testable design block with IEEE1149.1 test circuit that consists of IC#1 and IC#2 denoted by [11]. A test mode signal, T_{st}, is placed in each ICs and all terminals are connected to a switch, Sw1. A resistor, Rc, is inserted at terminal 2 of Sw1 and ground (GND) at terminal 1. To run the simulation, high (H) level signal and low (L) level signal are set at T_{st2} and T_{st1} respectively. Besides, H level signal is designated for defective interconnect while L level signal is fixed for other interconnects and led Sw1 to be at terminal 2 as shown in Figure 1.

Figure 2 illustrates the principle of the electrical interconnect test when a defective interconnect b is tested. The circuit added by the DfT is labeled as an "Added Circuit Block" in Figure 2 which consists of n-channel Metal Oxide Semiconductor (nMOS) switches and diodes. The anode terminal of those diodes is connected to a test terminal TSTO. The defective interconnect is detected by changes of the voltage across R_C, V_{Rc}, at T_{STO}. By providing high (H) level signal and low (L) level signal to b and to the other interconnect respectively, supply current, I_{Dtn}, and will flow through *b* to T_{STO} if no open defect occurs at *b*. On the other

hand, when an open defect occurs, supply current smaller than I_{Dtn} will flow.

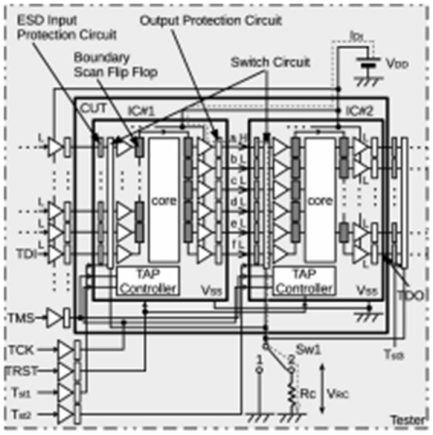


Figure 1: Testable design block

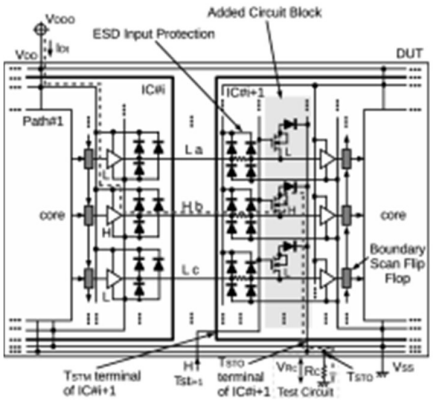


Figure 2: Principle of interconnect test

The differences appear in voltage across R_C. Thus, Eq. (1) represents the existence of open defects occurred at defective interconnect [14].

$$V_{RcN} - V_{RcC} \geq V_{th} \tag{1}$$

where V_{RcN} and V_{RcC} are measured quiescent voltages in the defect-free circuit and in the circuit under test (CUT) respectively. V_{th} is a threshold voltage that is specified from the variation of V_{RcN}.

A capacitive open defect is an open defect occurring between a land on a PCB and a ball of a BGA IC. When they are separated from each other by a gap of d, the open defect is modelled as a capacitor, C_f, which capacitance is defined by Eq. (2)[15].

$$C_f = k\varepsilon_0 \frac{S}{d} \tag{2}$$

where k is a dielectric constant, ε_0 is a permittivity of a vacuum and S is a BGA cross-sectional area. The diameter of a BGA ball and the gap of a targeted open defect in this paper are about 0.18~0.89mm and 1µm, respectively. When a capacitive open defect occurs at interconnect and tested by our test method, I_{Dtn} will not flow. Since the measured V_{RcC} is zero, the defect is detected by Eq. (1).

III. Feasibility Test Of DFT Method

In order to examine the feasibility of open defect detection, evaluation by SPICE simulation and experiments were conducted. We designed a layout of an IC in which our testable designed circuit was embedded of a 0.18µm CMOS process of Rohm Co. Ltd.

A. Evaluation by SPICE Simulation

For the evaluation by SPICE simulation, we extracted a SPICE netlists with an extraction tool "Virtuoso" produced by Cadence from the layout. We coded a SPICE netlist of the simulation circuit shown in Figure 3 from the SPICE netlist of the IC with added a parasitic resistor, R_p, and a parasitic capacitor, C_p, of an interconnect between the ICs.

Capacitive open defects are inserted to the netlist at interconnect S1 in Figure 3 by adding a capacitor, C_f, of 1pF to 6pF based on the calculation using Eq. (2). Open defects in the IC may be detected at a test speed faster than 500Hz. So, test input signal to S0, S1, S2 and S3 per Ts of 1ms and 1µs are provided as shown in Figure 4. The parasitic resistance, R_p, parasitic capacitance, C_p, and a resistor, R_C, are 0.1Ω, 10pF and 100Ω respectively. The source voltages used are V_{DDO}=3.3V *and* V_{DD}=1.8V.

Simulation results are shown in Figure 5 and Figure 6 at a test speed of 1kHz and 1MHz respectively. Figure 5(b), (c) and Figure 6 (b), (c) show that smaller quiescent V_{Rc}, relative to defect-free circuit (Figure 5(a), Figure 6 (a)) when *S1=H*. They reveal us that the defects are detected both at 1kHz and 1MHz. As the H level signal provided and in the meantime capacitive open defects occur at *S1*, the output signal, V_{out}, are shown in Figure 7.

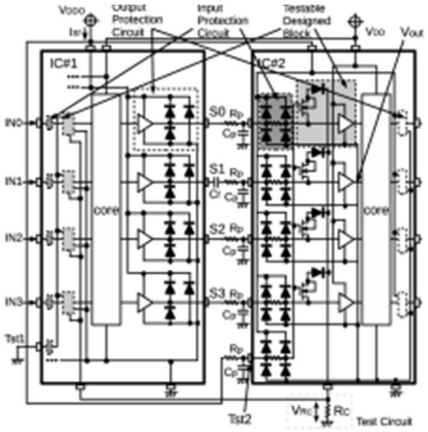


Figure 3: Simulation circuit architecture

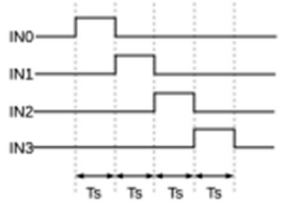
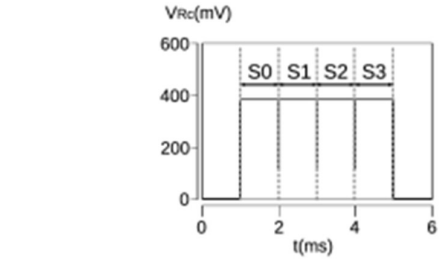
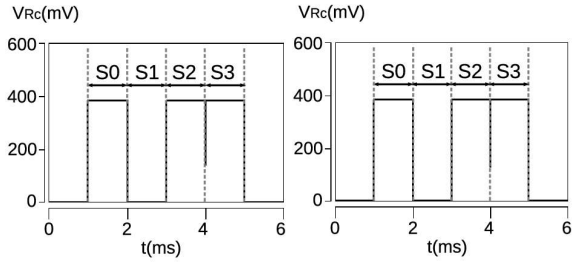


Figure 4: Test input signal

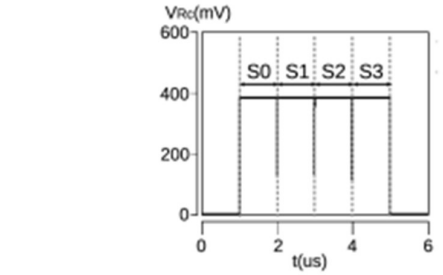


(a) Defect-free

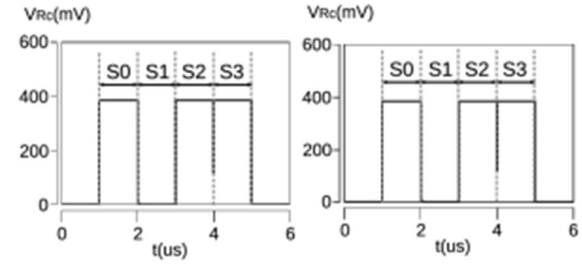


(b) C_f =3pF (c) C_f =4pF

Figure 5: Simulation results of capacitive open defects at 1kHz



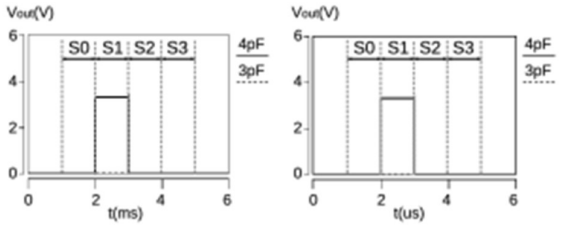
(a) Defect-free



(b) C_f =3pF (c) C_f =4pF

Figure 6: Simulation results of capacitive open defects at 1MHz

No logical error appears when C_f=4pF, while a logical error occurs when C_f=3pF. From Figure 5(b), (c) and Figure 6 (b), (c), it is said that capacitive open defects generating no logical errors are detected by our test method. The results show the value of C_f from 4pF and above will generate no logical error and vice versa. Thus, it shows that signals are propagated through the empty space between IC and PCB land. These simulation results are supported by [13].



(b) Output signal at 1kHz (c) Output signal at 1MHz

Figure 7: Output signal when H signal provided to S1

B. Evaluation by Experiment

For the evaluation by experiment, we prototyped the designed IC which our test circuit was embedded. We built a PCB circuit made of the prototyping ICs as shown in Figure 8. H signal is provided to the IC by a pattern generator to each interconnect S0, S1, S2, and S3. The followings are used in our experiments as source voltages specified by the CMOS process: V_{DDO}=3.3V and V_{DD}=1.8V. A resistor of 100Ω is used as RC. We inserted a capacitive open defect at S1 by adding a capacitor, C_f, from 1pF to 6pF to interconnect in the defect-free circuit. The signals are provided to the circuit per T_s of 1ms and 1µs as shown in Figure 9.

The experimental results of 1ms and 1µs are shown in Figure 10 and Figure 11 respectively. The measured value of V_{Rc} is smaller than SPICE simulation due to several factors such as parasitic capacitance of interconnect in prototyping IC and a PCB is larger than the SPICE simulation. Figure 10(b), (c) and Figure 11(b), (c) show smaller V_{Rc} relative to the defect-free circuit (Figure 10(a), Figure 11(a)) when *S1=H*. They reveal us that the defects are detected both at 1kHz and 1MHz.

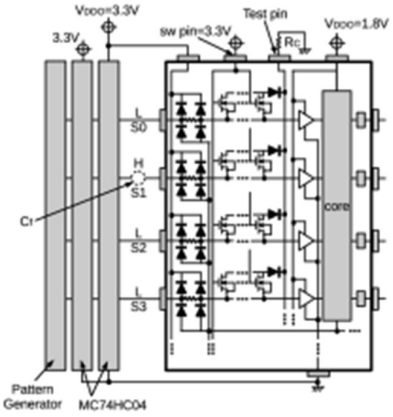


Figure 8: Experimental circuit with our prototyping IC

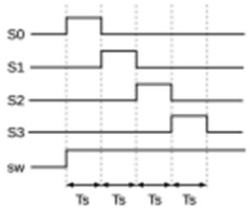
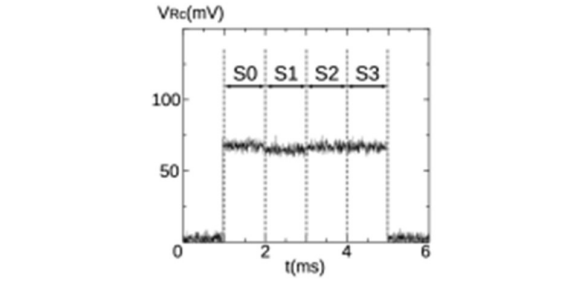
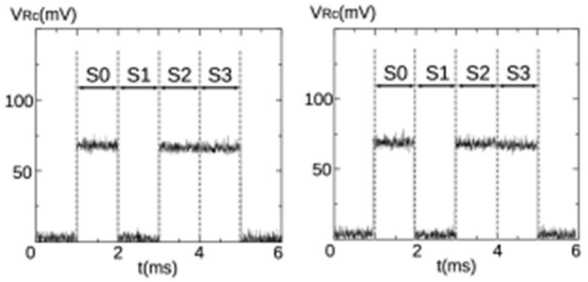


Figure 9: Test input signal

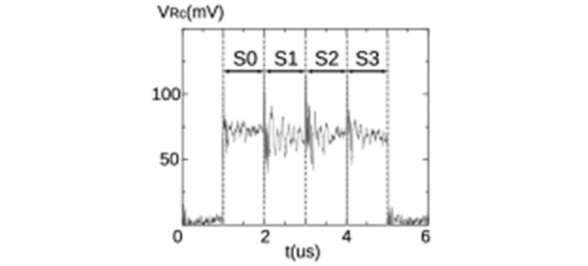


(a) Defect-free

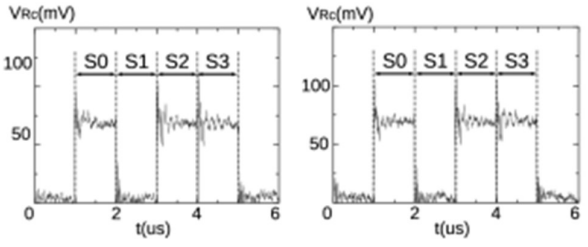


(b) C_f =3pF (c) C_f =4pF

Figure 10: Experimental results of capacitive open defects at 1kHz



(a) Defect-free



(b) C_f =3pF (c) C_f =4pF

Figure 11: Experimental results of capacitive open defects at 1MHz

IV. CONCLUSION

In conclusion, an electrical test approach in assembled PCB had been proposed in order to determine the capacitive open defects at a land on a PCB and a ball of BGA. To demonstrate the feasibility of proposed test method, circuit simulation and experiment were conducted. The results show that capacitive open defects generating no logical errors are detected by the test method. Based on both simulation and experimental results, as a post-bonding test, we strongly believed that the proposed electrical test method could determine the defective interconnects that may not be detected by the boundary scan test. Moreover, the size of DfT is small in size that can embedded into IC without increasing the size of the chip. Although in this stage positive results are obtained, further investigation of testability of capacitive open defects in a PCB circuit remains as a future work.

ACKNOWLEDGMENT

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