Electrical Test of Resistive and Capacitive Open Defects at Data Bus in 3D Memory IC

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***Abstract*— We propose an electrical test method of resistive and capacitive open defects occurring at data bus lines between dies, and between dies and I/O pins in 3D memory ICs. The test method is based on supply current of an IC. The number of test vectors for a 3D memory IC made of ND memory dies in the test method is 10·ND and small. Also, defective interconnects are located by the test method. Feasibility of the tests is examined by some experiments for a circuit made of an SRAM IC on a printed circuit board. The experimental results show that capacitive open defects and resistive open ones whose resistance values are greater than 200Ω can be detected by the test method.**

***Index Terms*— 3D memory IC; Data bus; Open defect; Supply current test.**

I. INTRODUCTION

A lot of attention has been paid to 3D stacked ICs, since low power dissipation and high speed operations are realized in the ICs [1]. 3D stacked ICs are made of known good dies. The dies are stacked and connected with Through Silicon Vias (TSVs) and micro bumps. Defects can occur at interconnects between dies in 3D stacked ICs including 3D stacked memory ones, since the fabricating process is complex. Thus, many kinds of test methods and DfT (design for testability) methods have been proposed for 3D stacked ICs [2-13].

Generally, interconnects between dies in 3D stacked logic ICs are tested by a boundary scan test method. In order to test them by the test method, a testable designed circuit should be embedded to each of the dies in the ICs. However, some speed degradation appears in the testable designed circuits. Since high speed operation is requested for memory ICs, it may not be accepted to add a boundary scan test circuit to dies in 3D stacked memory ICs [10].

Since open defects at TSVs may be detected by electrical tests, many kinds of electrical test methods and DfT ones have been proposed [14-24]. However, a testable design is indispensable for the tests and may cause additional delay in defect-free ICs. Thus, a test method of 3D stacked memory ICs, which are abbreviated as 3D memory ICs in this paper, should be developed with no testable design.

We have proposed an electrical test method for TSVs that transmit bi-directional signals [25]. The test method does not request us to add testable designed circuits to an original circuit. Since data bus lines in an SRAM IC are bi-directional signal lines, we proposed an electrical test method based on the test principle of the test method for bi-directional signals [26].

Hard open defects, resistive open defects and capacitive open defects are selected as targeted defects of the test method proposed in [26]. However, hard open defects will be detected by functional test methods. Generally, ICs are tested by functional test methods before shipping to a market. Thus, hard open defects need not be added to targeted defects of electrical tests.

We propose an electrical test method to detect only resistive open defects and capacitive open ones occurring at data bus lines between dies, and between dies and I/O pins in 3D stacked memory ICs. We examined feasibility of our electrical tests with a circuit made of an SRAM IC on a printed circuit board. After proposing the test method in section 2.0, we denote the experimental evaluation results in section 3.0.

II. ELECTRICAL TEST METHOD

A 3D stacked IC is made by stacking known good dies. Thus, we assume in this paper that dies in 3D memory ICs are known good ones.

The dies are connected with TSVs and micro bumps. An example of 3D memory ICs is shown in Figure 1.

Open defects can occur in TSVs and at micro bumps in the fabrication process. They can occur at data bus, address one and control one in 3D memory ICs. The open defects occurring at data bus are targeted ones in our test method.

Open defects occurring at the interconnects can be classified into two types: hard open defects and soft ones. When a hard open defect occurs at TSVs and micro bumps, they are separated into two parts. When the gap between the parts is long, no logical signal will be propagated. The open defect is modeled as a resistive open defect of infinite resistance. When the gap between the parts caused by a hard open defect is short, a high speed signal will be transferred without errors. The hard open defect is modeled as a capacitive open defect. On the other hand, when a soft open defect occurs at TSVs and micro bumps, the output ports of them are connected to the input ports in part. The soft open defect can be modeled as a resistive open defect of finite resistance.

In this paper, we discuss a test method for detecting only capacitive and resistive open defects occurring at interconnects between dies, and between the bottom die and I/O pins of the IC, since hard open defects are detected by

functional test methods. Circuit blocks of typical memory dies are shown in Figure 2(a).

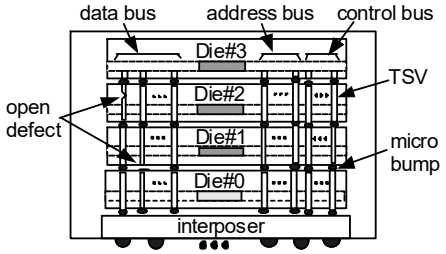
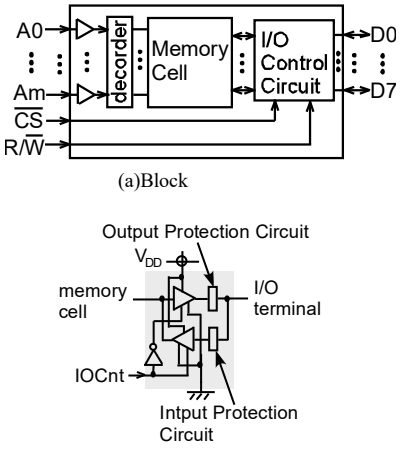


Figure 1: 3D memory IC and targeted defects



(a)Block

(b)I/O control circuit

Figure 2: Configuration of Memory IC

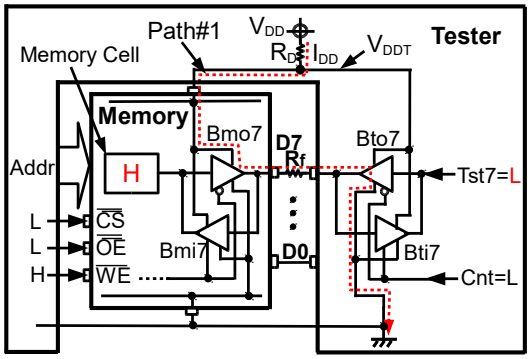
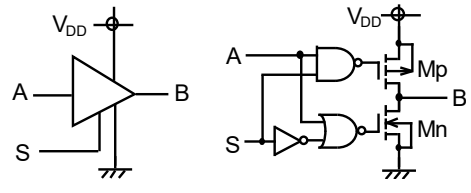


Figure 3: Electrical interconnect test of 3D memory IC



(a)gate symbol (b)equivalent circuit

Figure 4: 3-state buffer gate

Memory dies are made of memory cells, an address decoder and input/output control circuits. Memory cells to be accessed are specified by address data. The contents of the accessed memory cells are read out from the die. Also, some data are stored to the memory cells. The input/output operations are controlled by a chip select signal ($\overline{CS}$) and a read/write control signal (R/$\overline{W}$).

Each of dies in our targeting 3D memory ICs is made of word memories, each of which consists of 8 memory cells and is assigned to an address. By specifying an address, one byte data are read out from a word memory of the address or stored into it.

Each memory cell is accessed through an I/O control circuit whose example is shown in Figure 2(b), since data bus lines are bi-directional signal lines.

Test principle of the test method proposed in this paper for a data bus line D7 is shown in Figure 3. At first, a logic value is written into a memory cell. When the value is read out from the cell, a logic signal of the complement value is provided to the bus line from the outside of the IC in our tests. An equivalent circuit of a 3-state buffer gate is shown in Figure 4. A high level signal and low level one are denoted as H and L, respectively, in this paper. When H and L are provided to a data terminal A, an nMOS Mn and a pMOS Mp are turned on, respectively, if H is provided to an I/O control terminal S. Thus, by providing a logic signal of L that is complement to the one in a memory cell from a 3-state gate, a large supply current will flow along a path Path#1 as shown in Figure 3.

If a capacitive open defect and a hard one occur at a data bus line of D7, the supply current will not flow. If a resistive open defect occurs at it, smaller supply current will flow than the defect-free IC. Thus, it is examined whether (1) is satisfied in our tests. If (1) is satisfied, it is judged that an open defect occurs at the targeted data bus line.

$$I_{DDn} - I_{DDc} \geq I_{th} \quad (1)$$

where I_{DDn} and I_{DDc} are supply current I_{th} in the defect-free circuit and in the device under test, respectively. Ith is a threshold value.

If an open defect occurs at a data bus line, the logic value stored in a memory cell is unknown. Thus, in the test method proposed in [26], both H and L are provided to the targeted data bus line. Since test time should be short as possible, we tried to shorten our test time.

Our new test method for data bus lines between dies and between a die and I/O pins in a 3D memory IC is as follows:

<1> H is stored to all of the memory cells in a word memory inside each of the dies in the 3D memory IC.

<2> The data stored in the word memory are read out. If L is read out from a memory cell in the word memory, it is determined that an open defect occurs at the data bus line connecting to the memory cell.

<3> L is provided to each of the memory cells of the word memory from a tester and supply current IDD is measured. If (1) is satisfied, it is determined that an open defect occurs at the data bus line connecting to the memory cell. If (1) is not satisfied for all of the memory cells, it is determined that an open defect does not occur at the data bus lines.

The number of test vectors for a 3D memory IC made of ND memory dies in the test method is 10•ND. Supply current measurement is time-consuming. However, since the number of the measurements is 8•ND, test time of the test

method is proportional to ND and acceptable in production tests.

In the test method proposed in [26], the process at <1> is not performed and IDD that flows when both H and L are provided to the IC is measured. The current measurement time is extremely longer than a logic signal application to the IC. Thus, the test time of the test method denoted above is shorter than the one proposed in [26].

III. Experimental Evaluation

We examine feasibility of our tests with an experimental circuit shown in Figure 5. The circuit is made of a CMOS SRAM IC μPD431000 (1M-bits CMOS Static RAM, 128k-words by 8-bits) and a bus driver IC 74HC244 on a printed circuit board.

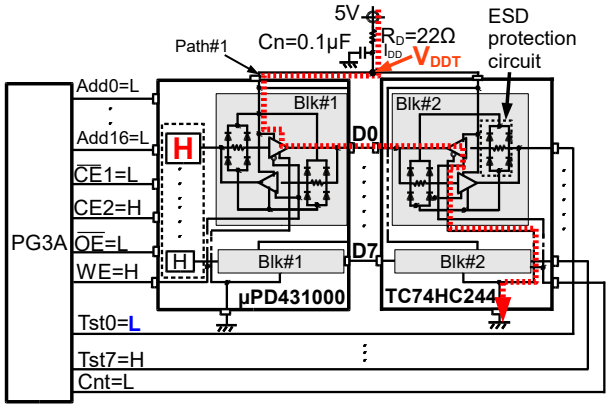


Figure 5: Experimental circuit

In our experiments, a resistive open defect, a capacitive one and a hard one are inserted to D0 in Figure 5. The resistive open defect and the capacitive one are inserted by adding a resistor of 200Ω and a capacitor of 1nF. The hard open defect is inserted by eliminating the signal line of D0 from the experimental circuit.

IDD is measured as the voltage across a resistor RD which is referred to as VDDT. VDDT waveforms are measured with a digital oscilloscope DPO3034. Test signals are provided with a pattern generator PG3A.

When a data is read out from the SRAM IC, H and L should be provided to it as a write-enable signal ($\overline{\text{WE}}$) and an output enable signal ($\overline{\text{OE}}$), respectively. The waveforms of test signals in our experiments are shown in Figure 6. The signals are provided per Ts=100μsec. When Tst0=L, Cnt=L and $\overline{\text{OE}}$ =L, D0 in our experimental circuit can be tested by our test method.

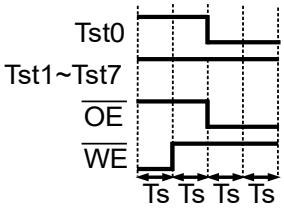


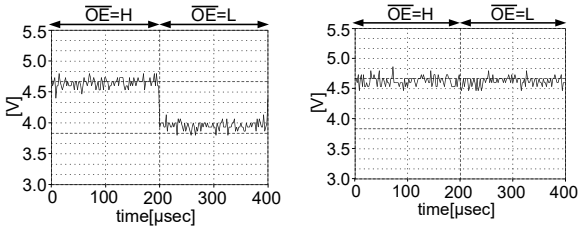
Figure 6: Test signals.

In order to test the data bus line of D0 by our test method, data "11111111" are stored into memory cells whose address is 000H. After that, a test data "11111110" is provided to the data bus line and L is provided to Cnt. As a result, supply current will flow along a current path denoted as "Path#2". Hence, VDDT will decrease in the defect-free circuit.

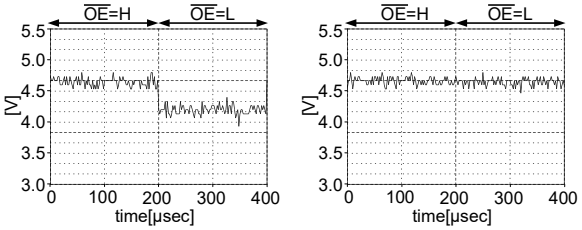
When a capacitive open defect occurs at the data bus line, the current will not flow. When a resistive open defect occurs at it, smaller current than the defect-free circuit will flow.

Measured waveforms are shown in Figure 7. In Figure 7(a), a large supply current flows and VDDT decreases when $\overline{\text{OE}}$=L. When a hard open defect occurs at D0, IDD will not flow and VDDT does not decrease when $\overline{\text{OE}}$=L as shown in Figure 7(b). When a resistive open defect of 200Ω occurs, smaller IDD flows than in Figure 7(a), and VDDT which is larger than in Figure 7(a) appears as shown in Figure 7(c). When a capacitive open defect occurs, IDD does not flow and VDDT does not decrease as shown in Figure 7(d). Thus, the resistive open defect and the capacitive one are detected by our test method.

Test speed of the test method has not been examined. It remains as a future work to examine it.



(a)Defect-free (b)Hard open defect



(c)Resistive open defect of 200Ω (d)Capacitive open defect of 1nF

Figure 6: Measured waveforms of V_{DDT}

IV. Conclusion

We have proposed an electrical test method for detecting resistive open defects and capacitive ones occurring at data bus lines between dies, and between dies and I/O pins in 3D memory ICs. We have examined feasibility of our tests with an experimental circuit made of an SRAM IC on a printed circuit board. It is shown by the experiments that capacitive open defects and resistive open ones whose resistance values are greater than 200Ω are detected by the test method.

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