The Analysis of Low Phase Nonlinearity 3.1-6 GHz CMOS Power Amplifier for UWB System

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***Abstract*—Low phase nonlinearity is important criteria in power amplifier (PA) especially in ultra-wideband system so that the output will remain original identity. Up to date there is no analysis study have been established in achieving low group delay PA in UWB technology, therefore this paper is to examined the factors that affect low phase nonlinearity in 3.1-6.0 GHz PA using two-stage amplifier with shunt resistive feedback technique for UWB system. The proposed PA adopts two stages amplifier together with inter-stage circuit to obtain adequate flatness of the gain. The shunt resistive feedback topology is used to have very wide input matching. The inductive peaking technique and Class A amplifier is adopted to obtain high gain flatness, low phase nonlinearity and linearity simultaneously. The analysis shows that the dominant factor is identified for low phase nonlinearity in UWB PA. The proposed PA achieves the average gain of 10±1 dB, S_{11}<-6dB, S_{22}< -7 dB, and phase nonlinearity of ±195.5 ps. A good linearity and power consumption are obtained. Therefore, these key performance factors of low phase nonlinearity can be applied to facilitate other researchers working in the area of power amplifier circuit design.**

***Index Terms*—Power Amplifier; CMOS; UWB; Phase Nonlinearity;**

I. INTRODUCTION

UWB technology has recently received significant attention to all researchers including academia and industry because of interesting benefit of high data rate, short distance range technology and low power. This makes UWB as fascinating technology for military and medical purposes that apply radar and information sensing [1, 2]. Multiband orthogonal frequency division multiplexing (MB-OFDM) proposal is a major solutions under consideration for UWB transceiver. MB-OFDM proposal offers each channel of 528 MHz by using 122 QPSK sub-carriers with 14 channels into five groups from 3.1–10.6 GHz as shown in Figure 1 [3, 4].

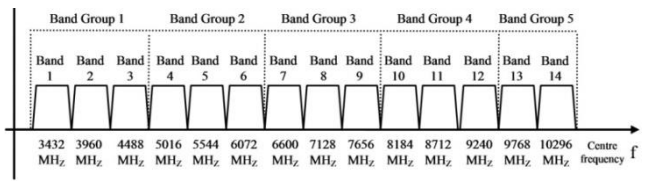

Figure 1: The band structure of MB-OFDM UWB system [4]

Group 1 and Group 2 with frequency range of 3.1 to 6.07 GHz is chosen as proposed PA [5]. The challenge in UWB module is to achieve low phase nonlinearity in power amplifier over a wide frequency band. Low phase nonlinearity is required so that the output will retain its original identity and the time domain will not become distorted especially for UWB system using impulse signal [6].

Several approaches UWB PAs have been implemented for frequency of 3.0–5.0 GHz (Group 1) [7-9], 3.0-6.0 (Group 1 to Group 2) [10, 11], 3.0–7.0 GHz (Group 1 to Group 3) [12], 5.0-10 GHz (Group 2 to Group 5) [13], 6.0–10.0 GHz (Group 4 to Group 5) [14, 15] and 3.1-10.6 GHz (Group 1 to Group 5) [16, 17]. Each of the group used different approach depending with the application. The distributed amplifier is typically used for wide frequency range and provides good linearity. However, this approach uses large area of chip and consumes high power consumption which is not suitable for UWB applications [18]. The RLC matching has the capability to offer very wideband matching but since that this approach requires many reactive element to form RLC filter that cause large area of chip [19]. The shunt feedback topology has advantage to offer flat gain and good wideband input and output matching, but high power consumption will produced [8]. In current-reused technique is one of the latest topology that used in UWB PA to have low power consumption, however it is tough to fulfil high gain with very wide frequency [12]. Another fabricated PA reported by using cascade common source topology also have shown that very wide band of 3.1 to 10.6 GHz , low phase nonlinearity, high gain, good gain flatness and small chip area were implemented and designed in PA for UWB application [11]. However, this design consumes very high power consumption up to 100 mW. Since that phase nonlinearity is one of the important criteria in power amplifier design for UWB and based on the studies mentioned above there is no analysis study have been established in achieving low phase nonlinearity power amplifier in UWB system.

This paper is to investigate the dominant factors influence in achieving minimum phase nonlinearity power amplifier from 3.1 to 6.0 GHz for UWB technology. In order to achieve phase nonlinearity, adequate and solid understanding is required on main design factors that must take into account, which include operating bandwidth, phase nonlinearity, linearity, and gain flatness for UWB. The theoretical analysis on the low phase nonlinearity is specified for UWB PA. Thus, the implementation of PA design is using 0.18µm CMOS technology has achieved average gain of S_{12}, good linearity, low phase nonlinearity, simultaneously. Also, the area of chip size is very small. The paper outline is as follows. In section II, the proposed design of UWB PA is presented. Section III, IV and V discuss the

detailed analysis for transfer function, group delay variation and linearity for proposed circuit design. Section VI is the detailed of measurement and simulation results. Finally, Section VII draws the conclusion.

II. CIRCUIT DESIGN

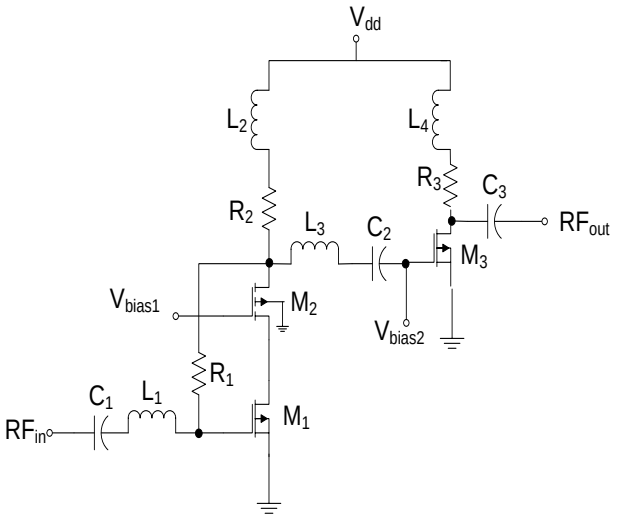

Figure 2: Proposed PA design schematic.

In the proposed PA there are two stage amplifiers in order to achieve high gain. First stage is employed cascode topology where common source stage and common gate is connected together on top of common stage. This technique provides good stability and isolation between the drain M_1 and common gate stage M_2. Hence, it will remove the Miller effect that exists in the circuit. M_2 is not useful in increasing the gain but has the possibility to improve the performance of the output impedance and enhance the reverse isolation. Resistive shunt feedback is connected to input stage so that 50Ω input matching can be achieved over wide bandwidth. Calculation of the input resistance is in Equation (1):

$$R_{in} = \frac{R_1}{1 + A} \tag{1}$$

From Equation (1), good input matching can be attained by using small value of R_1. But, the gain will decrease because of the significant signal feedback through the path. The value of R_1 must be large enough to achieve higher gain but it will reduce the effect feedback. Therefore, the optimization the value of R_1 needs to be chosen to meet high gain and good input matching. For input matching, simple LC is used to meet 50 Ω. M_1 (160µm/0.18 µm), M_2 (320µm/0.18µm) and M_3 (121.6µm/0.18µm) are biased in class A and retained in saturation region operation. First stage and second stage is connected with interstage circuit that consists of series of L_3 and C_2 to enhance the gain flatness of proposed PA. Fig 3 shows the post layout simulation on optimization value of L_3 to obtain a flat gain. By selecting appropriate value of L_3 to 2.3nH i.e., the flatness gain of 10±1 dB is achieved for entire frequency range. At second stage, the cascade common source transistor M_3 is employed to increase the gain and frequency response. Every stage is connected with shunt peaking load technique (i.e., L_2, L_4, R_2 and R_3) in order to have low phase nonlinearity and increase gain flatness. Therefore, the proposed PA is designed using the shunt peaking inductor and resistor to attain 60% bandwidth extension with optimum phase nonlinearity [20]. C_3 is employed at the output stage to have broadband output impedance of 50Ω matching.

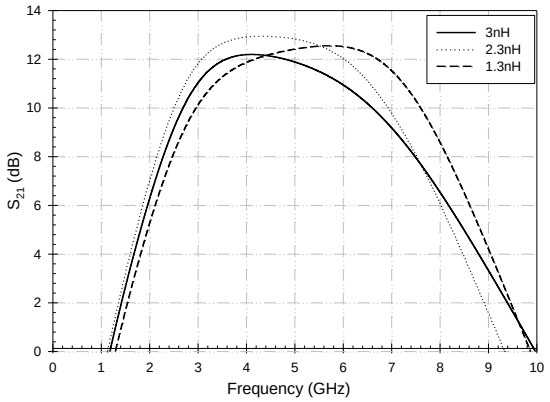

Figure 3: Effect of L_3 on gain (post layout simulation)

III. TRANSFER FUNCTION

Small signal equivalent approach is used to examine the transfer function of the circuit. Figure 4 is the small signal circuit of proposed PA design.

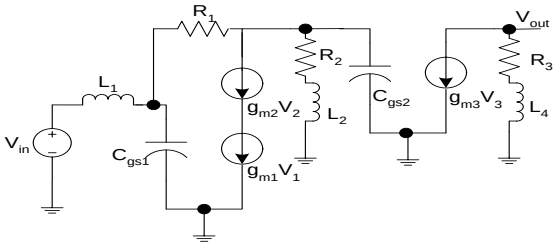

Figure 4: Small signal circuit

The parameter of C_{gd} and r_o are ignored due to the value of both parameters are insignificant. The transfer function of the first stage, $H_1(s)$, second stage amplifier, $H_2(s)$, and the overall of the transfer function can be calculated as Equation (2), (3), and (4), respectively.

$$H_1(s) = -\frac{sL_2(1 - g_{m1}R_1) + R_2(1 - R_1 g_{m1})}{\begin{matrix} s^3 L_1 L_2 C_{gs1} + \left[L_1 L_2 g_{m1} + C_{gs1} L_1 R_1 + C_{gs1} L_1 R_2\right] s^2 \\ +[L_2 + L_1 + L_1 R_2 g_{m1}]s + R_1 + R_2 \end{matrix}} \tag{2}$$

$$H_2(s) = -g_{m2}(R_3 + sL_4) \tag{3}$$

$$\begin{aligned} H(s) &= H_1(s) \cdot H_2(s) \\ &= \frac{s^3 L_1 L_2 C_{gs1} + \left[L_1 L_2 g_{m1} + L_1 C_{gs1}(R_1 + R_2)\right] s^2}{\begin{matrix} s^3 L_1 L_2 C_{gs1} + \left[L_1 L_2 g_{m1} + L_1 C_{gs1}(R_1 + R_2)\right] s^2 \\ +[L_2 + L_1(1 + R_2 g_{m1})]s + R_1 + R_2 \end{matrix}} \end{aligned} \tag{4}$$

where $B = g_{m2}(1 - g_{m1}R_1)$. From (4), by increasing the number of gain stage horizontally will also increase the gain of the PA. However, it also affects the rest of the PA performance such as linearity, efficiency, phase nonlinearity and etc.

IV. PHASE NONLINEARITY ANALYSIS

Phase nonlinearity i.e., group delay is the phase derivation of the transfer function with respect to angular frequency (5),

$$G_d = -\frac{\partial\theta\,(\omega)}{\partial\omega} \tag{5}$$

where θ is the phase delay and as a function for transfer function. The performance of overall transfer function H(s) is carefully considered because of the CMOS has high parasitic capacitance in drain. Analyzing overall circuit of group delay is very complicated task, hence to simplify the transfer function some parameters can be assumed as below:

i. $R_1 >> R_2$
ii. $1 - R_2 gm_1 \approx -R_2 gm_1$

From Equation (4), the overall transfer function, H(s) based on the assumption above can be expressed and approximated as Equation (6).

$$\begin{aligned} H(s) &= \frac{A_1(sL_2R_1 + R_1R_2)(sL_4 + R_3)}{s^3L_1L_2C_{gs1} + (L_1L_2g_{m1} + L_1C_{gs1}R_1)s^2 + (L_1 + L_2)s + R_1} \\ &= \frac{\left(\frac{s}{\omega_o}\right)^2 + \left(\frac{\omega_o}{Q}\right)s + R_1R_2R_3}{(\frac{s}{a})^3 b + (\frac{s}{a})^2 c + \frac{s}{a} + R_1} \end{aligned} \tag{6}$$

where $A_1 = g_{m1}g_{m2}$, $\omega_o = 1/\sqrt{L_2L_4R_1}$, $Q = 1/\sqrt{L_2L_4R_1}(L_2R_1R_3 + L_4R_1R_2)$, $a = 1/3L_1, b = 2C_{gs1}/27L_1$, $c = \frac{1}{9}(\frac{R_1C_{gs1}}{L_1} + 2g_{m1})$. From Equation (7), at ω_o=1 rad/s and Q = 0.577, two zeros in an imaginary part of the numerator causes/effects the phase nonlinearity peaking [21, 22] and the third order polynomial of the denominator consists of real pole $s_1=\sigma_1$ and two complex poles $s_2, s_3 = \sigma_2 \pm j\omega_2$. The phase nonlinearity performance for overall transfer function H(s) can be derived as in Equation (7) and (8), respectively.

$$G_d(\omega) = \frac{\partial\theta(\omega)}{\partial\omega}_{numerator} - \frac{\partial\theta(\omega)}{\partial\omega}_{denominator} \tag{7}$$

$$\begin{aligned} G_d = &\frac{Q\omega^5R_1R_2R_3}{Q^2R_1^2R_2^2R_3^2\omega_2^4 - 2Q^2R_1R_2R_3\omega_2^2\omega + Q^2\omega^2 + \omega_o^6\omega^2} \\ &- \frac{a(a^4R_1 + a^2\omega^2c - 3\omega^2a^2bR_1 + \omega^4ac^2)}{a^6R_1^2 - 2a^4R_1\omega^2c + a^2\omega^4c^2 + \omega^2a^4 - 2\omega^4a^2b + \omega^6b^2} \end{aligned} \tag{8}$$

Low phase nonlinearity can be obtained when the phase nonlinearity value at the denominator has large value as expressed in Equation (7). Equation (8) shows that by decreasing the value of a is the best way to obtain low phase nonlinearity. When the value of inductor L_1 is increased as much as possible it will give smallest phase nonlinearity due to the value of a is inverse proportional to L_1. However, increase of L_1 worsens the input matching of 50 ohm and declines the gain of the proposed PA. Hence, optimization of L_1 is conducted to meet the UWB requirement of desired input matching, gain, and phase nonlinearity. Figure 5 shows the simulation result of L_1 towards group delay variation. It clearly can be seen that increasing of L_1 will decreasing of the phase nonlinearity as proof in equation (8). Therefore, the inductance of L_1 at the input matching stage plays vital role in minimizing phase nonlinearity. Furthermore, the phasenonlinearity analysis play important role to determine dominant factor in UWB PA.

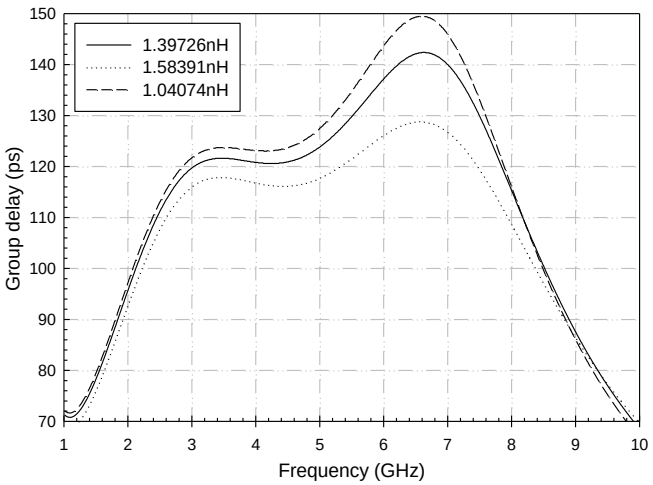

Figure 5: Effect of inductor, L1 on the group delay variation.

V. LINEARITY

Linearity is one of PA design specifications in UWB transmitter. Typically, good linearity can be achieved by deteriorating the gain and power consumption. Volterra's series can be used to analyze the output voltage of the transistor as expressed in Equation (9),

$$V_{out} = A_1(s)V_{in} + A_2(s_1, s_2) \circ V_{in}^2 + A_3(s_1, s_2, s_3) \circ V_{in}^3 + \cdots \tag{9}$$

where A_1 is the linear gain term and A_2, A_3 are the nonlinear gains. Two tone signals which are closely space frequency and equally in amplitude amplitude i.e. input third order intercept point (IIP3) produced the third-order intermodulation distortion as a result from nonlinearity of the transistor. The overall IIP3 for PA design can be obtained [24] and expressed in Equation (10):

$$\frac{1}{IIP3_T^2} = \frac{1}{IIP3_1^2} + \sum_{i=3}^{n} \frac{\prod_{k=1}^{i-1} G_i^2}{IIP3_i^2} \approx \frac{1}{IIP3_1^2} + \frac{G_1^2G_2^2}{IIP3_2^2} \tag{10}$$

where $IIP3_i$ and G_i is IIP3 and the gain for every stage i.e., stage 1 and stage 2. Equation (10) shows that the gain and IIP3 is much related to each other and will be trade-off between gain and IIP3. Therefore, the proposed PA is optimized to obtain good linearity and high gain. Also, the linearity can be realized by biasing at a gate-source voltage (V_{GS}) to zero.

VI. MEASUREMENT RESULTS

The implementation of the proposed PA was designed using 0.18µm CMOS technology with power supply of 1.8V. The proposed PA micrograph chip is shown in Figure 6. The size of the chip is 0.86 mm x 0.78mm. CADENCE SpectreRF simulator was used to simulate and calculate the result of the proposed PA circuit.

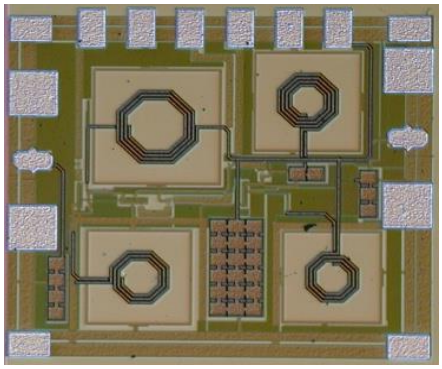

Figure 6: The proposed PA micrograph chip (0.88mm x0.78mm)

Figure 7 is the post layout simulation and measurement of S-parameters. It shows that the average gain measurement is 10 ± 1 dB at frequency of 3.1 to 6 GHz. There is 2 dB differences between simulated and measured gain because of losses in parasitic elements and testing board. Broadband input and output matching of < -6 dB and <-11 dB, respectively. As shown in Figure 8, it can be seen that the reverse isolation is -29 dB from 3.1 to 6 GHz indicates that high reverse isolation S_{12} that avoiding LO leakage signal receive to antenna. The Stern stability factor (K-factor) expression as defined [25] often used to characterize the stability of PA. In Figure 9, it is clearly that the PA in stable mode where oscillate does not occur with load impedance and source from 1 to 8 GHz. As illustrated in Figure 9, it shows that phase nonlinearity i.e., group delay variation of ±195.5 ps is attained. This means that the output retain its original identity and appropriate for UWB system application. The measurement result of input 1dB compression point i.e., IP1dB is shown in Figure 11. A good linearity, IP1dB of -6dBm and -5 dBm are obtained at 4 GHz and 5 GHz, respectively. Figure 12 illustrates the measurement of IIP3. The IIP3 measurement of 5 dBm at 5 GHz is achieved. The measurement result of power added efficiency (PAE) is depicted in Fig 13. At P1dB, the PA has PAE of 15.5%. Furthermore, the proposed PA consumes power consumption of 30 mW.

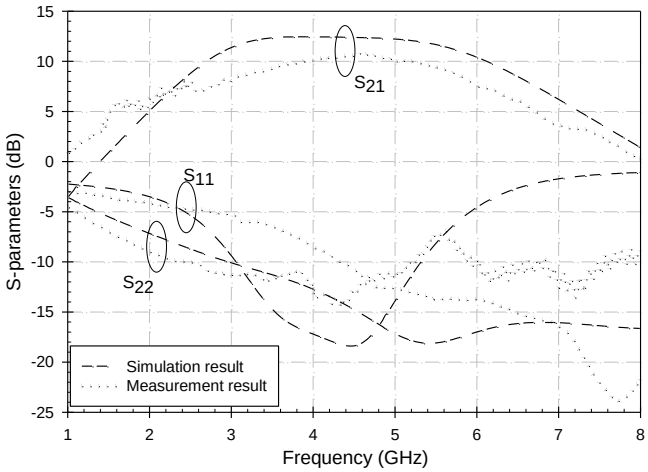

Figure 7: Measurement and simulation of S-parameters

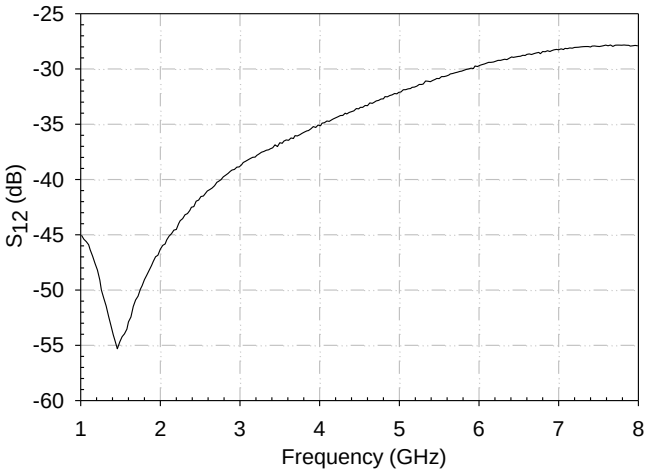

Figure 8: Measurement of reverse isolation (S_{12})

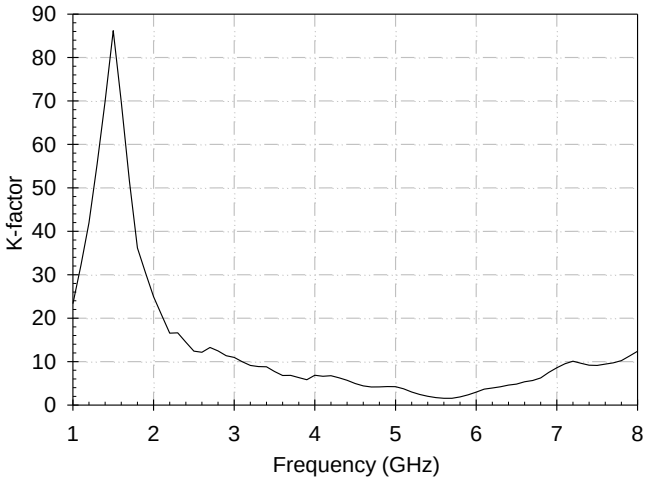

Figure 9: Measurement of stability factor (K-factor)

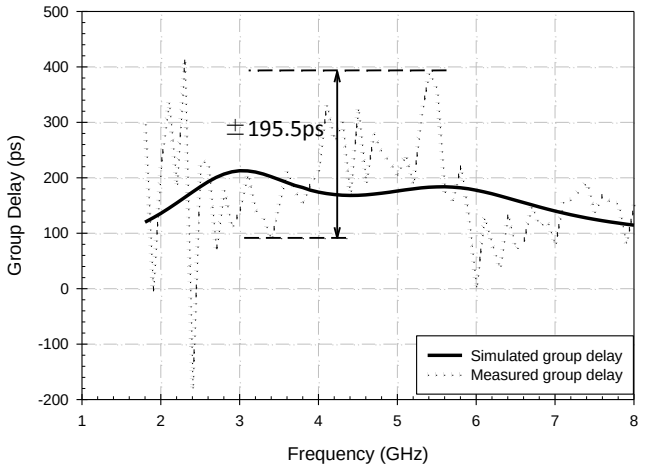

Figure 10: Measurement and simulation of group delay versus frequency

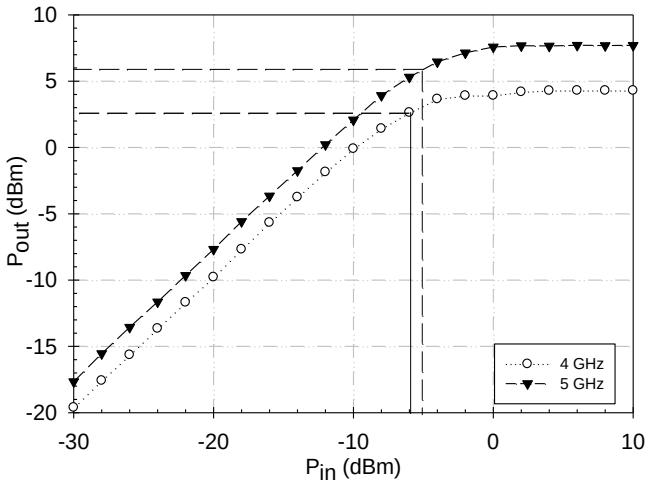

Figure 11: Measurement of P1dB

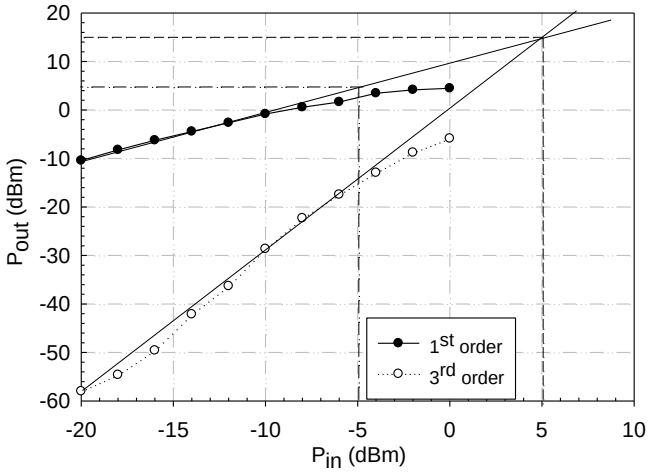

Figure 12: Measurement of IIP3

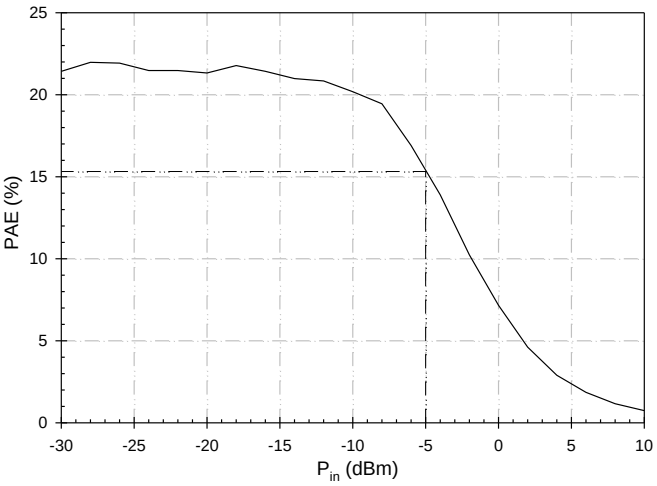

Figure 13: Measurement of PAE

The performance of other published papers on UWB CMOS PAs is shown in Table 1. It shows that the overall performances of proposed PA design are almost similar to [10], [16] and [26], which has achieved good gain, linearity, low phase nonlinearity and small chip area. The proposed PA is very appropriate for Group 1-2 of MB-OFDM UWB system.

Table 1
Performance of UWB CMOS PA

Ref	[7]	[10]	[21]	[16]	[26]	[27]	This work
CMOS technology	0.18	0.18	0.18	0.18	0.18	0.18	0.18
Frequency (GHz)	2.6-5.4	3.0-6.2	3.0-7.0	3.0-10	3.1-4.8	3.0-5.0	3.1-6.0
OP_{1dB} (dBm)	11.4	-5	7.0	5.6	8	6.6	5.8
Gain (dB)	15.8	11 ±0.6	14.5 ±0.5	10.46 ±0.8	10.3 ±0.8	16 ±0.5	10 ±1
S_{11} (dB)	<-5	<-14	<-6	<-10	<-5	<-11	<-6
S_{22} (dB)	<-6	<-12	<-7	<-10	<-8	<-8.5	<-7
Power (mW)	25	13	24	84	24	23.2	30
PAE (%)	34	N/A	N/A	N/A	40.5	16.4	15.5
Group Delay (ps)	N/A	N/A	±178.5	±250	±135	N/A	±195.5
Area (mm^2)	1.65	0.69	0.88	1.76	0.97	0.75	0.67

VII. CONCLUSION

The group delay variation, gain and linearity of a 3.1 to 6.0 GHz UWB CMOS PA using two-stage amplifier with shunt resistive feedback technique has been analyzed. It is found that high inductance at the input matching network can obtain low group delay variation. This implies that the key performance factors of minimum low group delay can be applied to facilitate other researchers working in the area of power amplifier circuit design. It is recommended that a mathematical modeling is introduced so that it can be applied to all topologies in UWB power amplifier.

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