CMOS Power Amplifier Design Techniques for UWB Communication: A Review

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***Abstract*—This paper reviews CMOS power amplifier (PA) design techniques in favour of ultra-wideband (UWB) application. The PA circuit design is amongst the most difficult delegation in developing the UWB transmitter due to conditions that must be achieved, including high gain, good input and output matching, efficiency, linearity, low group delay and low power consumption. In order to meet these requirements, many researchers came up with different techniques. Among the techniques used are distributed amplifiers, resistive shunt feedback, RLC matching, shunt-shunt feedback, inductive source degeneration, current reuse, shunt peaking, and stagger tuning. Therefore, problems and limitation of UWB CMOS PA and circuit topology are reviewed. A number of works on the UWB CMOS PA from the year 2004 to 2016 are reviewed in this paper. In recent developments, UWB CMOS PA are analysed, hence imparting a comparison of performance criteria based on several different topologies.**

***Index Terms*—Power Amplifier; Ultra-Wideband; CMOS; Techniques; Performance Criteria.**

I. INTRODUCTION

The emergence of UWB technology requires the transceiver to be wide-ranged in frequency, high data rate, and low power. PA is one of the components in the transmitter that is very difficult to design because it is the hungriest block that consume high power compared to other components. Furthermore, the critical part in designing CMOS PA in UWB technology is to achieve good linearity, high flat gain, low power use, and broadband input as well as output matching over wide band frequency from 3.1-10.6 GHz.

A number of CMOS PA designs for UWB application have been proposed with different techniques: distributed amplifier [1]–[2], resistive shunt feedback [3]–[6], RLC matching [7], shunt-shunt feedback [8]–[9], shunt peaking [8], [10], inductive source degeneration [11]–[12], inter-stage wideband transformer [13], current reuse [14]–[15], and lastly, stagger tuning [16]–[17]. The distributed amplifier can be used to achieve wideband matching in PA design, but it has high power consumption and large area of the chip. Resistive shunt feedback is one of wideband matching techniques that provides proper input and output matching. This technique offers smaller chip area compared to others technique since it utilises less to no inductor [18]. The RLC matching technique reduces power consumption and poses wideband matching, though large die area is required attributable to an amount of reactive elements to make a band pass filter [9]. Shunt-shunt feedback also provides proper input and output wideband matching. Shunt peaking is generally used for wideband matching technique. However, the results shown from a previous shunt peaking technique observes that this technique does not actually help to obtain proper input and output matching. Inductive source degeneration provides good input wideband matching and improves the linearity, however it can reduce the gain of the amplifier. Another technique is inter-stage wideband transformer that is used to provide high wideband impedance to reduce the power dissipation.

Unfortunately, this technique limits the gain and has poor wideband matching. Current-reused technique is employed in order to reduce sensitivity of the power gain and input impedance to parasitic, temperature and process variations [19]. It is also used to improve the gain flatness. A recent technique in PA, which is stagger-tuning usually consists of two or more stages and each stage tuned to a slightly different frequency. The advantage of this technique is its ability to obtain wider gain bandwidth.

II. UWB PA DESIGN TECHNIQUES

The UWB PA design is a taxing assignment because it must accomplish several constraints such as gain flatness, group delay, linearity, power consumption, power added efficiency, input and output matching over wide frequency. The selection of the techniques applied varies on the requirement of the power amplifier design for UWB application.

A. Distributed Amplifier

In 2004, [1] proposed four stages distributed amplifier technique in PA design for UWB as shown in Figure 1. In this technique, the transistor is separated into stages, which is linked by customised transmission lines in order to conjoin the transfer function of the required frequency behaviour. The transfer function on a whole is designed for greater bandwidth in relation to the ratio along with number of stages, as well as the impedance and the span of the transmission lines. The result shows high gain of 17 dB and output return loss, S_{22} is under -5 dB untilf_{3dB}, and until f= 6 GHz is below -10 dB. However, high power consumption of 100mW due to a vertical finger capacitance used in this design is measured, which contributes to large parasitic capacitance. The parasitic can be reduced by replacing the capacitance with metal insulator metal (MIM) capacitance that enhances the operation.

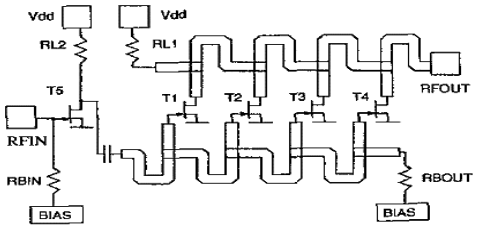

Figure 1: Block diagram of the four stage distributed amplifier and the non-distributed input stage [1].

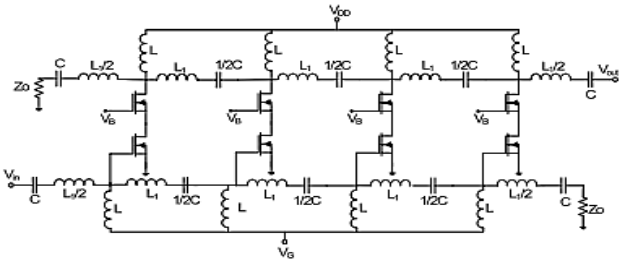

Figure 2: Schematic of the distributed amplifier topology with a wide band-pass artificial transmission line [2].

Later in 2006, [2] proposed dispersed amplifier topology with a wide band-pass artificial transmission line as shown in Figure 2. Four inductors are used as biasing to remove the implementation of large inductance chokes, that are broad frequently applied by mean of off-chip bias tees [1]. By employing this topology, some subjects associated to conventional distributed amplifiers, whereas electro migration and biasing can be resolved. Both input and output return loss is below -10 dB for 50 Ω input and output matching. The average gain and power consumption are 10.46±0.8 dB and 84 mW, respectively. The disadvantage of distributed amplifier is high power consumption related to the distribution of multiple amplifying stages, thus making them inapt for low power purposes.

B. Resistive Shunt Feedback

Resistive shunt feedback presented in Figure 3 is a popular technique to provide good wideband matching in PA designs [3] for UWB. [3] presents a low power CMOS PA for UWB application. In this design, RC feedback network is used as wideband matching techniques, as well as to obtain flat gain, which displayed in Figure 4. The input stage is proposed using separate PAs for each single ended input. It is used to relax the required gain and linearity on each of these PAs in comparison to utilising a lone PA. The simulation result shows high gain of 19±1 dB, input matching and output matching is under -10 dB and -8 dB correspondingly, whilst consuming power of 25 mW.

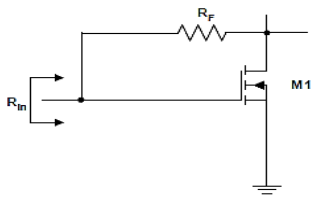

Figure 3: Resistive shunt feedback [3]

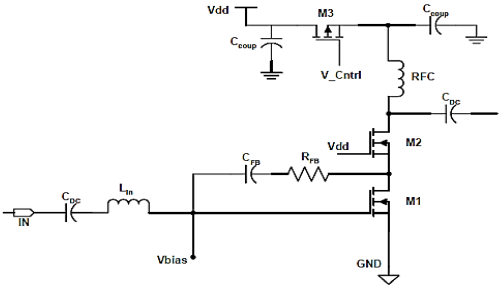

Figure 4: Schematic of the input stage of PA [3].

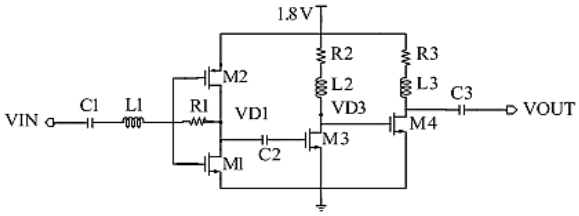

Figure 5: Schematic of the proposed PA core [4]

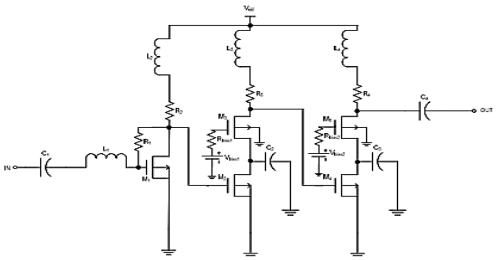

Figure 6: Schematic of the proposed PA [6].

[4] proposed high frequency UWB PA for China's UWB standard with resistive feedback complementary amplifying topology as shown in Figure 5. The bandwidth could be expanded to cover from 6 to 9 GHz with appropriate feedback resistor, R_1. This technique reduces the chip area since it uses less inductors compared to the conventional band-pass filter input matching topology. This paper achieved average gain of 10±0.6 dB, and consumes 21 mW. The measurement result shows the suggested UWB PA has gained excellent wideband matching, good input and output matching of < -10 dB and <-35 dB, respectively.

[6] Proposed a low power 3.1 - 10.6 GHz UWB PA with resistive shunt feedback technique. Figure 6 shows the suggested design of UWB PA consisting of a two-stage amplifier with resistive shunt feedback and output buffer. Resistive shunt feedback method is within the first stage with common source (CS) topology to provide high gain, larger bandwidth and achieve flat gain. The simulation results of average gain, input matching, output matching, and power consumption are 12±1.1 dB, <-8.6 dB, <-8.6 dB and 19 mW, respectively. The suggested UWB PA also acquires good group delay of ±18.3 dB, stating that the derived group delay in regard to angular frequency is especially near to zero.

Resistive shunt feedback also is used in [5], [14], [16], [20]–[24] to obtain proper wideband matching. This technique gives good stability and good gain flatness [6] to the PA. However, as a result of the high dependency of voltage gain on the transconductance of the amplifying transistor, high current in the CMOS is expected.

C. RLC Matching

RLC matching provides good input and output matching alongside low power dissipation, but large area is required seeing as the amount of reactive elements is used to create band-pass filter [9]. [7] proposed PA with an enhanced RLC filter and multilevel RLC matching attaining the wideband input and output matching as shown in Figure 7. Resistance R2, capacitance C10, parasitic capacitance C11, and bondwire L8 are employed to develop a wideband multilevel output matching network. Inductance L7 and capacitance C9 are also an inclusion of the outmatching network, where L7 is the load of the cascade amplifier and C9 is the coupling capacitance [7]. In this paper, the proposed PA manages to get low die area of 1.1 mm2 by lessening the numbers of inductors and input and output matching are <-9 dB as well as <-8 dB, respectively whilst consuming 25.2 mW. However, the gain obtained is not very good, i.e., 8±2 dB.

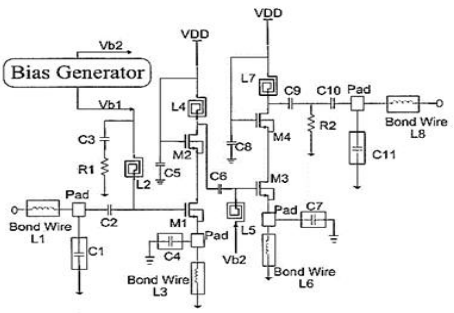

Figure 7: Schematic of the proposed UWB PA [7].

D. Shunt-shunt Feedback

Another wideband matching approach is shunt-shunt feedback [25]. Figure 8 shows the combination of the shunt-shunt feedback with resistive shunt feedback [21]. To improve the bandwidth alongside wideband output matching, the shunt-shunt feedback for the resistance, R4 and capacitance, C5 is operated at the output stage, whereas the utilisation of resistive shunt feedback helps achieving flat gain. [8] applied shunt-shunt feedback technique in their proposed PA as shown in Figure 9. As can be seen, shunt-shunt feedback is employed in both two stages of the cascoded amplifiers. It can enhance the input and output matching of the circuit. Shunt peaking technique and three-stage LC ladder matching network also applied in this proposed PA. The measured results obtain high gain of 19.25±1.75 dB. Both the return loss at the input and output is below-10 dB, on top of the frequency ranging from 3.1 to 4.8 GHz, showing that the shunt-shunt feedback can achieve proper wideband matching.

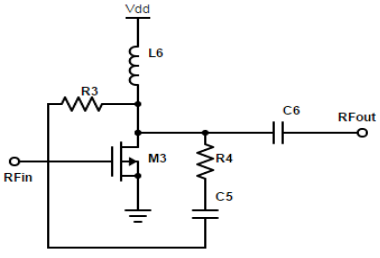

Figure 8: Shunt-shunt feedback and resistive feedback at the output stage

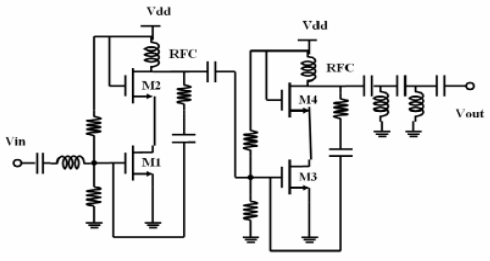

Figure 9: Schematic of proposed UWB PA [8].

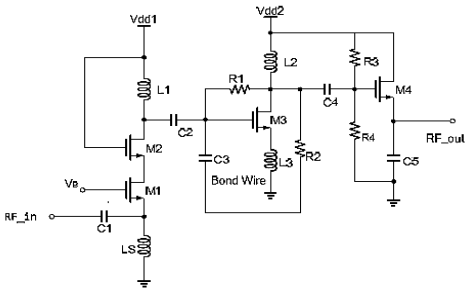

Figure 10: Schematic of the proposed UWB PA [9].

[9] proposes low power of 3.0 to 6.2 GHz CMOS PA for implanted biomedical UWB communication system. The proposed PA as shown in Figure 10 employs RC shunt-shunt feedback and bond-wire inductor source degeneration in the second stage to improve the bandwidth and linearity. In addition, common-gate (CG) circuit at the input stage and source follower at the output stage are used for impedance matching. The simulation results obtain average gain of 11±0.6 dB and input-matching is <-14 dB, whilst output-matching is<-12 dB. The small power consumption of 13 mW is achieved. However, the large area chip size is obtained because of the usage of bonding wire in the PA.

The shunt-shunt feedback technique is also applied in [21], [22]. However, high group delay of ±137.7 ps [21] and ±178.5 ps [22] are obtained, causing signal distortion in PA. This indicates that the output fails to maintain its initial identity with the PA of high group delay. This problem can be solved by determining the factors that affect the group delay and applying others technique that can minimise the group delay.

E. Shunt Peaking

Wideband matching also can be achieved by using a shunt peaking technique as shown in Figure 11. This procedure includes inductance, L and resistance, R which are connected in series, altering the frequency response of the amplifier. This presents a transfer function of zero-point, then increasing gain at the high-frequency edge of the bandwidth [8]. [24] presents a design of 3.1 - 6.0 GHz CMOS PA in lieu of UWB applications, as shown in Figure 12. As can be seen, the shunt peaking load techniques are L_2, L_4, R_2, as well as R_3. This technique is applied in both the first and the second stages to improve the gain, group delay variation and linearity. A resistive shunt feedback method is also operated in stage one of the suggested PA. The measured result obtains average gain of 10±1 dB, input and output matching are <-6 dB and <-7 dB, respectively. However, the high group delay variation of ±195.5 dB is obtained.

[23] presents the design of 0.9 - 4.8 GHz CMOS PA in favour of UWB transmitters, as shown in Figure 13. This

proposed PA applies a two-stage cascade CS topology, a resistive shunt feedback technique and inductive peaking. This is for the purpose of obtaining high gain flatness and good input matching. The inductor, L_2 is utilised as inductive peaking, with a purpose of counter weighing the bandwidth limitation. It also helps to improve the gain flatness in the high frequency region. The measured result obtains average gain about 10.2±0.8 dB, whereas the input-matching and output-matching are <-4.4 dB and <-9.2 dB, whilst consuming 30 mW. Moreover, the group delay of ±124 dB is obtained.

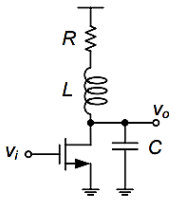

Figure 11: A CS amplifier with a shunt peaking load

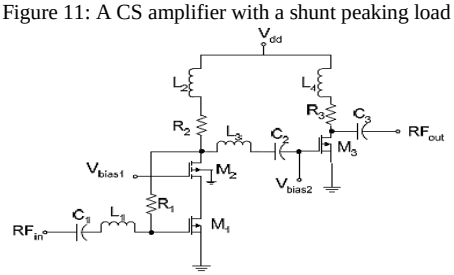

Figure 12: Schematic of the proposed UWB PA [24].

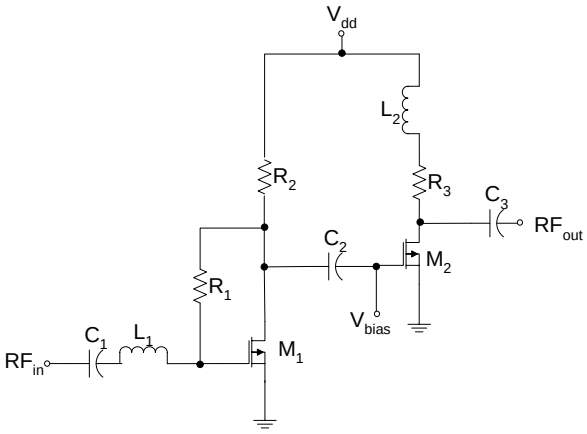

Figure 13: Schematic of the proposed UWB PA [23].

Shunt peaking technique is also used in [6], [8], [26]–[30] as a wideband matching technique in their proposed PAs design. Through all the proposed UWB PA design that uses this technique, the result shows that this technique does not actually help to obtain proper input and output matching.

F. Inductive Source Degeneration

Inductive source degeneration as shown in Figure 14 is often employed in RF design to improve linearity and stability of the amplifier [28]. [20] suggested the model and application of a single-stage and double-stage inductive, disintegrated with resistive shunt feedback PA for UWB as shown in Figure 15. The single-stage PA obtained an average gain of 8.95±1.45 dB, and the input-matching and output-matching are <-4.5 dB and <-5.8 respectively. The cascaded double-stage PA obtained an average gain of 14.45±1.05 dB, and the input-matching and output-matching are <-1.4 dB and <-1.9 dB respectively. Lastly, the cascoded double-stage PA obtained an average gain of 23.9±1.6 dB, and the input-matching and output-matching are <-4.6 dB and <-1.3 dB respectively. These three proposed PA designs show high gain, but very poor wideband matching. The target input and output matching for UWB applications must be less than or equal to -10 dB. Beneficially, these PA designs can serve as reference to forthcoming UWB PAs design.

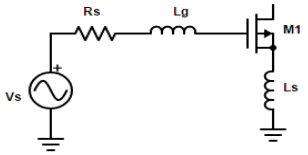

Figure 14: Example of inductive source degeneration technique.

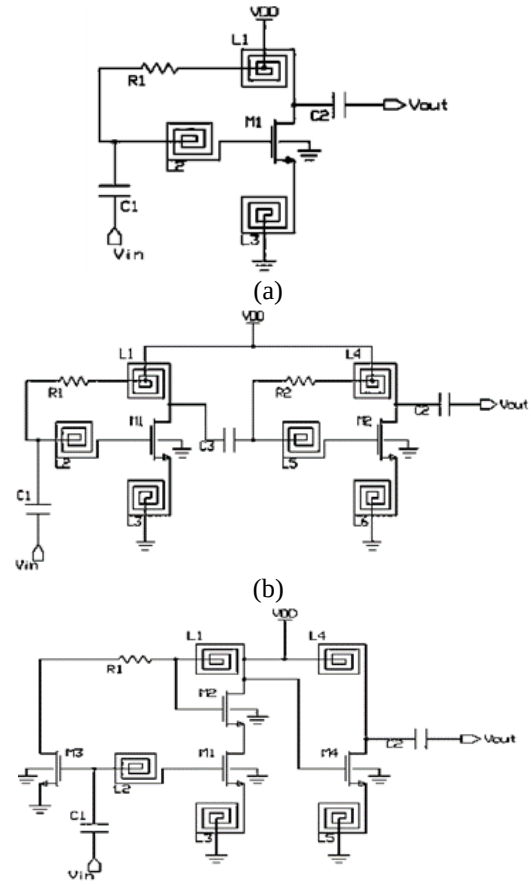

Figure 15: (a) Single-stage UWB PA (b)Double-stage cascaded UWB PA (c)Double-stage cascoded PA [20]

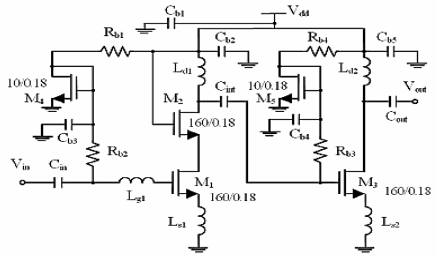

Figure 16: Schematic of the proposed UWB PA [11].

[11] also applied inductive source degeneration in the suggested PA design as illustrated in Figure 16. As can be

seen, L_{s1} is the source degeneration inductor that enhances the stability and linearity, whilst$L_{g1}$is used in the impedance matching amidst the source impedance and transistor,M_1 input. The result shows that high gain of 15.2± 0.6 over frequency ranging between 2.6 and 5.4 GHz is achieved. The input-matching and output-matching are less than -5 dB and -6 dB, correspondingly.

The inductive source degeneration is also used in [9], [14], [15], [28], [30]. All the proposed PAs design using this technique have problems in achieving good input and output matching.

G. Inter-stage Wideband Transformer

[13] presents a 6 - 10 GHz CMOS PA for UWB transmitter as shown in Figure 17. For the wideband operation, an inter-stage wideband impedance transformer is assembled in the middle of the small-signal stage and driver amplifier. It offers high wideband impedance to reduce the consumption of power in the first stage. The resistance R_1 is in series with inductance L_1in order to lower the high reactance of approximately 8 GHz to a proper level. The corresponding resistance and reactance is expressed as (1):

$$R_{shunt} = \frac{L_1}{C_1}, \frac{1}{R_1}; X_{shunt} = -\frac{1}{\omega C_1} \quad (1)$$

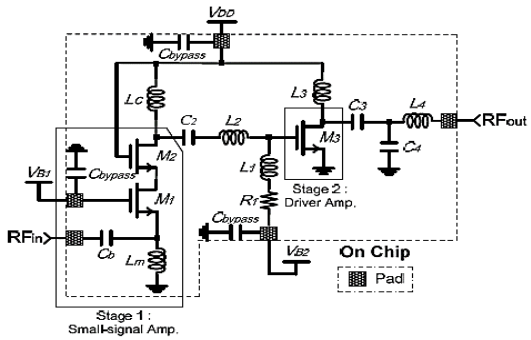

Figure 17: Schematic of the proposed UWB PA [13].

From (3), the values for resistance and reactance are varied to ones that are limited by the passive components of R_1, L_1, and C_1. The normalised resistance and reactance are cut significantly around the frequency offset of 1 GHz of the central frequency by adding the resistance R_1. The calculated outcome of the average gain is 8.5 dB above the frequency ranging between 6.0 and 10.6 GHz, whereas the input-matching and output-matching are <-7 dB and <-4 dB, whilst consuming 18 mW. The result of proposed PA shows that this technique limits the gain, and has poor wideband matching.

H. Current Reuse

Current reuse is one of the most used technique in UWB amplifier designs because it can improve gain flatness and achieve low power use [31]. The design between 3.1 and 4.8 GHz CMOS PA for UWB applications is presented by [14] as shown in Figure 18. Cascode topology and a current-reused method are employed together in the suggested UWB PA,with the purpose of increasing the gain of the top end of the required band. This UWB PA obtained a gain about 10.3± 0.8 dB and high group delay roughly ±135 ps. The input and output matching are <-5 and <-8 respectively. The performance of group delay and wideband matching should be improved.

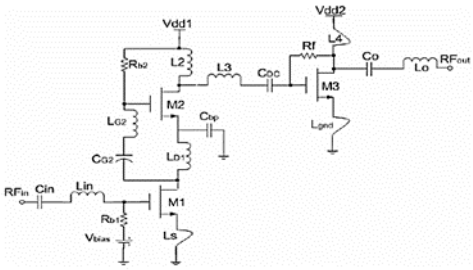

Figure 18:Schematic of the proposed UWB PA [14].

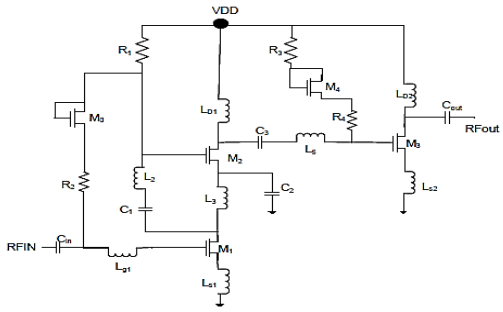

Figure 19: Schematic of the proposed UWB PA [15].

[15] uses the current reuse technique in the suggested UWB PA, illustrated in Figure 19. In this design, the inductive source degeneration is chosen as input wideband matching technique. The outcome of the simulation demonstrates that the suggested PA design has a high gain about 16±0.4 dB, alongside low group delay variation of ±20 ps, whilst consuming 25 mW. The input and output matching are <-4 dB and <-5 dB respectively. The result shows that this technique can reach high gain and excellent gain flatness, at the same time contributes to low group delay. However, poor wideband matching is obtained.

Furthermore, the current reuse technique indeed helpful to reduce power consumption and to obtain gain flatness in [17], [21], [22], [26], [27]. However, it has difficulty of reaching wide range frequency band between 3.1 and 10.6 GHz [6].

I. Stagger Tuning

Stagger tuning technique is a multi-stage amplifiers, in which each stage is tuned to a different frequency so as to attain good gain flatness, whilst at the same time to provide a broad bandwidth characteristic [32]. [16] applied this technique in the UWB PA design as shown in Figure 20 and achieves good gain flatness about 11.48±0.6 dB. The good input-matching and output-matching of <-10 dB to<-14 dB are also achieved. Also, good group delay of ±85.8 ps is achieved. However, cascade topology used in this design consumes high power of 100 mW.

[17] proposed two-stage cascaded PA by stagger tuning technique, as shown in Figure 21. The wide bandwidth is realised by using different centre frequencies in each gain stage, by which the stage one obtains a tuning frequency of 6.5 GHz whereas and the stage two 9.6 GHz. In addition, the current reuse method is also employed in the first stage of the PA design. The measured result shows the proposed design achieves high gain of 16±1 dB over 5 - 10.6 GHz. The input-matching and output-matching are <-5.5 dB and <-7 dB respectively. The suggested UWB PA attains good

group delay about ±40 ps.

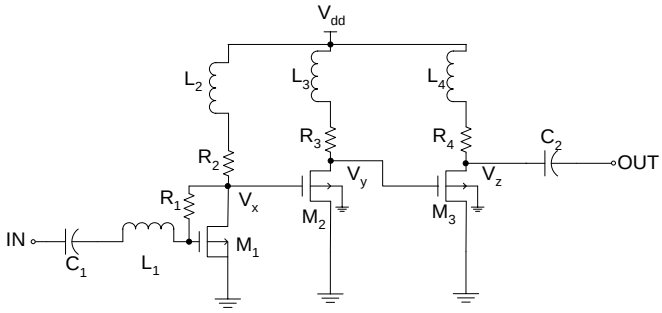

Figure 20: Schematic of the proposed UWB PA [16]

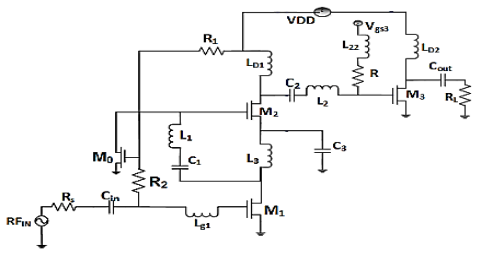

Figure 21: Schematic of the proposed UWB PA [17].

Another research by [33] employs stagger tuning technique to enhance the bandwidth. This design also incorporates current-reused and self-biasing for low power consumption and linearity, respectively. The simulation outcome gives good result for all parameters except that the value of the power consumption is not mentioned at all. Also in this research, it mentions about the noise figure which is not a design parameter for power amplifier.

J. Performance Summary

Table 1 sums up the performance of issued CMOS PAs design from 2004 to 2016 for UWB application. As can be seen, most of the UWB PA design meets the gain requirement of less than 10 dB, except the PA with RLC matching [7], single-stage inductive degeneration [20], wideband impedance transformer [13] and resistive shunt feedback [5]. The high gain can also be achieved easily when the PA is designed for low frequency band such as [3], [8], [20], and [11]. However, it is difficult to meet UWB requirements for PA which covers full frequency ranging from 3.1 to 10.6 GHz, for instance these previous four works; [2], [7], [16] and [6], since it has wider bandwidth. Amongst these four works, the UWB PA with distributed amplifier [2] and stagger tuning [6] achieve good gain and wideband matching, but it consumes high power which is not suitable for low power UWB applications.

Furthermore, most of the works fail to meet the required return loss requirement of less than -10 dB at both the input as well as the output, which indicates the wideband matching of the PA. It is important to choose the right input and output matching technique or networks based on the required frequency range to achieve proper wideband matching. Apart from these UWB PAs, the most excellent UWB PAs design so far which meets the overall UWB requirements are [4], [27], and [9]. They achieve good gain, as well as input and output matching, low power consumption and low group delay.

Over the past decade, PA mostly used expensive technology, for example, Silicon Germanium (SiGe) or Gallium Arsenide (GaAs) to be realised in transmitter. During that time, the PA was not achievable in CMOS technology due to its limitation. With the increasing of CMOS technology used in cellular phones and millions of devices that are developed and marketed at monthly intervals, it becomes a motivation to all researchers to investigate and demonstrate new topology and architecture that are different from the PA topologies as summarised in Table 1. However, based from the data obtained, it is found that the usage of CMOS power amplifier still has its limitation that needs to be improved and strengthened in the future PA topology, especially in UWB system. Firstly, the CMOS PA have been studied intensively, however the question of which PA topologies is the best topology for UWB system still has not been resolved. The result shows that there is trade-off between the characteristics, and difficult to achieve all design specifications over wide frequency spectrum.

Secondly, many studies have shown great effort and achievement, but several characteristic shortcomings of the CMOS, such as lower f_T of transistors that has not been discussed in detail before, causes the UWB circuits design in CMOS enormously challenging indeed.

Lastly, not many studies have shown the result of group delay variation analysis. Group delay variation is one of the important criteria for linearity in order to have the output retains its original identity. The gain, efficiency and wide frequency bandwidth in CMOS power amplifier are difficult to be complied with, mainly because it has the inclination to fail the group delay variation. The mathematical models that have been established are not suitable for ultra-wideband application in CMOS power amplifier, due to the limitation of the bandwidth frequency. Therefore, mathematical modelling is required to investigate key performance factor of group delay variation to achieve low group delay variation.

III. CONCLUSION

A review CMOS power amplifier design techniques for UWB application has been discussed. Several approaches UWB PAs have been implemented for frequencies of 3.0–5.0 GHz, 3.0-6.0, 3.0–7.0 GHz, 5.0–10 GHz, 6.0–10.0 GHz and 3.1–10.6 GHz with different kind of topologies. The performance of the UWB CMOS PA depends on the selection of the techniques and requirement of UWB applications. Current publish has achieved very good PA performance in UWB application. This review hopefully can help to facilitate other researchers working in the area of power amplifier circuit design.

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Table 1
Performance summary and comparison of UWB CMOS PAS

Ref. & Year	Techniques	Frequency (GHz)	Gain (dB)	|S11| (dB)	|S22| (dB)	Power (mW)	Group delay (ps)	Area (mm^2)	Measured/ Simulation Result
[1] 2004	Distributed amplifier	2.0-8.0	17	N/A	-5	100	N/A	N/A	Measured
[3] 2005	Resistive shunt feedback	3.1-4.8	19±1	<-10	<-8	25	N/A	2.09	Simulation
[2] 2006	Distributed amplifier	3.0-12.6	10.46±0.8	<-10	<-10	84	N/A	1.76	Measured
[7] 2006	Multilevel RLC matching & improved wideband RLC filter	3.1-10.6	8±2	<-9	<-8	25.2	N/A	1.1	Measured
[8] 2006	Shunt-shunt feedback, shunt peaking, 3-stage LC ladder network	3.1-4.8	19.25±1.75	<-10	<-10	N/A	N/A	1.52	Measured
[20] 2007	Single stage inductive degeneration	3.1-4.8	8.95±1.45	<-4.5	<-5.8	23	N/A	N/A	Simulation
	Cascaded wideband inductive degeneration	3.1-4.8	14.45±1.05	<-1.4	<-1.9	35.5	N/A	N/A	Simulation
	Cascoded wideband inductive degeneration & resistive feedback	3.1-4.8	23.9±1.6	<-4.6	<-1.3	26.7	N/A	N/A	Simulation
[13] 2008	Wideband impedance transformer	6.0-10.0	8.5	<-7	<-4	18	N/A	1.08	Measured
[11] 2009	Inductive source degeneration	2.6-5.4	15.2±0.6	<-5	<-6	25	N/A	1.65	Measured
[21] 2009	Current reuse, shunt-shunt feedback, & resistive shunt feedback	3.0-7.5	10	<-5	<-7	15	±137.7	0.88	Simulation
[4] 2010	Resistive feedback complementary amplifying topology	6.0-9.0	10±0.6	<-10	<-35	21	N/A	0.88	Measured
[14] 2010	Current reuse, inductive source degeneration, & resistive shunt feedback	3.1-4.8	10.3±0.8	<-5	<-8	24	±135	0.97	Measured
[22] 2010	Current reuse, shunt-shunt feedback, & resistive shunt feedback	3.0-7.0	14.5±0.5	<-6	<-7	24	±178.5	0.88	Measured
[5] 2010	Resistive shunt feedback	3.0-5.0	9.1±0.4	<-15	NA	14.4	±8	0.84	Measured
[35] 2010	Series transformer matched /stack	1-5	15-20	<-10	<5	N/A	N/A	0.68	Measured
[36] 2010	Transfomer-based high order output matching network	5.2-13	18.5	<-10	<-4	N/A	±20	0.70	Measured
[26] 2011	Current reuse & shunt peaking	6.0-10.6	11±1	<-8	<-11	18	±55.6	0.77	Simulation
[24] 2011	Resistive shunt feedback & shunt peaking	3.1-6.0	10±1	<-6	<-7	30	±195.5	0.67	Measured
[27] 2011	Current reuse & shunt peaking	3.1-7.5	11.4±0.8	<-11.1	<-10.5	14.5	±67.1	0.95	Simulation
[28] 2012	Inductive source degeneration & shunt peaking	3.0-7.9	18.8	<-2	<-6.6	30	N/A	NA	Simulation
[9] 2012	Source-follower, RC shunt-shunt feedback, bondwire inductor source degeneration	3.0-6.2	11±0.6	<-14	<-12	13	N/A	0.69	Simulation
[16] 2012	Stagger tuning & resistive shunt feedback	3.1-10.6	11.48±0.6	<-10	<-14	100	±85.8	0.69	Measured
[29] 2012	Current reuse & shunt peaking	5.0-11.0	11.5±0.4	<-10.4	<-9.5	17	±41	0.96	Simulation
[23] 2012	Resistive shunt feedback & shunt peaking	0.9-4.8	10.2±0.8	<-4.4	<-9.2	30	±124	0.55	Measured
[15] 2013	Current reuse & inductive source degeneration	5.0-9.0	16±0.4	<-4	<-5	25	±20	0.93	Simulation
[6] 2013	Resistive shunt feedback & shunt peaking	3.1-10.6	12.4±1.1	<-8.6	<-8.6	19	±18.3	0.95	Simulation
[30] 2014	Inductive source degeneration & shunt peaking	3.0-7.9	18.8	<-2	<-6.6	25.2	N/A	N/A	Simulation
[17] 2015	Current reuse & stagger tuning	5.0-10.6	14±1	<-5.5	<-7	20	±40	0.77	Measured
[34] 2015	Common drain with transformer-base input matching network	2.8-6	17.5	N/A	N/A	N/A	N/A	0.49	Measured
[33] 2016	Stagger tuning	3.1-10.6	18±0.2	<-10	<-8.4	N/A	±25	N/A	Simulation
[38] 2016	Differential	3-5	15.5±0.4	<-12.9	<-13.3	25.46	18.4	N/A	Simulation
[39] 2016	Current reuse	3.1-5.1	20.3±0.8	<-1.5	<-6	27.3	±121.3	N/A	Simulation

REFERENCES

[1] Grewing, C., Winterberg, K., Waasen, S., Friedrich, M., Puma, G. L., Wiesbauer, A., & Sandner, C. (2004). Fully integrated distributed power amplifier in CMOS technology, optimized for UWB transmitters. 2004 IEEE Radio Frequency Integrated Circuits (RFIC) Systems. 87–90.

[2] Lu, C., Pham, A.-V., & Shaw, M. (2006). A CMOS power amplifier for full-band UWBtransmitters. IEEE Radio Frequency Integrated Circuits (RFIC) Symposium. 1, 1–4.

[3] Jose, S., Lee, H.-J., Ha, D., & Choi, S. S. (2005). A low-power CMOS power amplifier for ultra wideband (UWB) applications. IEEE International Symposium on Circuits and Systems. 12–14.

[4] Zhendong, G., Zhiqiang, L., & Haiying, Z. (2010). A 6–9 GHz ultra-wideband CMOS PA for China's ultra wideband standard. Journal of Semiconductors. 31(9), 095008.

[5] Tianzuo, X., Lu, H., Zhong, Z., & Lisong, F. (2010). A 3–5 GHz CMOS UWB power amplifier with ±8 ps group delay ripple. Journal of Semiconductors. 31(4), 045005.

[6] Sapawi, R., Sahari, S. K., & Kipli, K. (2013). A low power 3.1-10.6 ghz ultra-wideband CMOS power amplifier with resistive shunt feedback technique. 2013 International Conference on Advanced Computer Science Applications and Technologies. 1, 3– 6.

[7] Hsu, H. C., Wang, Z. W., & Ma, G. K. (2006). A low power CMOS full-band UWB power amplifier using wideband RLC matching method. 2005 IEEE Conference on Electron Devices and Solid-State Circuits (EDSSC). 233–236.

[8] Wang, R., Su, Y. K., & Liu, C. H. (2006). 3~5 GHz cascoded UWB power amplifier. 2006 IEEE Asia Pacific Conference on Circuits and Systems. 367–369.

[9] Wang, L. Y., Li, B., & Wu, Z. H. (2012). A low power CMOS power amplifier for implanted biomedical ultra wideband (UWB) applications. IEEE 11th International Conference on Solid-State and Integrated Circuit Technology (ICSICT). 1–3.

[10] Meaamar, A. (2010). An ultra-wideband receiver front-end. Ph.D Thesis, The Nanyang Technological University, 2010.

[11] Wong, S. K., Maisurah, S., Osman, M. N., Kung, F., & See, J. H. (2009). High efficiency CMOS power amplifier for 3 to 5 ghz ultrawideband (UWB) application. IEEE Transactions on Consumer Electronics. 55(3), 1546–1550.

[12] Kim, M. G., & Yun, T. Y. (2014). Analysis and design of feedforward linearity-improved mixer using inductive source degeneration. IEEE Transactions on Microwave Theory and Techniques. 62(2), 323–331.

[13] Chung, H. W., Hsu, C. Y., Yang, C. Y., Wei, K. F., & Chuang, H. R. (2008). A 6-10-GHz CMOS power amplifier with an inter-stage wideband impedance transformer for UWB transmitters. Proceedings of the 38th European Microwave Conference (EuMC). 305–308.

[14] Murad, S. A. Z., Pokharel, R. K., Sapawi, R., Kanaya, H., & Yoshida, K. (2010). High efficiency, good linearity, and excellent phase linearity of 3.1-4.8 GHz CMOS UWB PA with a current-reused technique. IEEE Transactions on Consumer Electronics. 56(3), 1241–1246.

[15] Mosalam, H., Allam, A., Jia, H., Pokharel, R., Ragab, M., & Yoshida, K. (2013). A 5-9 GHz CMOS ultra-wideband power amplifier design using load-pull. Proceedings of the IEEE International Conference on Electronics, Circuits, and Systems. 13–16.

[16] Sapawi, R., Pokharel, R. K., Murad, S. A. Z., Anand, A., Koirala, N., Kanaya, H., & Yoshida, K. (2012). Low group delay 3.1-10.6 GHz CMOS power amplifier for UWB applications. IEEE Microwave and Wireless Components Letters. 22(1), 41–43.

[17] Mosalam, H., Allam, A., Jia, H., Abdelrahman, A., Kaho, T., & Pokharel, R. K. (2015). Group delay for UWB applications. IEEE MTT-S International Microwave Symposium. 0–3.

[18] Rifin, R., Mamun, M., Amin, S., & Husain, H. (2013). Design of an inductor-less LNA using resistive feedback topology for UWB applications. Research Journal of Applied Sciences, Engineering and Technology. 5(6), 2196–2202.

[19] Chunhua, W., & Qiuzhen, W. (2011). A 0.18 um CMOS low noise amplifier using a current reuse technique for 3.1-10.6 GHz UWB receivers. Journal of Semiconductors. 32(8):085002.

[20] Maisurah, S., Wong, S. K., Kung, F., & See, J. H. (2007). 0.18um CMOS power amplifier for ultra-wideband (UWB) system. IEEE International Conference on Wireless and Optical Communications Networks (WOCN). 8–11.

[21] Murad, S. A. Z., Pokharel, R. K., Kanaya, H., & Yoshida, K. (2009). A 3.0-7.5 GHz CMOS UWB PA for group 1~3 MB-OFDM application using current-reused and shunt-shunt feedback. 2009 International Conference on Wireless Communications and Signal Processing (WCSP). 5–8.

[22] Murad, S. A. Z., Pokharel, R. K., Galal, A. I. A., Sapawi, R., Kanaya, H., & Yoshida, K. (2010). An excellent gain flatness 3.0-7.0 GHz CMOS PA for UWB applications. IEEE Microwave and Wireless Components Letters. 20(9), 510– 512.

[23] Sapawi, R., Pokharel, R. K., Kanaya, H., & Yoshida, K. (2012). A wide range CMOS power amplifier with improved group delay variation and gain flatness for UWB transmitters. IEICE Transactions on Electronics. 95(7), 1182–1188.

[24] Sapawi, R., Pokharel, R. K., Mat, D. A. A., Kanaya, H., & Yoshida, K. (2011). A 3.1–6.0 GHz CMOS UWB power amplifier with good linearity and group delay variation. Proceedings of the Asia-Pacific Microwave Conference 2011. 9–12.

[25] Sun, X., Huang, F., Tang, X., & Shao, M. (2012). A 0.7-6 GHz broadband CMOS power amplifier for multi-band applications. International Conference on Microwave and Millimeter Wave Technology, Proceedings. 1(2), 371–374.

[26] Murad, S. A. Z., Shahimim, M. M., Pokharel, R. K., Kanaya, H., & Yoshida, K. (2011). A 6-10.6 GHz CMOS PA with common-gate as an input stage for UWB transmitters. TENCON-IEEE Region 10 Annual International Conference, Proceedings. 607–610.

[27] Sapawi, R., Pokharel, R., Murad, S. A. Z., Mat, D. A. A., Kanaya, H., & Yoshida, K. (2011). Low power, low group delay MB-OFDM UWB CMOS power amplifier using current-reused technique. TENCON-IEEE Region 10 Conference. 788–791.

[28] Abraham, A. A., & Manikandan, P. (2012). A novel CMOS power amplifier for UWB application. Proceedings - 2012 2nd International Conference on Advanced Computing and Communication Technologies (ACCT). 439–442.

[29] Sapawi, R., Murad, S. A. Z., & Mat, D. A. A. (2012). 5–11GHz CMOS PA with 158.9±41ps group delay and low power using current reused technique. AEU-International Journal of Electronics and Communications. 66(11), 928–932.

[30] Bhale, V. P., Shah, A. D., & Dalal, U. D. (2014). 3-5 GHz CMOS power amplifier design for ultra-wide-band application. 2014 International Conference on Electronics and Communication System (ICECS). 3–5.

[31] Liao, C. H., & Chuang, H. R. (2003). A 5.7 GHz 0.18 um CMOS gain controlled differential LNA with current reuse for WLAN receiver. IEEE Microwave and Wireless Components Letters. 13(12), 526–528.

[32] Lim, W. M., Do, M. A., Ma, J. G., & Yeo, K. S. (2003). A broadband CMOS LNA for WLAN applications. IEEE Conference on Ultra Wideband Systems and Tehnologies. 42–4.

[33] S. Hanen, M. Dhieb, H. Chariani, M. Lahiani, 3.1-10.6GHz High Linearity, excellent gain flatness CMOS Power Amplifier for UWB Application using stagger tuning technique, 2nd International Conference on Advance Technologies for Digital and Image Processing. 2016.

[34] A. Basaligheh, P. Safffari, M. Taherzadeh-Sani, F. Nabki, A Highly Efficient and Linear Broadband Common-Drain CMOS Power Amplifier with Transformer-Based Input Matching Network, IEEE Microwave and Wireless Component Letter. Vol 25, No. 12, 2015.

[35] P-H. Huang, Z-M. Tsai, K-Y. Lin, H. Wang, A High-Efficiency, Broadband CMOS Power Amplifier for Cognitive Radio Applications, IEEE Transactions on Microwave Theory and Techniques. Vol, 58, N. 12, 2010.

[36] H. Wang, C. Sideris, A. Hajimiri, A CMOS Broadband Power Amplifier with a Transformer-Based High-Order Output Matching Network, IEEE Journal of Solid State Circuit. Vol. 45, No. 12 2010.

[37] K. Kim, J. Ko, S. Lee, S. Nam, A Two-Stage Broadband Fully Integrated CMOS Linear Power Amplifier for LTE Applications. IEEE Transactions on Circuits and Systems, Vol 63, No 6, 2016.

[38] A. Neifar, G. Bouzid, M. Masmoudi, A 3-5 GHz Fully Differential Power Amplifier for Low Power Medical Application. 13th International Multi-Conference on Systems, Signals & Devices (SSD),pp562 – 566, 2016.

[39] R. Sapawi, D.N.S.D.A. Salleh, S.K. Sahari, S.M.W.Masra, D.A.A. Mat1, K. Kipli, S.A.Z. Murad, "High Gain of 3.1-5.1 GHz CMOS Power Amplifier for Direct Sequence Ultra-Wideband Application", Journal of Telecommunication, Electronic and Computer Engineering, Vol. 8 No. 12, pp. 99-103.