A Review of CMOS Low Noise Amplifier for UWB System

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***Abstract*—A number of CMOS low noise amplifier (LNA) design for ultra-wideband (UWB) application had been produced with a various topology and techniques from year 2004 to 2016. The performance of LNA such as frequency bandwidth, noise figure, input and output matching and gain depend with the choice of the topology and technique used. Among the techniques introduced are current reuse, common source, resistive feedback, common gate, Chebyshev filter, distributed amplifier, folded cascade and negative feedback. This paper presents the collection of review about design of low noise amplifier used for UWB application in term of topology circuit. Thus, the problem and limitation of the CMOS LNA for UWB application are reviewed. Furthermore, recent developments of CMOS LNAs are examined and a comparison of the performance criteria of various topologies is presented.**

***Index Terms*—Low Noise Amplifier (LNA); Ultra-Wideband (UWB); Radio Frequency (RF).**

I. INTRODUCTION

Ultra-wideband (UWB) is a very promising technology with its features for major advances in wireless communications, networking, radar and imaging system. UWB transceiver is a combination of transmitter and receiver that will be used to transmit and receive the data signal processing. In UWB transmitter and receiver, the component involved are power amplifier [1]- [2], mixer [3], low noise amplifier (LNA) [4]-[6], and oscillator. UWB transmission system offers ability to transmit the data for short-range communications, security system and measurement applications. The advantages of this technology including low-power transmission, its stability for multi-path fading and it require low power. In 2002, Federal Communication Commission (FCC) had defined UWB as any signal having bandwidth of greater than 500 MHz or a fractional bandwidth larger than 20% at all times of transmission where the frequency allocated is from 3.1 GHz to 10.6 GHz.

LNA is the "front end" of the receiver that function to get and amplify a very low power, low voltage signal which also containing unwanted signal that received from antenna, at the range of certain bandwidth. LNA are commonly located very close to receiver to reduce the loss. In fact, the LNA is an important block in wireless communication receiver that widely used in UWB technology. The key parameters of LNA are wide input and output matching, flat gain, low power consumption, good linearity and low noise figure. The most important requirement for LNA is to have tolerable gain to minimize the noise that will be produced by another block after LNA. However, if the gain is extremely high, it will cause a large interference signal that is exceeding the limit can be handled by mixer's linearity. Generally, UWB application, minimum gain of LNA is above 10 dB. Meanwhile, the best noise figure (NF) for LNA is lower than 3dB because of unavoidable losses of RF filter remain little noise budget for other active block [4]. Therefore, the LNA design must be a good design to minimize the contribution of noise and higher gain as possible.

II. DEVELOPMENT OF LNA FOR UWB

Development of LNA in UWB using CMOS technology had been introduced since 2004 [4] with the introduction of LNA with cascode feedback. Since then, there are various designs and improvement to produce better LNA used in UWB. Table 1 shows the development of low noise amplifier for UWB system. The design is fully based on CMOS technology. In this table, the proposed design cover frequency from 3.1-10.6 GHz, 3-5 GHz, 3-7 GHz etc., depending on the application of the design.

III. LOW NOISE AMPLIFIER FOR ULTRA-WIDEBAND DESIGN TECHNIQUES

The first research on LNA for UWB had been conducted 2 years after FCC released the frequency for UWB by [4]. In their design, they using cascode feedback technique to reduce the high frequency roll-off of the input devices due to the Miller effect [4]. Since then, a lot of researches on LNA for UWB system had been done. The most topology used are current reuse topology, some of the research used filter known as Chebyshev filter, feedback circuit and single-ended cascode topology.

A. Single-ended Cascode Topology

The single ended cascode topology involved only one stage of differential LNA. This topology adopted to reduce the needed of using multiple stage or transmission line based matching technique that will lead to space consuming. Most of the single stage in LNA use common source (CS). The reason is common gate (CG) has lower noise values than CS and make it more suitable to be used for optical and microwave broad-band communication applications. However, common drain (CD) is rarely use in LNA design but widely used for the low thermal-resistance, oscillator and low-distortion variable-gain amplifier [25].

Figure 1 shows the schematic of LNA with common source and common drain topologies [18]. The proposed design used single stage differential LNA using matching technique at the output circuit to avoid the degrading effect of the low-quality factor, Q. This design adopted using 0.13 µm CMOS technology. The common source configuration then will

relate to the gate-drain capacitance to give good central operating frequency. The noise figure of this design is 4.4 dB with the simulated gain (S_{21}) is 9.72 dB. The supply voltage is at 1.2V with power consumption is 20.76 mW.

Table 1
Summary of LNA UWB design

Year	Frequency (GHz)	Technology	Circuit topology/ technique	NF(dB)	S_{11}(dB)	S_{21} (dB)
2016 [5]	3-11	TSMC 0.18 µm	Current reuse	3.22-3.53	-8.2	17.1-18.38
2015 [6]	3.1-10.6	90nm CMOS	Common source	1.7	<-10	>20
2015 [7]	2.8-10.6	TSMC 0.18 µm	Current reuse	2.98-3.4	<-7.45	11.25-13.4
2015 [8]	3.1-10.6	0.18 µm CMOS	Current Reuse	4-7	<-11	10.3
2014 [9]	3.1-10.6	0.18 µm CMOS	Current reuse	<3.8	<-10	12.25
2014 [10]	3.1-10.6	TSMC 0.18µm	Chebyshev filter	2.89	<-10	20
2014 [11]	3.1-10.6	0.18 µm CMOS	Common Source	<3.8	<-10	12.25±0.25
2012 [12]	1-9	TSMC 0.18 µm	Resistive Feedback	3.5-4.8	-	22±5
2011 [13]	3.1-10.6	0.18 µm CMOS	Resistive Shunt Feedback	3.9-6.3	-	9-11
2010 [14]	4.36-12.2	0.18 µm CMOS	Shunt Feedback	2.0- 3.0	<-8.7	10-13
2010 [15]	3.1-10.6	TSMC 0.18µm CMOS	Current Reuse	5.27-7	<-13.5	7-12
2010 [16]	3.1-4.8	90nm CMOS	Common Gate	0.4-1.1	<-9	>10
2009 [17]	3-5	0.18µm RF CMOS	Chebyshev filter	2.7-3.2	<10.3	8.6-9.5
2009 [18]	21	0.13µm CMOS	Common source	4.4	<-26	9.72
2008 [19]	3-12	UMC 0.13µm CMOS IC	Dual loop negative feedback	2	<-10	17
2007 [20]	3.1-10.6	0.18 µm CMOS	Current reuse	5-5.6	<-8.6	9.5
2007 [21]	0.4-10	0.18 µm CMOS	Common gate	4.4-6.5	-	12.4
2007 [22]	3-5	HJTC 0.18µm CMOS	Chebyshev Filter	3.5-5.5	<-9	12
2006 [23]	3.1-10.6	TSMC 0.18µm	Negative Feedback	<3	-	>11
2006 [24]	3.1-10.6	TSMC 0.18µm CMOS	Folded cascade and negative f/back	2.9	<-10	>12
2006 [25]	2.7-9.1	0.18µm CMOS	Distributed	3.8-6.9	<-10	10
2005 [26]	2-4.6	0.18µm CMOS	Resistive Shunt Feedback	2.3	<-9	9.8
2004 [27]	3.1-4.8	0.18µm CMOS	Common gate	3.95-4.3	<-15dB	16.05
2004 [4]	3-7	TSMC 0.18µm RF CMOS	Cascode feedback	<1.9	-	14.5-15

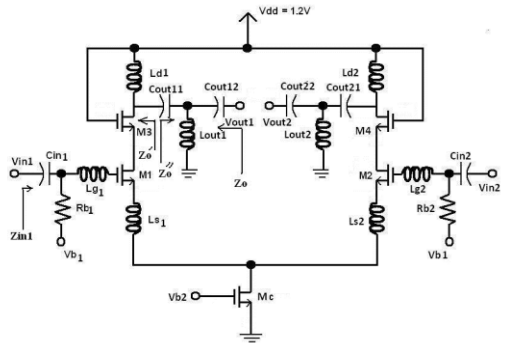

Figure 1: The 21 GHz UWB differential LNA [18]

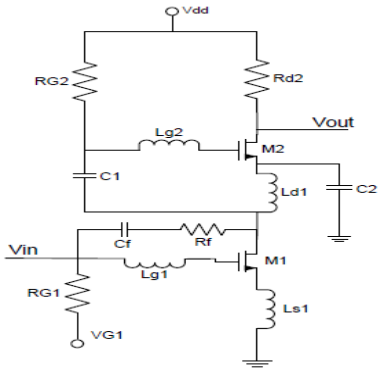

Figure 2: Complete UWB LNA schematic circuit [11]

The common source based current reuse LNA is proposed in [11]. The design involved two common source stages that combined and forms a current reuse core with resistive termination. This design also implemented a little bit of delicate shunt capacitive-resistive feedback technique used to widen the input impedance matching and give better stability. The NF for this design is less than 3.8 dB and the application is for full band UWB. The power consumption for this design is 18 mW and fabricated with the chip size of 0.33 mm^2. Figure 2 shows the complete LNA circuit for common source topology.

In [27] as in Figure 3, common gate is used as wideband input matching. Common gate topology is adopted because in this topology, transistor g_m is not much affected by the frequency. With the non-existing of miller capacitance multiplication at the input, it will make this topology have a broadband impedance and wide gain. The proposed design had been designed using 0.18 µm CMOS process and the NF is 3.95 dB to 4.3 dB at the frequency of 3.1-4.8 GHz. The gain is quite high from 16.4 dB to 16.98 dB with supply voltage at 1.8V and power consumption is 21mW.

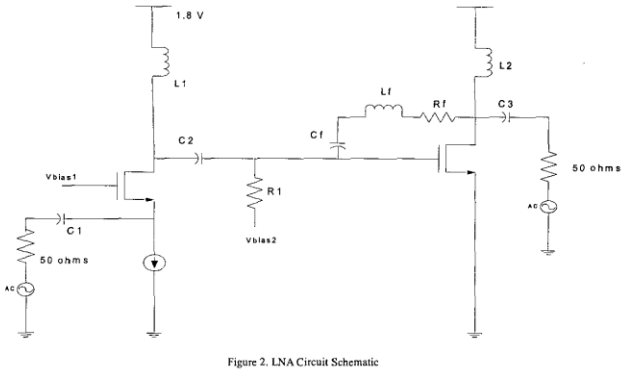

Figure 3: LNA Circuit Schematic [27]

In [21], common gate, common source and output buffer is employed to design UWB LNA. Besides using common gate as wideband noise, it also used for power matching purpose. At input stage, common gate also provides a narrow-band frequency response apart from give wide band input matching. To have good input matching, the size of M_1 needs

to be determined carefully in this design. R_{L1} also affect the value of the gain at first stage and gate bias at second stage. Simple cascade common-source stage is used in second stage that contributes high-frequency gain and determines higher bandwidth. The completed circuit as in Figure 4 had been fabricated using 0.18 µm CMOS technology with chip size of 0.42 mm^2 for 0.4-10 GHz application. The measured gain is 11.2 to 12.4 dB with noise figure of 4.4-6.5 dB and consumed power of 12 mW from 1.8V power supply.

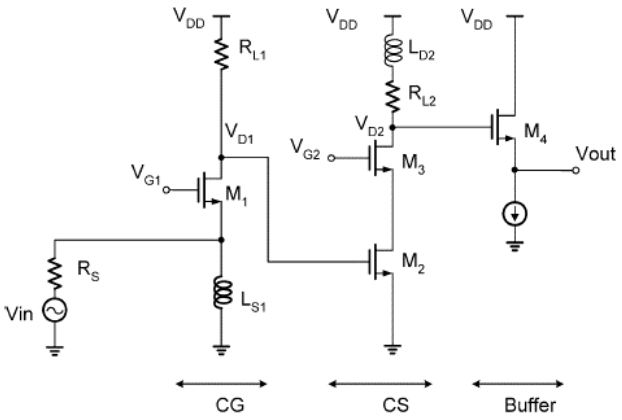

Figure 4: UWB LNA [21]

In 2009, common gate topology once again used in designing 1-5 GHz UWB LNA by [29]. In this design, it consists of 3 stages which are common gate stage, cascode stage and buffer as shown in Figure 5. The main function of cascode stage is to give high gain at high frequency. Transistor in this stage is used to determine the isolation between the output and the input while the purpose of inductor is for 50 Ω output matching. This design had been fabricated with chip size of 0.78mm^2 and power consumption of 9 mW and 1.8 V supply voltage. The maximum NF is at 6.5dB and maximum gain is 13.7dB.

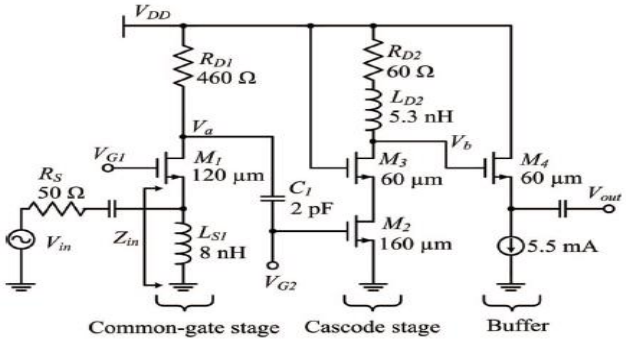

Figure 5: Schematic for the UWB LNA [29]

With the additional of inductor, L_{S1} in the common gate stage for input matching, it will help to resonate the parasitic capacitance as used in [16]. This proposed design is using 90 nm technology and Balun (balanced-unbalanced) network to convert perform single-ended to differential at the input and reverse conversation at the output. To achieve a better performance in the range of certain band, the inductive load $L_{D1}(L_{D2})$ is introduced as shown in Figure 6. This inductive load is a very crucial component because of its function to set the frequency out of operating frequency to avert the LNA becoming a narrow band amplifier. Moreover, the optimum value of this load also need to be considered because it can cause the low self-resonance frequency if the value is set more that maximum value. The results show that the working frequency is from 3.1-4.85 with gain is from 11-24 dB, NF at 0.4-1.1 dB and power dissipation is 4 mW from 1V power supply.

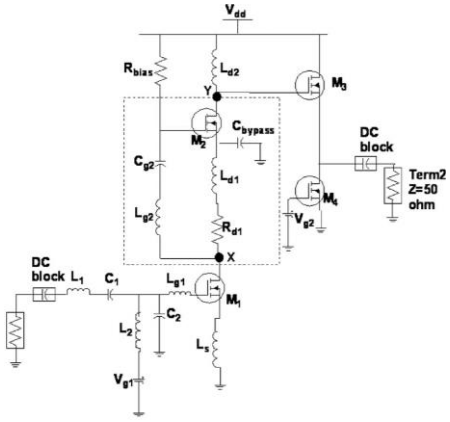

Figure 6: Proposed Differential LNA [16]

For low voltage application, [27] proposed LNA design is employed two-stage common source (CS) that adopt a forward-body bias technique as illustrated in Figure 7. The first stage gives extraordinary high gain caused by high transconductance used as input component. In second stage, it involved with simple source degenerated CS topology with the shunt peaking inductor. The purpose of the inductor is to boost the gain response at high frequencies. A large value of resistor is used at first stage to cut down noise contribution at the input. C_c will be short circuit at high frequency which will allowed the signal to travel from first stage to the next stage. This design is used 90 nm CMOS process to achieve a great gain which is more that 20dB for full band UWB application with very low power supply of 0.6 V and power consumption of 12.6mW. Furthermore, this design also attained very low noise figure value of 1.7dB.

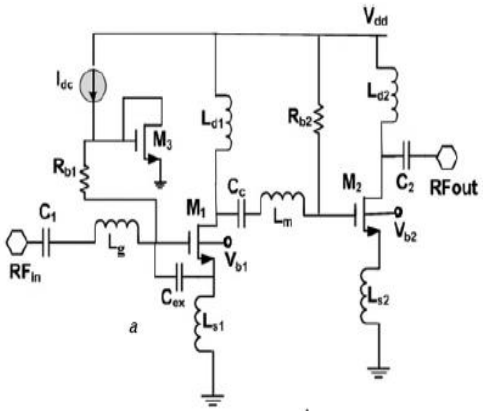

Figure 7: LNA Circuit Schematic [27]

B. Current Reuse

Current reuse is believed can be used to overcome the disadvantage of previous topologies which have high power consumption that is not very compatible to be used in battery-powered UWB application. According [30], to reduce NF and increase gain for LNA design, current reuse topology usually implemented in series inter-stage resonance with high gain current-reused two-stage amplifier technique.

[20] had employed current reuse topology and fabricated

using 0.18µm/IP6M standard CMOS process with the chip size of 0.98 mm^2. The proposed design involved two stages of amplifier by using current-reused cascaded common-source structure as depicted in Figure 8. The first stage is to resonate the desired frequency at the lower part and the second stage is used to obtain higher frequency band. Second stage is stacked on top of first stage to reduce the power consumption.

The results show that the proposed design achieved the frequency from 3.1 to 10.6 GHz, power gain, NF, and power consumption of 9-11dB, 5-5.6B and 9.4mW, respectively.

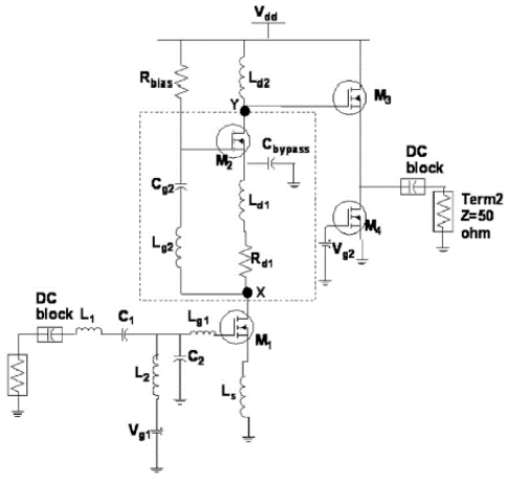

Figure 8: Schematic of the ADS-designed UWB LNA circuit [20]

The current reuse with stagger tuning technique is introduced in [15]. The purpose of stagger tuning technique is to extend the bandwidth and current reuse is used to decrease the power consumption for the LNA. This design used TSMC 0.18-µm CMOS process and gives average gain of 9.7 dB with chip size of 1.17 x 0.88 mm^2. As shown in Figure 9, the proposed design involved two stages that common gate and common source amplifier. The second stage is used as gain stage that RF signal will be highly amplified. This design is operated at 1.5V power supply with power consumption of 4.5 mW and the NF is maintained under 7dB for the full band operation.

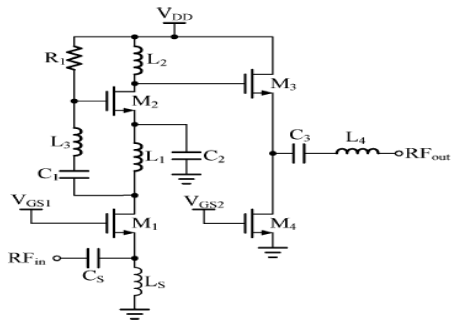

Figure 9: Proposed low-power Full Band LNA [15]

In 2014, [9] presented the proposed design of CMOS LNA by employing a common source based current reuse technology with the aim to reduce group delay variation and enhance NF. This design is works on full band and achieved gain flatness of 12.24±0.25 dB with NF below 3.8 dB and group delay variation of ±25 ps. At the input common source stage, it has inductive source degeneration and series peaking to achieve good input impedance. For wide input impedance matching and better stability, a weak shunt capacitive-resistive feedback is implemented at the input stage. This design shows in Figure 10 is fabricated on 0.33 mm^2 chip and consumes 18 mW of power from 1.8 V DC supply.

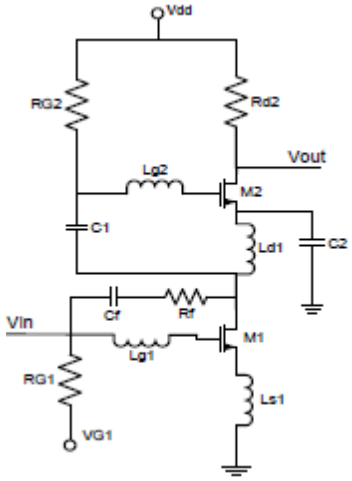

Figure 10: Proposed LNA circuit [9]

Current reuse with a peaking inductor through inter stage technique LNA for UWB designed by [7]. The design used TSMC 0.18 µm CMOS technology and the main focus is to produce low power consumption. The proposed design consumed of 5.74 mW from 1.8 V power supply. Common gate with resistive feedthrough technique and current reuse is applied to minimize power consumption. The source follower that connected in cascade with current reuse connection is employed to flatten the overall gain and to obtain greater output impedance. The schematic of the proposed LNA UWB design can be seen in Figure 11. The simulation result shows that the frequency range is 2.8-10.6 GHz, the power gain is between 11.25dB to 13.39dB and the NF is at range of 2.98-3.4dB.

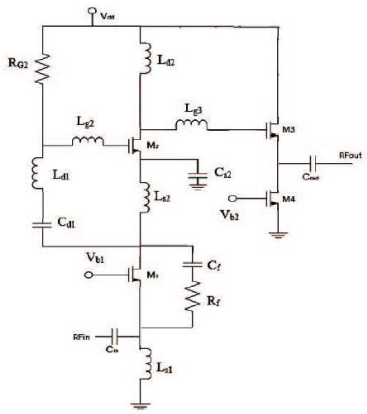

Figure 11: Schematic of proposed UWB-LNA [7]

Coupled inductor together with cascade current reused topology are used in [8] LNA UWB circuit. The usage of coupled inductor is to produce feedback through mutual inductance then synchronously achieve both high gain and bandwidth and low power consumption. By adding extra inductive feedback by combining the inductive source degeneration, it will help to increase the gain and input matching of the topology simultaneously. Two inductors are

connected in the form of spiral shape of adjacent metal layers with stacked up on top of each other to create coupling effect [8]. The simulation results for this design were power gain of 14±.2 dB, NF of 3.7±.5dB, S_{11} and S_{22} below than -10dB and -9dB, respectively across the frequency from 3.1-10.6 GHz. Figure 12 shows the schematic of design that draw 3.24 mA from 1.5 V supply.

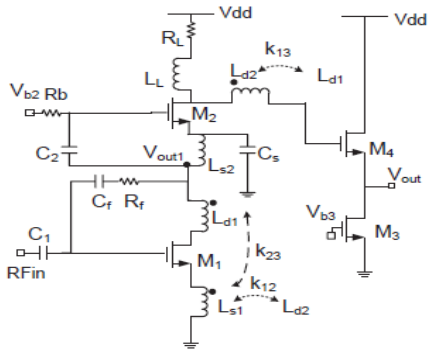

Figure 12: Ultra-wideband Low-Power LNA using couple inductors [8]

The latest design of UWB LNA using current reuse is proposed in [5]. Inter stage technique used current reuse topology to cut down the power consumption and to attain flat gain, it connected in cascade with a source follower. The design is employed common gate with resistive feedthrough technique to reduce the noise factor at the lower point. Noise figure from simulation is at the range of 2.98-3.4 dB for this proposed design shown in Figure 13. The power gain is 11.25-13.39 dB for frequency of 2.8-10.6 GHz and consumes power of 5.74mW from 1.8V.

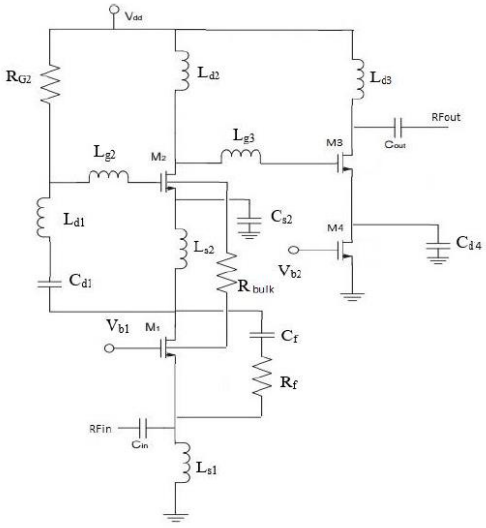

Figure 13: Schematic of the proposed current reuse technique LNA [5]

C. Feedback Topology

Definition of feedback is a circuit or loops that form from the chain of connection which the outputs are routed back as inputs of the same circuits. A negative feedback is when an output signals is opposite in value or phase to input signal. The advantages of this type of topology are decreased the distortion, less noise, less effect in changes occur in surrounding and improve system bandwidth and better impedances.

Resistive feedback is used to improve performance of LNA in [22] with combination of common-source topology. This design implemented in HJTC 0.18 µm CMOS consists of three stages which are cascade common source, resistive feedback and source follower. The full schematic of proposed design is shown in Figure 14, the function of R_1 is to improve gain at lower frequency and R_2 is used to control the stability factor indirectly increase the feedback. Gain from simulation result for this design is 10-3.3dB for 3-5 GHz, noise figure is less than 5.5dB. However, power consumption is quite high which is 12.5mW drawn from 1.8V supply.

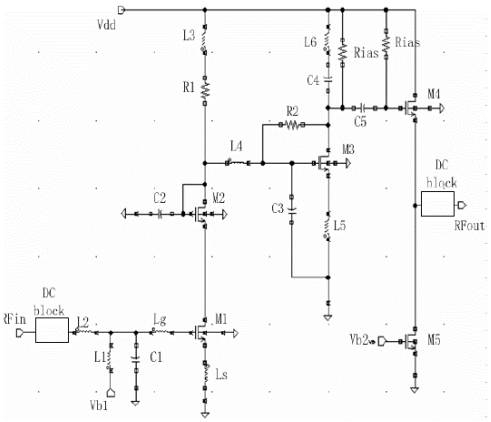

Figure 14: Resistive Feedback LNA UWB [22]

Resistive shunt feedback topology used by [26] for 3-5 GHz LNA design implemented using 0.18 µm CMOS technology. This type of feedback is choosing because of its ability to give wider input matching with low noise effect. In this design, feedback resistor is added into conventional cascode for shunt-feedback purpose as can be seen in Figure 15. Besides that, Q-factor also can be determined by applying the feedback resistor apart from extending the bandwidth and gain flatness. The measurement result shows NF level only at below 3 dB, 7 mA power dissipation at 1.8V supply. The disadvantages of this design are high power dissipation and the frequency range is not widely to cover full UWB application.

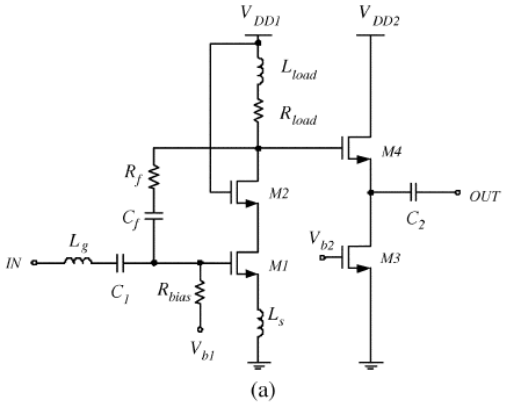

Figure 15: Resistive Shunt Feedback LNA [26]

Another design involving with resistive shunt feedback is proposed by [13] for full band of UWB. This design shown in Figure 16 had been designed, fabricated and tested on 0.55 x 0.4 mm^2. R_f is the feedback resistor in first stage and C_f works as blocking capacitor. At this stage, loading element

formed by a resistor parallel with and inductor that will affected input impedance. The measured results show the noise figure from 3.9dB to 6.3dB and power consumption at 9 mW. Even though this circuit can achieve full band requirement, the power gain is considered low with gain of 7.5dB.

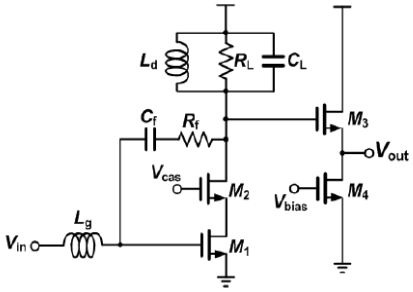

Figure 16: Developed UWB LNA with resistive shunt feedback [13]

[12] proposed another LNA that involved with resistive feedback with current reuse technique. The proposed circuit shown in Figure 17 is consisting of two variable stages, biasing circuit and output. In current reuse configuration, load resistance is swap by a PMOS transistor to hold the saturation level of the transistor. Feedback resistor need to be large enough to maintain the low NF. The simulation result for this design are gain of 22dB and NF of 3.5-4.8dB for operating frequency from 1-9 GHz. The power consumption for this design is considered high which is 12.9 mW from 1.4 V supply compared with other design that been stated in this paper. The other drawback of this design is it require a lot of transistor.

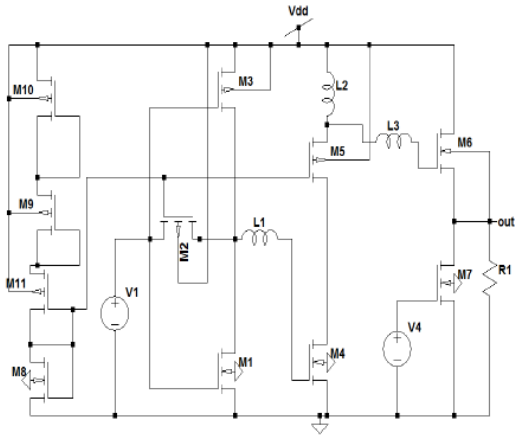

Figure 17: UWB LNA [12]

UMC 0.13µm CMOS IC technology adapt in [19] dual-loop negative feedback to achieves good impedance matching, decrease noise figure and reduce the size of chip because of less inductor used. In this design, resistive feedback and nullor are employed to fulfil the requirement of good LNA. Two feedback loops are involved which are voltage-to-current feedback loop and an indirect current-to-current feedback loop. Current-to-current feedback does not sense the output directly caused the final circuit to have two inputs and four current outputs consists of two negative and two positive outputs. One of negative output will fed back into input while the other one will go to the load and the positives outputs are put in parallel and converted to a voltage before feedback to the input. To get low noise, feedback resistor in this design need to be small and R_2 need to be as large as possible. However, if the feedback is too small, it might cause a clipping effect to the circuit. This design can be applied on 3-12 GHz UWB application with noise figure is 2 dB minimum at 5GHz, power gain is quite high which is at 17 dB and power supply needed is 1.2 V. Unfortunately, the power dissipation for the design in Figure 18 is still high at 16.8mW.

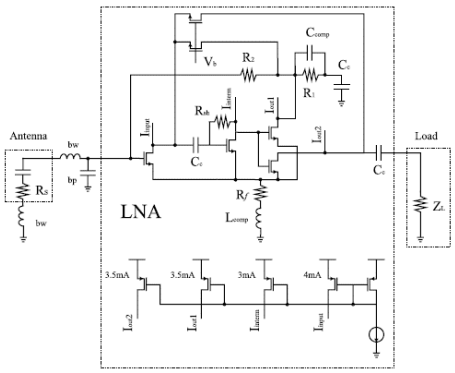

Figure 18: Final circuit with biasing [19]

Another feedback used is shunt feedback by [14]. Input shunt feedback is adapted because of its ability to increase the bandwidth. Apart from the shunt feedback, forward body bias for decreasing the threshold voltage and inductive degeneration for good matching also been complied in this design. The first stage focusses on input matching and noise figure using both inductive degeneration and input shunt feedback topologies while the second stage is for gain. Figure 19 shows the wideband body enabled LNA and fabricated with the chip size of 750 x 512 µm. The measured gain is over 10 dB over frequency of 1.4-12.2 GHz bandwidth with noise figure as low as 1.97 dB. The disadvantage of this design is the power consumption is still high i.e., 133mW from 1.5V DC supply.

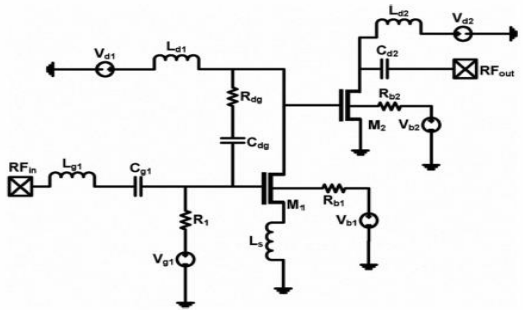

Figure 19: Wideband Body Enable LNA [14]

Negative feedback to increase the bandwidth with cascode configuration is the main design by [23]. This full band design is applied noise cancelling technique in the proposed design as shown in Figure 20. Although feedback does not give any effect on noise performance, but it is useful for broaden the bandwidth. The first stage of the design, cascade configuration with negative feedback is used to enhance the bandwidth and to achieve synchronously output impedance matching, common drain is used after the cascade stage. The combination of cascode stage and negative feedback

combination, it will produce a noise cancelling technology which after doing some calculation mention in their paper, the noise current at output port will cut off to zero value. For the second stage, RLC shunt-shunt feedback is used to get the broadband gain. The simulation results show the gain above 11 dB, noise figure below 3 dB, first stage draw 12 mA and 8 mA at second stage, were achieved. But, high power dissipation of 27mW is achieved.

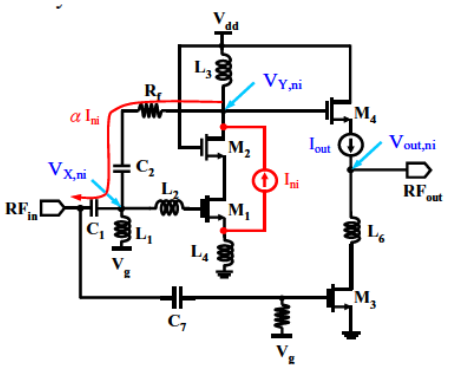

Figure 20: Matching UWB LNA using noise cancelling [23]

[24] used folded cascade and negative feedback topology in their design. The purpose of the folded cascade configuration and negative feedback is to have low noise figure and broadband bandwidth. In first stage, the folded cascade stage been used to extend the input matching to the whole UWB frequency band. Since folded cascade configuration only used to operate at low supply voltage, negative feedback is used to extend the bandwidth. For a better performance of wideband amplifier, shunt-shunt feedback network is used. Negative feedback is believed to reduce the gain to optimize the frequency response because of the constancy of the gain and bandwidth. However, the usage of negative feedback will not give any effect to noise performance for amplifier. The chip size for this design is shown in Figure 21 of 1.195 x 1.275 mm with simulated results S_{21} above 12 dB and noise figure below 3.6 dB. Chip size for this design is considered big for LNA since it used 8 inductors and indirectly it shows the complexity of the design.

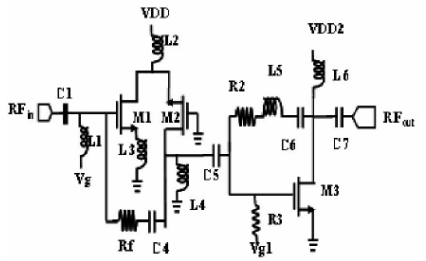

Figure 21: UWB LNA schematic for 3.1-10.6 GHz [24]

Another type of feedback that had been used in designing UWB LNA is cascode feedback that proposed by [4]. The combination of this feedback and wideband matching technique is choose by the authors because it can achieve both broad bandwidth performance and good input/output matching. Cascode configuration used to maintain the high frequency of the input component due to Miller effect. For better stability and bandwidth, it employs negative parallel feedback. For the feedback resistor, the value is determined between 800Ω to 1kΩ for the LNA to achieve desired gain and good NF over wide band frequency range. Complete design of LNA is shown in Figure 22. The simulation results show the maximum power gain is 15.3dB, NF is 1.4-1.9 dB for 3-7 GHz frequency range. This design is well stable in term of power gain and noise figure but still it has larger power consumption compare with another topology.

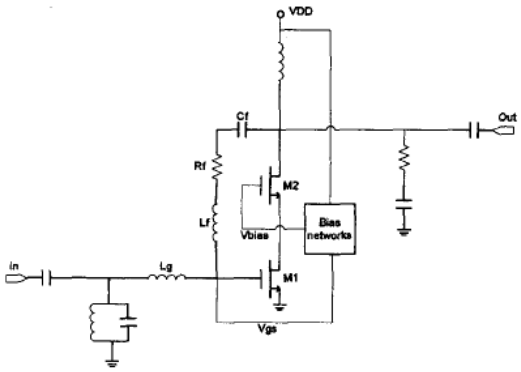

Figure 22: The complete schematic of LNA with bias network [4]

D. Chebyshev Filter

Chebyshev filter topology had been used in UWB LNA designs. The researchers had found out Chebyshev filter can overcome the disadvantage of using band pass LC filter and resistive feedback amplifier which will require larger chip area and poor NF value. Chebyshev filter is used to get wideband input matching and flat gain. It has a property of sharp roll of factor in stop band and ripples in the pass band [10].

Three section bandpass Chebyshev filter structure of the input matching network is employed in [31]. The main purpose of the filter is to resonate the reactive part of the input impedance over full band frequency of 3.1 to 10.6 GHz. All the filter's components are determined by denormalization, by set up the desired frequency and by calculating the center frequency for the whole system. To minimize the parasitic capacitance, the cascode device is chosen to be small value. To phase out the noisy bias isolation resistor, MI referring to whole design in Figure 23 is biased through one ac-ground point of the filter. The measurement results show the forward gain of 9.2 dB, NF of 4.78 dB and power dissipation of 9 mW are achieved. The disadvantage of this design is does not to give good power gain which should be more than 10 dB and high in noise figure.

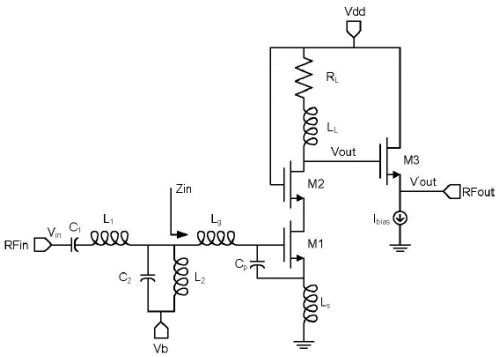

Figure 23: Complete schematic of LNA [31]

By using the same three section passband Chebyshev filter and combine with common source topology, the full band

UWB LNA is proposed by [17]. This design covered 3-5 GHz of UWB frequency and implemented in 0.18µm RF CMOS technology. Figure 24 shows the complete circuit of this LNA which the L_1 and C_1 are series resonator, L_2 and C_2 are parallel resonator, $L_3=L_g + L_s$ is input matching of narrowband cascode. The other capacitor, C_3 is parasitic capacitor placed as input for M_1 and C_P and these component produce the Chebyshev filter. To obtain low noise and good gain, apart from fulfil all the broadband requirement, the impedance matching must be good enough. In addition, for the system to attain high gain, the input and output impedance must be unified. The simulation result for this circuit shows a good noise figure of 2.7dB and the power consume of 15mW is achieved. However, the power gain for this design is considered low because it only can achieve up to 9.5dB in short range of frequency.

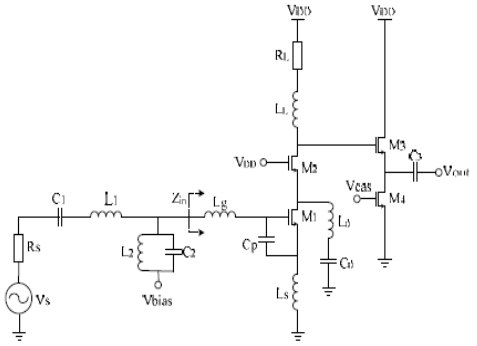

Figure 24: Full UWB Schematic with Chebyshev Filter [17]

Another design that used Chebyshev Filter is proposed by [10]. After the signal pass Chebyshev filter, the reactive part of the input impedance will oscillate by double terminated band pass filter circuit over full band frequency of UWB. For amending the bandwidth of amplifier, active inductor is placed between the common gate and common source topologies. The design is shown in Figure 25 that leads to good power gain at the maximum value is 20dB, good noise figure value at 2.89 and power dissipation of 12mW.

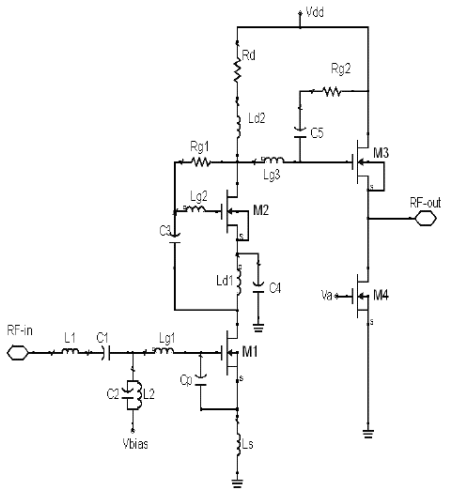

Figure 25: circuit of proposed LNA [10]

E. Distributed Amplifier

Generally, distributed amplifier is a topology that can absorb parasitic capacitance produce by transistors to improve the amplifier bandwidth. However, this topology has it great disadvantages because it requires large area and high in power consumption. This will affect the overall performance of UWB LNA that required as minimum space as possible and low power consumption since it need to be combined with other elements in receiver.

This topology introduce in [25] and the full schematic is shown in Figure 26. Apart from using two stages of distributed amplifier, this design combines inductive degeneration technique to get broadband and minimize the noise effect. In addition to improve the gain at high frequency, conventional distributed amplifier is cascaded with common source topology. At the first level, inductive degeneration technique is applied to conventional distributed to improve noise characteristic. However, this will weaken the gain and the changes of the gain is very minimum as the frequency increases. To overcome the problem, common source single stage amplifier is cascaded with the two-stage distributed amplifier. In the conventional distributed amplifier, it has poor transmission line that mutually connected in parallel with the active devices. This cascaded connection is to improve the overall gain performance and the common source is for tuning the signal at high frequency band. The measurement results show good power gain at the frequency range of 2.7-9.1 GHz but poor noise figure of 3.8-6.9 dB. However, with the combination from a few technique and topology, this design able to operate in very low voltage, 0.6 V and overcome the problem of high power consumption caused by usage of distributed amplifier which the power dissipation is only at 7 mW.

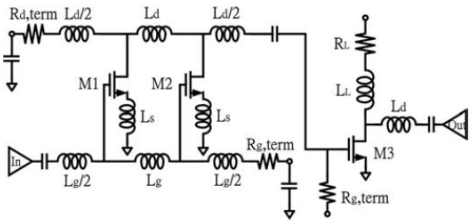

Figure 26: Schematic representation of Distributed Amplifier for UWB LNA [25]

IV. CONCLUSION

The CMOS low noise amplifier had been widely investigated and developed. Various design is been reviewed and most of the design is using 0.18 µm technology. Negative feedback, distributed amplifier and folded cascade topologies help to get broad bandwidth and better stability. Folded cascade also can be used to get low noise figure. For low power supply and low power consumption application, current reuse technique is the best choice. For a better performance and effective approach, the suitable techniques can be combined. Moreover, the optimum low noise amplifier circuit design can be achieved by using the right techniques that suits the requirement and application of UWB. With this paper, hopefully it can give benefit to other researchers whom working on the UWB LNA circuit design to help the researchers to choose which topologies is suitable the application.

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REFERENCES

[1] R. Sapawi, S. A. Zainol Murad, and D. A. A. Mat, "5–11GHz CMOS PA with 158.9±41ps group delay and low power using current-reused technique," *AEU - Int. J. Electron. Commun.*, vol. 66, no. 11, pp. 928–932, 2012.

[2] R. Sapawi, R. K. Pokharel, S. A. Z. Murad, A. Anand, N. Koirala, H. Kanaya, and K. Yoshida, "Low Group Delay 3.1-10.6 GHz CMOS Power Amplifier for UWB Applications," vol. 22, no. 1, pp. 41–43, 2012.

[3] E. Ehsaeyan, "Design of a Broadband HEMT Mixer for UWB Applications," *Indian J. Sci. Technol.*, vol. 9, no. 26, pp. 2–6, 2016.

[4] H. Doh, Y. Jeong, S. Jung, and Y. Joo, "Design of CMOS UWB Low Noise Amplifier with Cascode Feedback," *47th IEEE Int. Midwest Symp. Circuits Syst.*, pp. 641–644, 2004.

[5] E. N. A. Hamid Karrari, Hassan Faraji Baghtash, "A 3-11GHz Current-Reuse Low Noise Amplifier for Ultra-Wideband Recievers," pp. 563–567, 2016.

[6] J. Singh and S. Pandey, "A 0.6 V, low-power and high-gain ultra-wideband low-noise amplifier with forward-body-bias technique for low-voltage operations," *IET Microwaves, Antennas Propag.*, vol. 9, pp. 728–734, 2015.

[7] E. N. A. Hamid Karrari, "A 2.8-10.6GHz Low-Power Low-Noise Amplifier for Ultra-Wideband Recivers," vol. 352326, pp. 7–10, 2015.

[8] P. Jamshidi, "An Ultra Wideband Low-power Low-Noise Amplifier Using Coupled Inductors," pp. 1220–1224, 2015.

[9] H. K. Yousef, K., H. Jia, R. Pokharel, A Allam, M. Ragab, "A 0 . 18 µm CMOS Current Reuse Ultra-Wideband Low Noise Amplifier (UWB-LNA) With Minimized Group Delay Variation," vol. 85002, pp. 448–451, 2014.

[10] N. Gautam, M. Kumar, and A. Chaturvedi, "A 3.1-10.6 GHz CMOS two stage cascade topology low-noise amplifier for UWB system," *Proc. - 2014 4th Int. Conf. Commun. Syst. Netw. Technol. CSNT 2014*, pp. 1070–1073, 2014.

[11] K. Yousef, H. Jia, R. Pokharel, A. Allam, M. Ragab, and H. Kanaya, "A 0.18 µm CMOS current reuse ultra-wideband low noise amplifier (UWB-LNA) with minimized group delay variations," *Eur. Microw. Week 2014 Connect. Futur. EuMW 2014 - Conf. Proceedings; EuMC 2014 44th Eur. Microw. Conf.*, pp. 1392–1395, 2014.

[12] P. Manikandan and A. S. Areeckal, "A Novel CMOS Low Noise Amplifier for UWB Application," *2012 Second Int. Conf. Adv. Comput. Commun. Technol.*, pp. 450–453, 2012.

[13] X. Guan, C. Huynh, and C. Nguyen, "Design of a 0.18-µm CMOS Resistive Shunt Feedback Low-Noise Amplifier for 3.1-10.6-GHz UWB Receivers," pp. 5–6, 2011.

[14] J. Asmussen, S. P. Sah, X. Yu, and D. Reo, "A Wideband Body Biased Low-Noise Amplifier," no. 1, pp. 687–690, 2010.

[15] R. Weng, C. Liu, S. Member, and P. Lin, "A Low-Power Full-Band Low-Noise Amplifier for Ultra-Wideband Receivers," vol. 58, no. 8, pp. 2077–2083, 2010.

[16] N. A. V. Vaithianathan, Dr. J. Raja, R. Kavya, "A 3.1 to 4.85GHz Differential CMOS Low Noise Amplifier for Lower Band of UWB Applications," *Comput. Eng.*, pp. 20–23, 2010.

[17] J. Duan, X. Han, and S. Li, "A Wideband CMOS Low-Noise Amplifier for 3-5 GHz UWB Systems," no. 575096, pp. 4–7, 2009.

[18] S. M. S. Rashid, A. Roy, S. N. Ali, A. B. M. H. Rashid, and S. Member, "Design of A 21 GHz UWB Differential Low Noise Amplifier Using . 13µm CMOS Process," pp. 538–541, 2009.

[19] L. A. De Michele, W. A. Serdijn, S. Bagga, G. Setti, and R. Rovatti, "A UWB CMOS 0.13µm low-noise amplifier with dual loop negative feedback," *Proc. - IEEE Int. Symp. Circuits Syst.*, pp. 672–675, 2008.

[20] H. L. Kao and K. C. Chang, "Very low-power CMOS LNA for UWB wireless receivers using current-reused topology," *Solid. State. Electron.*, vol. 52, no. 1, pp. 86–90, 2008.

[21] S.-I. L. Ke-Hou Chen, Jian-hao Lu, Bo-Jiun Chen, "An Ultra-Wide-Band 0.4-10-GHz LNA in 0.18-µm CMOS," vol. 54, no. 3, pp. 217–221, 2007.

[22] J. Su, Z. Fu, H. Yuan, and M. Zeng, "An Ultra-Wideband CMOS Low Noise Amplifier For 3 – 5 GHz UWB Wireless Receivers," pp. 407–410, 2007.

[23] S. Chen, R. Wang, H. Kuo, and M. K. C. Gao, "The Design of Full-Band (3 . 1-10 . 6GH Z) CMOS UWB Low Noise Amplifier with Thermal Noise Canceling," no. 1, pp. 6–9, 2006.

[24] R. L. Wang, S. C. Chen, H. C. Kuo, and C. H. Liu, "A 0.18-µm CMOS UWB low noise amplifier for full-band (3.1-10.6GHZ) application," *IEEE Asia-Pacific Conf. Circuits Syst. Proceedings, APCCAS*, no. 1, pp. 363–366, 2006.

[25] E. H. Yu, Y. J. E. Chen, and D. Heo, "An ultra-low voltage UWB CMOS low noise amplifier," *Asia-Pacific Microw. Conf. Proceedings, APMC*, vol. 1, pp. 313–316, 2006.

[26] C. W. Kim, M. S. Kang, P. T. Anh, H. T. Kim, and S. G. Lee, "An ultra-wideband CMOS low noise amplifier for 3-5-GHz UWB system," *IEEE J. Solid-State Circuits*, vol. 40, no. 2, pp. 544–547, 2005.

[27] S. Vishwakarma, "Ultra Wideband CMOS Low Noise Amplifier with Active Input Matching," no. February, pp. 10–14, 2002.

[28] M. Shen, T. Tong, J. H. Mikkelsen, O. K. Jensen, and T. Larsen, "A 1-5 GHz UWB low noise amplifier in 0.18 µm CMOS," *2009 Norchip*, pp. 0–4, 2009.

[29] M. S. M. Shen, T. T. T. Tong, J. H. Mikkelsen, O. K. Jensen, and T. Larsen, "A 1-5 GHz UWB Low Noise Amplifier in 0.18 µm CMOS," *2009 Norchip*, pp. 0–4, 2009.

[30] S. Dixit, "A Review Paper on Different Methodology of Low Noise Amplifier," pp. 16–19, 2014.

[31] F. Ghz, W. Communication, M. Hsu, and K. Li, "An Ultrawideband CMOS Low Noise Amplifier For 3.1-10.6 GHz Wireless Communication," pp. 457–460, 2007.