Design of High Order LPF with On Chip Active Inductor Using 0.18 micron CMOS Technology

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***Abstract*— Active inductor is a circuit technique which is based on gyrator loop. Gyrator loop is composed of at least two transconductance amplifiers. Usually, the frequency response of active inductor has a phase shift 90 degrees at the resonance frequency. This paper proposes circuit technique which is based on complementary common source amplifier with drain degeneration resistors. The core circuit is connected by four transcondutors to form floating active inductor. Elements substitution is used to implement 5th and 10th order LPF Elliptic based on the proposed circuit. Due to nonlinear of a polynomial in the input impedance of transfer function, the inductor value is not constant as a function of input frequency. As a result, simulation results by Cadence Spectre is designed with transconductance curve compared with the graph of ideal LCR prototype by using 0.18 micron CMOS process.**

***Index Terms*— Floating Active Inductor; Elliptic Filter; 5th Order LPF; 10th Order LPF; Low Power WLAN Filter.**

I. INTRODUCTION

Gyrator is an architecture which can be a circuit for implementation of the grounded active inductor which is proposed since 1948 by Tellegen [1]. The simplest transconductance amplifier which can be formed gyrator loop is common source amplifier, common drain amplifier and common gate amplifier. Gyrator loop means feedback output voltage of the first transconductance amplifier to input voltage of the second transconductance amplifier. Then, the output voltage of the second transconductance amplifier is fed back to the input voltage of the first transconductance amplifier so it closes the gyrator loop. The proposed circuit add four additional between the drain terminal of the NMOS and PMOS of the transconductance amplifier to increase impedance gain of the active inductor which is seen in the formula of the symbolic input impedance of the circuit which will be derived in the later section.

Passive Filter prototype can be designed and used in continuous time filter but if cutoff frequency is low, the problem is silicon inductor consumed too much area. The active inductor is used to solve this problem. Holmes proposed low pass filter which has sharp cutoff frequency since 1962 [2]. The papers show the circuit diagram of grounded gyrator and semi floating gyrator which uses BJT transistor implementation. Nauta proposed ingenious transconductor since 1992[3]. It is more complicated circuit than basic common source amplifier. Its advantage is that it can source and sink current at the same time. As a result, its transconductance output range is wider than a simple transconductance amplifier. It also saves silicon area for resistor implementation compared with the proposed circuit. The transconductance value can be computed by derivative of output current which flows out of output nodes of the transconductor. For comparative reference with other types of the transconductance amplifier, there are some types of transconductor which have very small transconductance which is published since 2002 [7]. Some types of the grounded active inductor are proposed since 2002 [8] which have improvement of the quality factor. Higher frequency Gm-C Filter can be proposed since [9], this paper proposes a figure of merit of Gm-C filter so that someone can compare specification of Gm-C filter with fairness with the parameter such as OIP3, maximum cutoff frequency, tuning range, the order of the filter, noise figure and power dissipation. High Q active inductor is proposed to design low power CMOS VCO which is published since 2012 [10]. The recent breakthrough in active inductor called flipped active inductor is proposed since 2014 [11].

Section 2 discusses the floating active inductor based on the complementary common source amplifier with drain degeneration resistors. Section 3 discusses 5th order LPF Elliptic LCR prototype and table of elements value design based on resistor scaling and cutoff frequency scaling. Section 4 discusses how to create a full schematic of 5th order LPF Elliptic based on the proposed circuit called CCSDDR by element substitution. Section 5 discusses simulation results which performed by Cadence Spectre. Section 6 discusses how to design transconductor. Section 7 discusses the analysis of floating active inductor equivalent circuit of the block diagram. Section 8 is how to design 10th order LPF Elliptic LCR prototype. Section 9 is the discussion on dynamic and power consumption of continuous time filter. Section10 is the conclusion.

II. FLOATING ACTIVE INDUCTOR BASED ON CCSDDR AMPLIFIERS

The proposed circuit composed of two transistors and two resistors to form transconductor. The floating active inductor architecture is composed of four transconductors. It is connected as depicted in Figure 1.

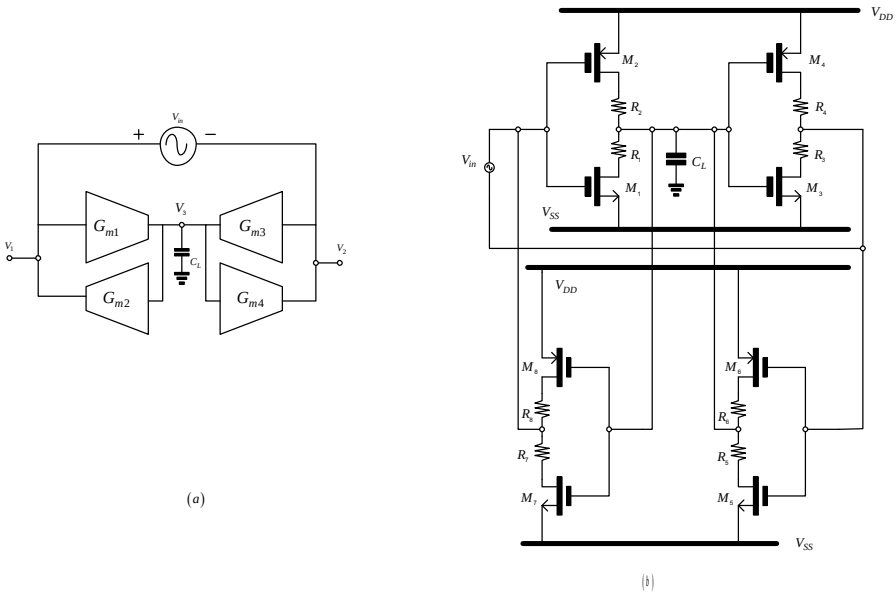

Figure 1: (a) Architecture of floating active inductor (b)Transistor schematic of (a)

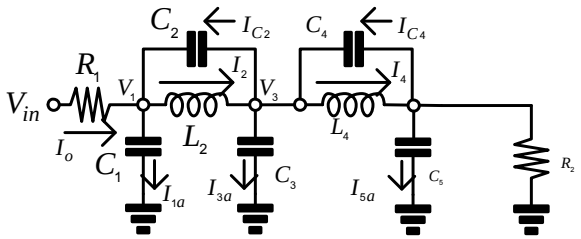

Figure 2: 5th order Elliptic LPF LCR prototype

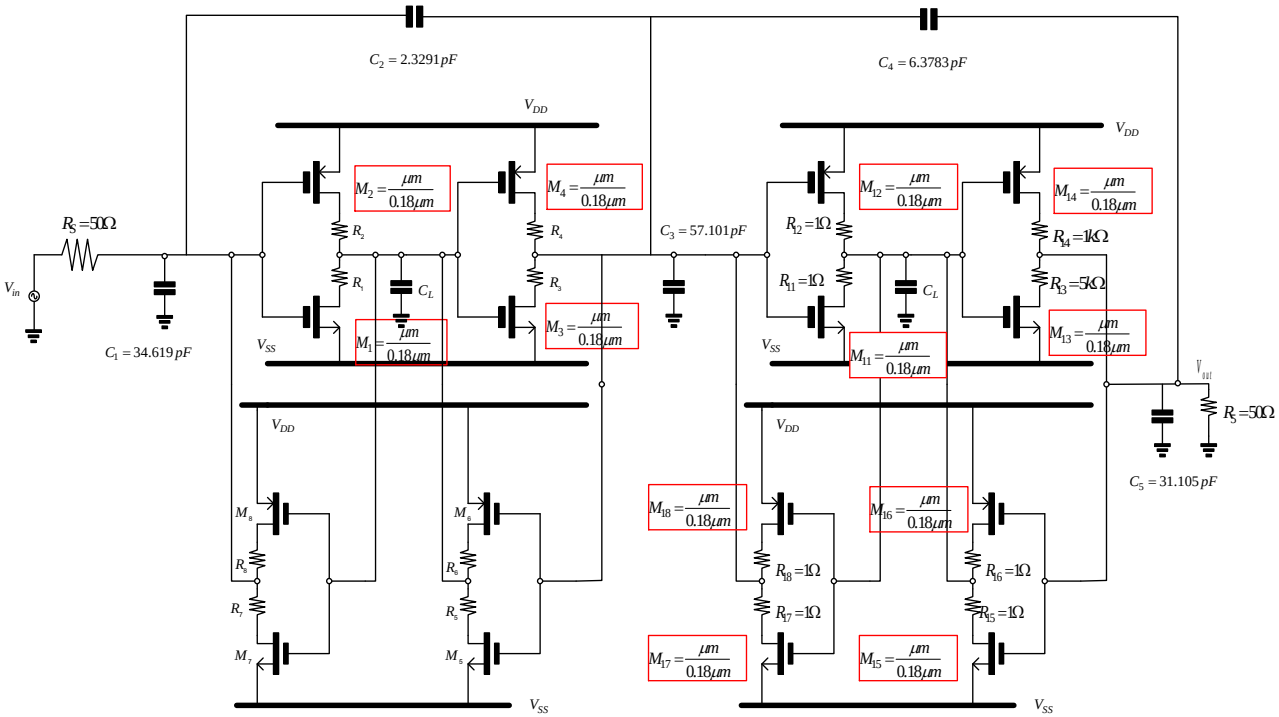

Figure 3: Transistor schematic of low power 5th order LPF with Elliptic Response

III. 5TH ORDER LPF ELLIPTIC LCD PROTOTYPE

The LCR prototype is published for the first time since 1962 [12]. There are two schematics which can implement polynomial of elliptic function. But this section is shown only one schematic which is believed to consume less current at the same cutoff frequency because it uses less inductor than the counterpart. For a typical example, this paper will design low pass filter for WLAN specification which has a cutoff frequency range from 1MHz-20MHz.

The element value of LCR prototype 5th order Elliptic LPF is designed and shown in Table 1 listed as following based on impedance scaling and frequency scaling theory which was published since 1986 [13].

Table 1
Elements Value of 5th Order LCR Prototype

$\omega_c = 1rad/s$	$f_c = 100MHz$	$f_c = 20MHz$
$R = 1$	$R_{scale} = 50$	$R_{scale} = 50$
$C_1 = 0.70813$	$C_1 = 22.54pF$	$C_1 = 112.7023pF$
$L_2 = 0.76630$	$L_2 = 60.98nH$	$L_2 = 304.9010nH$
$C_2 = 0.73572$	$C_2 = 23.419pF$	$C_2 = 117.0934pF$
$C_3 = 1.12761$	$C_3 = 35.893pF$	$C_3 = 179.4647pF$
$L_4 = 0.20138$	$L_4 = 16.025nH$	$L_4 = 80.1265nH$
$C_4 = 4.38116$	$C_4 = 139.46pF$	$C_4 = 697.2832pF$
$C_5 = 0.04985$	$C_5 = 1.5868pF$	$C_5 = 7.9338pF$

IV. LOW POWER 5TH ORDER LPF ELLIPTIC TRANSISTOR SCHEMATIC

The whole transistor schematic of low power 5th order LPF elliptic transistor schematic is depicted in Figure 3.

It can be seen that element substitution is easy to implement. It substitutes transistor schematic of floating active inductor into ideal inductor in Figure 2 from Figure 1 as shown in Figure 3.

The aspect ratio of the transistors is designed by iteratively guessing the number in Cadence Spectre. Thus, if the transconductor need more current, it can be designed as a block of transistors in parallel with itself. Because of feedback of output current in gyrator loop make dc operating point unpredictable. Multiplication factor (M.F) is used to multiply aspect ratio with a number. The unit transconductor is designed with a maximum width of the transistor which is 50 µm. (maximum size). There are two value of floating active inductor which are related with transconductance value of 0.0286 and 0.0559 mho. But the unit transconductor is simulated to have value 0.005 mho Thus, M.F are calculated to be 5.72 and 11.18, respectively.

The aspect ratio and degeneration resistors value are listed in the Table 2.

Table 2
Aspect Ratio and Resistor Value of CCSDDR Transconductor

Aspect Ratio	Aspect Ratio	Resistor	Resistor
$\left(\frac{W}{L}\right)_1 = \frac{12\mu m}{0.18\mu m}$	$\left(\frac{W}{L}\right)_{11} = \frac{12\mu m}{0.18\mu m}$	$R_1 = 10\Omega$	$R_{11} = 10\Omega$
$\left(\frac{W}{L}\right)_2 = \frac{50\mu m}{0.18\mu m}$	$\left(\frac{W}{L}\right)_{12} = \frac{50\mu m}{0.18\mu m}$	$R_2 = 4.9\Omega$	$R_{12} = 4.9\Omega$
$\left(\frac{W}{L}\right)_3 = \frac{12\mu m}{0.18\mu m}$	$\left(\frac{W}{L}\right)_{13} = \frac{12\mu m}{0.18\mu m}$	$R_3 = 1\Omega$	$R_{13} = 1\Omega$
$\left(\frac{W}{L}\right)_4 = \frac{50\mu m}{0.18\mu m}$	$\left(\frac{W}{L}\right)_{14} = \frac{50\mu m}{0.18\mu m}$	$R_4 = 19.4\Omega$	$R_{14} = 19.4\Omega$
$\left(\frac{W}{L}\right)_5 = \frac{12\mu m}{0.18\mu m}$	$\left(\frac{W}{L}\right)_{15} = \frac{12\mu m}{0.18\mu m}$	$R_5 = R\Omega$	$R_{15} = R\Omega$
$\left(\frac{W}{L}\right)_6 = \frac{50\mu m}{0.18\mu m}$	$\left(\frac{W}{L}\right)_{16} = \frac{50\mu m}{0.18\mu m}$	$R_6 = R\Omega$	$R_{16} = R\Omega$
$\left(\frac{W}{L}\right)_7 = \frac{12\mu m}{0.18\mu m}$	$\left(\frac{W}{L}\right)_{17} = \frac{12\mu m}{0.18\mu m}$	$R_7 = R\Omega$	$R_{17} = R\Omega$
$\left(\frac{W}{L}\right)_8 = \frac{50\mu m}{0.18\mu m}$	$\left(\frac{W}{L}\right)_{18} = \frac{50\mu m}{0.18\mu m}$	$R_8 = R\Omega$	$R_{18} = R\Omega$

The values of transconductance amplifiers are shown in Table 3.

Table 3
Elements Value of Transconductance of 10th Order LCR Prototype

	$f_c = 100MHz$	$f_c = 20MHz$
GmL2	0.0286 □	0.0128 □
GmL4	0.0559 □	0.0250 □

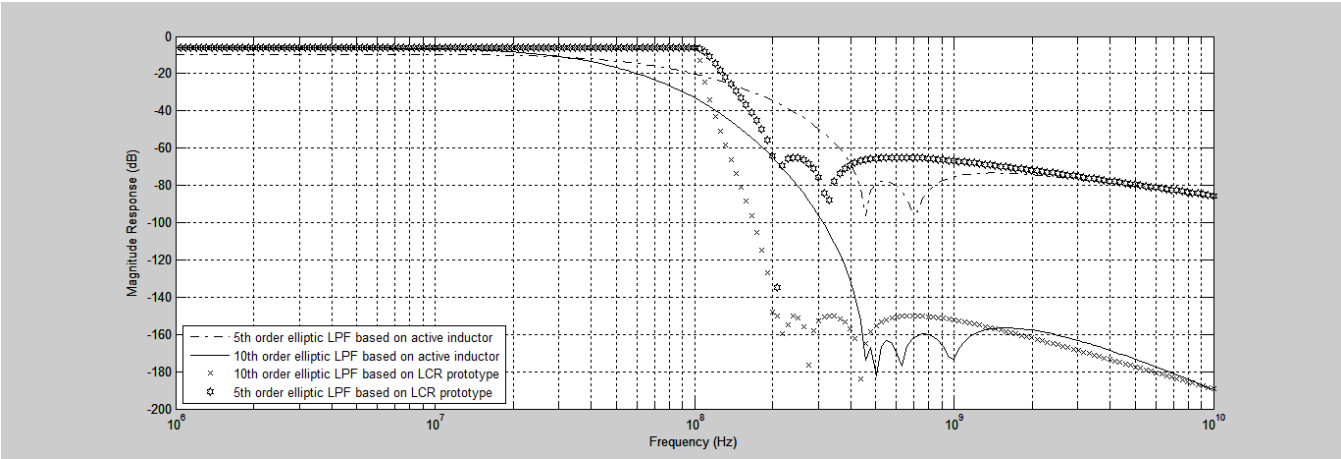

Figure 4: Magnitude response of 5th and 10th order Elliptic LPF based on Complementary common source amplifier with drain degeneration resistors (CCSDDR)

V. Simulation results of 5TH Order LPF and 10TH Order LPF

Simulation results of 5th and 10th order LPF based on the elliptic response is performed by Cadence Spectre. Transistor model is using the 0.18-micron process. It can be seen that dash dot line curve is 5th order LPF based on the active inductor and solid line curve is 10th order LPF based on the active inductor. The graph can be described as following: Passband of 10th order Elliptic LPF is steady at -6dB, its passband decreased down to -9dB at 22.37 MHz. Its magnitude response is decreased down at a rate -170dB per decade until it reaches first stop band at -174 dB, then it rises up gradually until it decreases down and reach second stop band at -182 dB, then it rises up again until it decreases down and reach third stop band at -177 dB, then it rises up again until it decreases down and reaches fourth stop band at -173 dB.

The passband of 5th order Elliptic LPF is steady at -9.5dB, its passband decrease down to -12.5dB at 43.65 MHz which should be called cutoff frequency. Its magnitude response is decreased down at a rate -90dB per decade until it reaches first stop band at -96 dB, then it rises up gradually until it decreases down and reaches second stop band at -94.9dB.

VI. Transconductor Design

Ideal transconductor can be designed based on drain current in saturation and triode region of operation. It can be seen in Figure 1 that the proposed transconductor is different from Prof. Nauta transconductor that if it is designed in Cadence and adapt drain source voltage, both transistor can operate in saturation region, but if the drain source voltage of NMOS or PMOS transistor is converged to be less than gate source voltage minus threshold voltage, it can operate in triode region. It is possible that there is a voltage drop between drain degeneration resistors very low, maybe less than microvolt, thus, the transistor may operate in the triode region.

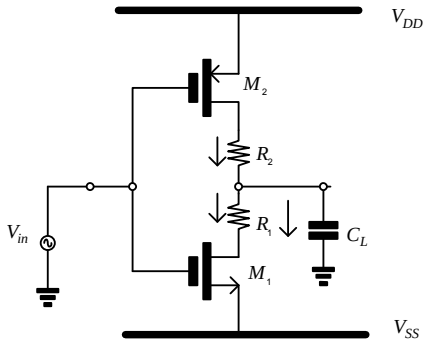

Figure 5: The proposed complementary common source with drain degeneration resistors.

Let us perform KCL at the output node of Figure 5.

$$I_{R1} + I_{OUT} = I_{R2} \tag{1}$$

Let us minus I_{R1} both sides of Equation (1), so that it can be written Equation (2). From Figure 5, it can be seen that drain current flow from M2 should be equal with I_{R2} while drain current flow from M1 should be equal with I_{R1}

$$I_{OUT} = I_{R2} - I_{R1} = I_{D2} - I_{D1} \tag{2}$$

For saturation region, the transconductance should equal with:

$$\begin{aligned} &I_{out} = \left(\frac{\mu_P C_{ox}}{2}\right)\left(\frac{W}{L}\right)_2 \left(V_{GS2} - V_{THP}\right)^2 - \left(\frac{\mu_N C_{ox}}{2}\right)\left(\frac{W}{L}\right)_1 \left(V_{GS1} - V_{THN}\right)^2 \\ &A = \left(\frac{\mu_P C_{ox}}{2}\right)\left(\frac{W}{L}\right)_2, B = \left(\frac{\mu_N C_{ox}}{2}\right)\left(\frac{W}{L}\right)_1 \end{aligned} \tag{3}$$

$$\begin{aligned} &I_{out} = A\left(V_{GS2} - V_{THP}\right)^2 - B\left(V_{GS1} - V_{THN}\right)^2 \\ &I_{out} = A\left(V_{in} - \left(V_{S2} + V_{THP}\right)\right)^2 - B\left(V_{in} - \left(V_{S1} + V_{THN}\right)\right)^2 \\ &x = \left(V_{S2} + V_{THP}\right), y = \left(V_{S1} + V_{THN}\right) \\ &I_{out} = A\left(V_{in} - x\right)^2 - B\left(V_{in} - y\right)^2 \\ &I_{out} = A\left[V_{in}^2 - 2V_{in}x + x^2\right] - B\left[V_{in}^2 - 2V_{in}y + y^2\right] \\ &\frac{\partial I_{out}}{\partial V_{in}} = 2AV_{in} - 2Ax - 2BV_{in} + 2By = G_m \end{aligned} \tag{4}$$

For triode region, the transconductance should equal with:

$$\begin{aligned} &I_{out} = \left(\frac{\mu_P C_{ox}}{2}\right)\left(\frac{W}{L}\right)_2 \left[2\left(V_{GS2} - V_{THP}\right)V_{DS} - V_{DS}^2\right] \\ &-\left(\frac{\mu_N C_{ox}}{2}\right)\left(\frac{W}{L}\right)_1 \left[2\left(V_{GS1} - V_{THN}\right)V_{DS} - V_{DS}^2\right] \\ &A = \left(\frac{\mu_P C_{ox}}{2}\right)\left(\frac{W}{L}\right)_2, B = \left(\frac{\mu_N C_{ox}}{2}\right)\left(\frac{W}{L}\right)_1 \\ &I_{out} = A\left[2\left(V_{GS2} - V_{THP}\right)V_{DS2} - V_{DS2}^2\right] - B\left[2\left(V_{GS1} - V_{THN}\right)V_{DS1} - V_{DS1}^2\right] \\ &I_{out} = A\left[2\left(V_{in} - \left(V_{S2} + V_{THP}\right)\right)V_{DS2} - V_{DS2}^2\right] - B\left[2\left(V_{in} - \left(V_{S1} + V_{THN}\right)\right)V_{DS1} - V_{DS1}^2\right] \\ &G_m = \frac{\partial I_{out}}{\partial V_{in}} = 2AV_{DS2} - 2BV_{DS1} \end{aligned} \tag{5}$$

VII. Analysis of Floating Active Inductor Block Diagram

Block diagram of floating active inductor can be shown in Figure 6. It can be analyzed by substitute voltage controlled current source into the block as shown in Figure 6.

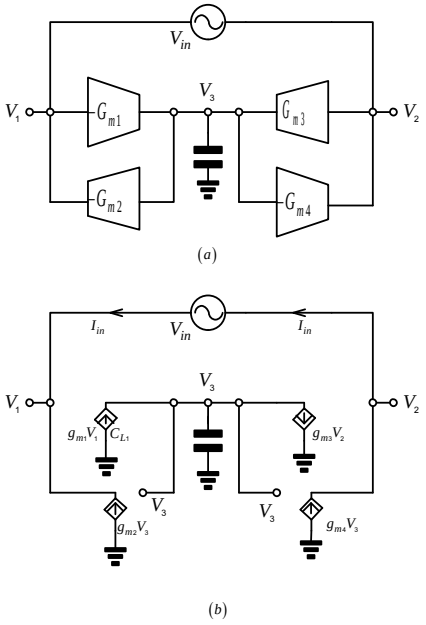

Figure 6: (a) Block diagram of floating active inductor (b) Equivalent circuit of (a)

After using KCL at all nodes in the circuit in Figure 6, the input impedance formula can be derived as Equation (6).

$$Z_{in}=\left(\frac{V_2-V_1}{I_{in}}\right)=sC_L\left(\frac{1}{g_{m4}g_{m1}}-\frac{g_{m4}+g_{m2}}{2g_{m2}g_{m3}g_{m4}+2g_{m2}g_{m1}g_{m4}}\right) \quad (6)$$

Assume that all transconductor can be designed to have equal value, even though in the simulator, it is not possible because dc operating point is not equal in every transistor in the circuit. As a result of feedback of dc operating point. Equation (6) can be reduced form to:

$$\begin{aligned} Z_{in} &= sC_L\left(\frac{1}{g_{m1}^2}-\frac{2g_{m1}}{4g_{m1}^3}\right)=sC_L\left(\frac{1}{g_{m1}^2}-\frac{1}{2g_{m1}^2}\right) \\ Z_{in} &= sC_L\left(\frac{2g_{m1}^2-g_{m1}^2}{2g_{m1}^4}\right)=s\left(\frac{C_L}{2g_{m1}^2}\right) \end{aligned} \quad (7)$$

If someone wants to write transconductance value as a function of load capacitor and inductor. Transconductance value can be derived as a function of capacitive load and inductance as following:

$$L=\left(\frac{C_L}{2G_m^2}\right)\rightarrow G_m=\pm\sqrt{\frac{C_L}{2L}} \quad (8)$$

It can be seen that three transconductance amplifier in the block diagram of Figure 6 has negative transconductance which is represented by VCVS flow out of the ground. One transconductance amplifier namely Gm3 have positive transconductance which is represented by VCVS flow into the ground.

VIII. 10TH ORDER LPF ELLIPTIC LCR PROTOTYPE

If deep notch at stopband of the low pass filter is required. Attenuation of the magnitude response of 44 dB of 5th order Elliptic LPF LCR prototype is not good enough. Thus, it proposes more attenuation at the first stopband which is maximized at order 10 of the filter to be equal with 144dB from the table of element value which was published in 1993 [6].

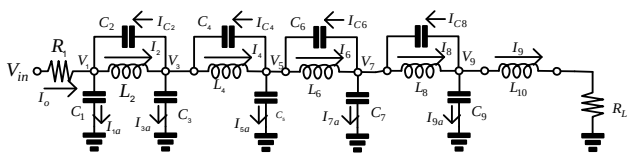

Figure 7: 10th order LPF Elliptic LCR prototype

The figure which is depicted in Figure 7 is called 10th order LPF Elliptic LCR prototype. It composed of 5 floating inductors and 4 floating capacitors and 5 grounded capacitors.

IX. DISCUSSION ON DYNAMIC RANGE AND POWER CONSUMPTION OF CONTINUOUS TIME FILTER

The dynamic range of continuous time filter is the most important specification in filter but it is very difficult to analyze with exact derivation. But in Cadence Spectre, there is a command called periodic steady state (PSS) and scattering parameter analysis (SP) which is used to analyze maximum output power of the filter and total integrated output referred noise power of the filter [14]. Current consumption of 5th and 10th order low pass filter is 84mA, 187 mA while using a supply voltage of 1.8 V.

Table 4
Elements Value of 10th Order LCR Prototype

$\omega_c=1rad/s$	$f_c=100MHz$	$f_c=20MHz$
$R=1$	$R_{scale}=50$	$R_{scale}=100$
$C_1=1.07857$	$C_1=34.332pF$	$C_1=85.83pF$
$L_2=1.47977$	$L_2=0.11776\mu H$	$L_2=1.177\mu H$
$C_2=0.03516$	$C_2=1.1192pF$	$C_2=2.7979pF$
$C_3=1.81552$	$C_3=57.790pF$	$C_3=144.47pF$
$L_4=1.61465$	$L_4=0.12849\mu H$	$L_4=1.2849\mu H$
$C_4=0.12563$	$C_4=3.9989pF$	$C_4=9.9973pF$
$C_5=1.69286$	$C_5=53.885pF$	$C_5=134.71pF$
$L_6=1.66661$	$L_6=0.13262\mu H$	$L_6=1.3262\mu H$
$C_6=0.14673$	$C_6=4.6706pF$	$C_6=11.676pF$
$C_7=1.63110$	$C_7=51.920pF$	$C_7=129.80pF$
$L_8=1.80819$	$L_8=0.14389\mu H$	$L_8=1.4389\mu H$
$C_8=0.07224F$	$C_8=2.2995pF$	$C_8=5.7487pF$
$C_9=1.46428$	$C_9=46.609pF$	$C_9=116.52pF$
$L_{10}=1.11311$	$L_{10}=88.578nH$	$L_{10}=0.88578\mu H$

Table 5
Elements Value of Transconductance of 10th Order LCR Prototype

GmL2	0.0206 □	0.0065 □
GmL4	0.0197 □	0.0062 □
GmL6	0.0194 □	0.0061 □
GmL8	0.0186 □	0.0059 □
GmL10	0.0238 □	0.0075 □

X. CONCLUSION

A design of low pass filter with on chip active inductor using 0.18-micron process is shown. The simulation results of the proposed circuit are deviated from ideal 5th and 10th order Elliptic LCR prototype because of parasitic capacitances of floating active inductor which should be based on the small signal concept. The first advantage of additional resistor called drain degeneration resistor (D.D.R) is that voltage gain can be adjusted by D.D.R. Second advantage is a systematic layout can be designed by parallel the same block of the transistor in parallel. The disadvantage is the additional silicon area consumption.

A conclusion to review the main points of the paper, do not replicate the abstract as the conclusion. A conclusion might elaborate on the importance of the work or suggest applications and extensions.

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