Evaluation of Charge Transfer Blocks in CP Circuit Topologies

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***Abstract*—Harvested energy major challenge in self-powered devices is due to its low power energy supply. Therefore, a charge pump is required to overcome this constraint. Charge pumps are inductorless DC-DC converters that have the ability to transfer charge to the high level through the effectiveness of switches to turn on and off at the designated clock phases. This paper investigates the features of charge transfer switches in two and four-phase charge pump. The charge pumps have been evaluated in terms of the output voltage and leakage current in charge transfer block. The sizing of transistor, frequency, stage and load capacitance have been optimized. The rise time has been analysed over the stage and load capacitance. The correlation on the performance of charge pump has been observed. The charge pumps have been simulated in 130nm standard CMOS process.**

***Index Terms*—Charge Pump; Charge Transfer Switches; Dickson Voltage Doubler; Two and Four-phase Charge Pump Topologies.**

I. INTRODUCTION

Leading to the improvement of wireless device technologies, they have their own challenge that is battery lifetime. This issue continues as the device operate. In order to overcome this critical issue, many researchers proposed a few methods to support the device battery using the free energy. The energy collected was harvested from ambient energy sources includes: solar, RF, vibration, and heat potentially provide indefinite lifetime through charging a rechargeable battery or super capacitor to store and provide energy to the whole device. The voltage level available from the harvested energy is not sufficient enough to drive self-powered devices or to recharge the battery. Therefore, a charge pump (CP) is used to step up the voltage and bring it to the usable level.

The charge pump (CP) are widely used to generate high voltage, as reported in [1-13]. The circuit makes use of capacitors, which are interconnected by diodes and coupled in parallel with two non-overlapping clocks. The current design, diodes have been replaced with NMOS for a better performance [4] as shown in Figure 1.

However, the threshold voltage drops and reverse charge phenomenon limit the NMOS performance. Increasing the threshold voltage may increase the output voltage, nevertheless, reduce the pumping efficiency [2, 4, 7]. To overcome the problem, a new two-phase CP has been implemented to prevent the reverse charge flow [2, 4].

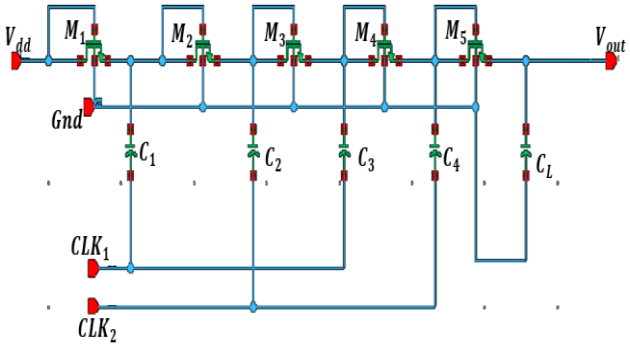

Figure 1: Two-phase of Dickson CP

This design used charge transfer switches which are controlled by pass transistors NMOS and PMOS. Then, the design of CP was extended by using two-phase of multi-staged voltage doubler which shows high efficiency of pumping voltage [2]. To reduce the transistor counts, another version of two-phase of CP design was introduced by [4] which is extended design from multi-stage voltage doubler [2]. The developed CP provides clock voltage for two stages of the transfer transistor, hence reducing the number of transistors in the design.

On the other hand, four-phase CP has been proposed in [5]. However, the original design is in switched polarity CP which can be used to generate either positive or negative output voltage based on standard low-voltage transistors. The design was implemented in 0.18µm technology by using NMOS transistors and implemented in a triple-well structure.

The purpose of this paper is to evaluate the performance of these two and four-phase CP topologies. The high output voltage will be the target of this works. The output voltage and leakage current will be analysed from these two topologies. Parametric analysis is performed on the CP topology with the best performance including the sizing of the transistor, frequency, stage capacitor and load capacitor. The design parameters demonstrate the performance correlation of the CP.

The organisation of the paper is as follows. Section II and III present the operation of two and four CP topologies respectively. Section IV compares and analyse the simulation results. Parametric analysis is presented in Section V. Section VI concludes the work.

II. TWO-PHASE OF CHARGE PUMP

The design of two-phase CP is shown in Figure 2. The supply voltage is constant at the value of V_{DD} while V_{CLK} has oscillated between 0 to V_{DD}. As the clock is at high (V_{DD}), the NMOS (M_{n5}) will be turned on and the output voltage of the inverter will be discharged to 0V. When the clock goes low (0V), PMOS (M_{p3}) will turn on because its gate voltage is 0V and its source voltage is $2V_{DD}$. The source voltage $2V_{DD}$ of PMOS transistor will charge the output capacitor of the inverter. Eventually, the output node of the inverter becomes $2V_{DD}$. So, the value of V_{out2} oscillates between 0V to $2V_{DD}$ during the operation of the clock. Same operation on V_{out1}but it has different operation polarity.

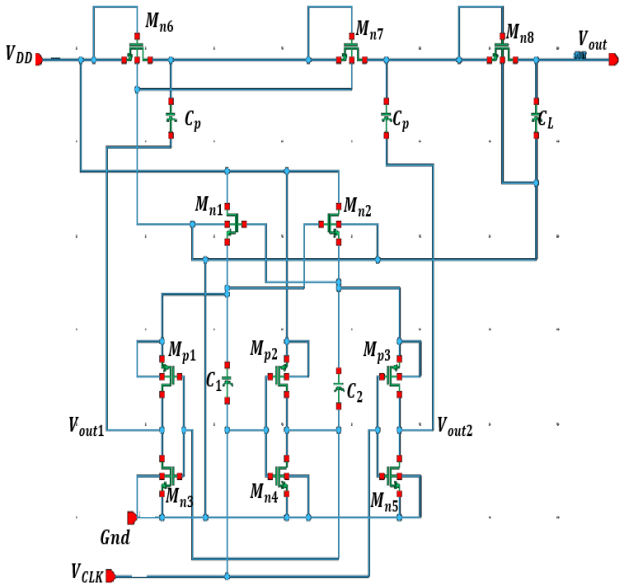

Figure 2: Two-phase CP circuit diagram

III. FOUR-PHASE OF CHARGE PUMP

The four-phase CP circuit design is presented in Figure 3. This design is using NMOS transistors and consists of two parts. The performance of charge transfer switches to generate high output voltage will be observed. Thus, this CP is designed in the standard transistor technology. M1/M2 is used to connect the bulk of their respective stage transistors (M_{pass1}/M_{pass2}) while Ma1/Ma2 and Mb1/Mb2 are used to connect the bulk of auxiliary transistors (M_{Aux1}&M_{Aux2}). C_{mid} has been applied to guarantee that the reverse voltage drop across the stage transistors is always limited to V_{DD} and also to supply the energy necessary to switch ON the auxiliary transistors. C_{blnc} is used to improve boosting the gate-source voltage of M_{pass1} during its ON state.

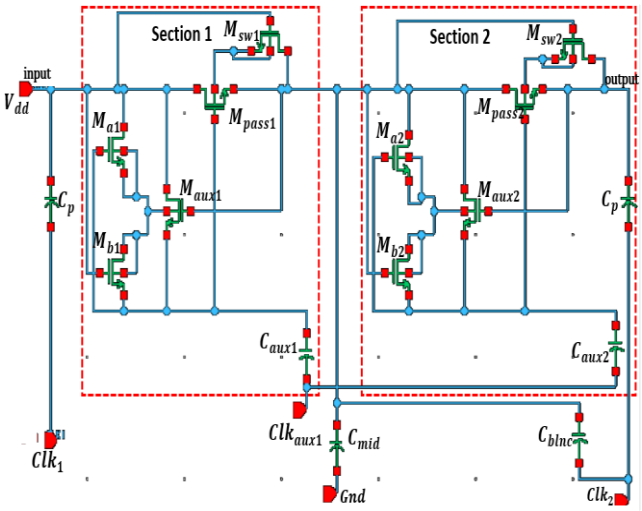

Figure 3: Four-phase CP circuit diagram

Figure 4 shows clock signal for four-phase of CP and consists of five states of operation in one period. At state 0, CLK_2 is high and CLK_1 is low. At this stage, M_{Aux1}/M_{Aux2} are ON and stage transistors M_{pass1}/M_{pass2} are OFF. At state 1, capacitor C_{Aux1} will be charged through M_{Aux1} as CLK_1 goes high. When CLK_2 goes low at state 2, M_{Aux2} will switch OFF while C_{Aux1} is still charging. Next, at the state 3 where CLK_{Aux1} goes high, M_{Aux1} will be OFF and the gate voltage of the stage transistors will be boosted through the auxiliary capacitor (C_{Aux1}/C_{Aux2}). The stage transistor will be ON leading to charge transfer from input to output. During the high state of CLK_1, current will flow through stage transistors charging node C_{mid} while C_p connected to the output side. When CLK_{Aux1} goes low, the current through stage transistor will be reduced further toward zero because of the reduced voltage on their gates. When CLK_2 goes high at state 4, M_{Aux2} will be ON causing M_{pass2} to switch OFF and reverse voltage across drain-source of M_{pass2} will be slightly less than V_{DD}. At the last of state 5, CLK_1 will go low, M_{Aux1} will be ON and CLK_{Aux1} discharges through M_{Aux1} and C_p. Hence, M_{pass1} will be OFF and reverse voltage across its drain-source terminal will be slightly less than V_{DD}.

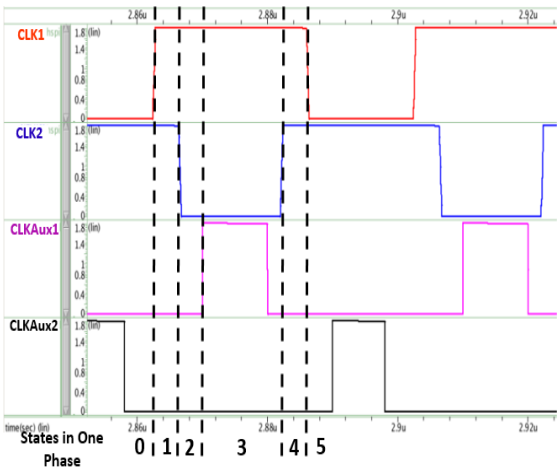

Figure 4: Clock scheme for four-phase of CP topology

IV. SIMULATION RESULTS

Simulations of two and four-phase CP topologies have been performed and both circuits have been designed using Synopsys Custom Designer. Table 1 shows the parameters that have been applied. Output voltage and leakage current have been observed in subsection A and B.

Table 1
Design Parameters in CP

Topology	Two-phase CP	Four-phase CP
Technology	130nm	130nm
No. of stages	4	4
Supply Voltage	1.8V	1.8V
Frequency	25MHz	25MHz
Stage Capacitor	3pF	3pF
Load Capacitor	6pF	6pF
W/L NMOS	2µm/ 0.13µm	2µm/ 0.13µm
W/L PMOS	5µm/ 0.13µm	

Output Voltage

Transient analysis of output voltage for two-phase and four-phase CP in four stages topologies have been simulated as shown in Figure 5. Output voltage two-phase CP is 8.21V and has 0.001V ripple voltage, ΔV. The output voltage for four-phase CP is 5.44V while the ripple voltage is 0.35V. Two-phase achieved higher output voltage compared to four-phase. In terms of ripple voltage, four-phase shows a higher ripple compared to two-phase CP. Higher ripple degrades the performance of charge pump. Ripple could be reduced by applying larger capacitor. However, die area is consumed by having a bigger size of the capacitor.

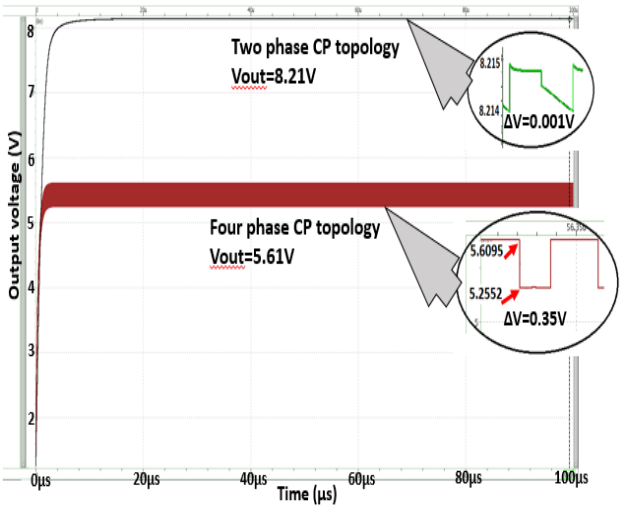

Figure 5: Transient analysis on output voltage for two and four-phase CP topologies

Leakage Current

Leakage current in the charge transfer block of two and four-phase CP have been obtained and shown in Figure 6. The simulation result shows that the leakage current of two-phase is 40µA while four-phase is 5µA and 7µA respectively. This because of the connection of bulk in four-phase CP has been biased appropriately as presented in section III. This action eliminates the body effect and maintains reverse biased to stop leakage current from occurring.

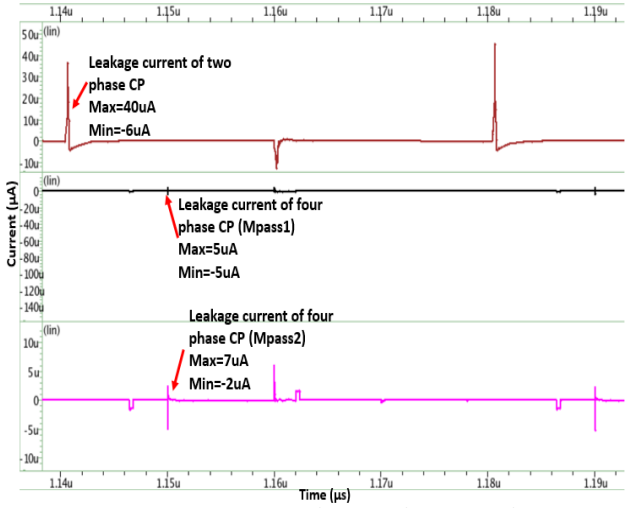

Figure 6: Leakage current analysis of two and four-phase of CP topologies

Figure 7a shows voltage across drain-source while Figure 7b is the result of the voltage across gate-source in CP topologies. The voltage across drain-source is measured as the value must be always lower than V_{DD}. The voltage across drain-source, V_{DS} is 0.6V and 1.2V for four-phase and 2V for two-phase CP. This shown that the two-phase CP has stronger charge pass through across stages compared to four-phase CP. The voltage across gate-source, V_{GS} has been observed. For four-phase CP, V_{GS} is 1.4V and 1.2V while two-phase CP is 2.2V. This happens because of the diode-connected in two-phase CP circuit is used to transfer charges from the present stage to the next stage. When the diode-connected is turn off to prevent the charges flowing back to the previous stage, the voltage across the gate-oxide of the diode-connected is around 2 x $V_{DD} - V_t$, where V_t is the threshold voltage of diode-connected. The diode-connected and the charge transfer switches suffer serious high voltage overstress on the gate oxide.

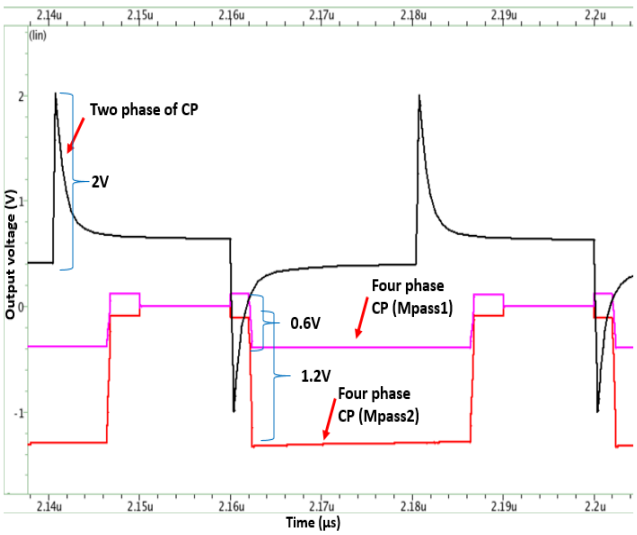

Figure 7a: Voltage across drain-source

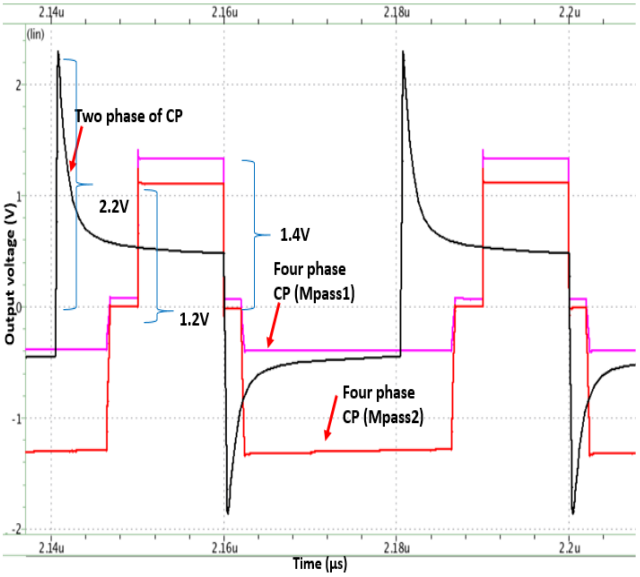

Figure 7b: Voltage across gate-source

V. PARAMETER OPTIMIZATION ON TWO-PHASE CP

Two-phase CP topology has been proceeded to the parameters optimization on operating frequency, sizing of the transistor, stage capacitance and load capacitance.

Effects on the operating frequency have been investigated. Figure 8 shows the result which the frequency has been swept from 25MHz to 500MHz. The output of the two-phase CP shows a slightly degrades across the frequencies. Decreasing of the output voltage in four-phase CP is significant as increasing the operating frequency. This also reduced the pumping capacitor. Hence this resulting in a lower pumping voltage. From both results obtained, concludes, increasing the frequency will reduce the output voltage proved by Equation (1). Therefore, in terms of operating frequency, two-phase CP is a compatible design for an application that operates in wide operating frequency compared to four-phase CP.

$$V_{out} = (N+1)V_{DD} - \frac{NI_{out}}{fC_p} - N(V_{ohm} + V_{stry}) \quad (1)$$

Where V_{ohm} represents the ohmic voltage drop across stage transistors and clock drivers while V_{stry} represents voltage loss due to stry capacitances respectively.

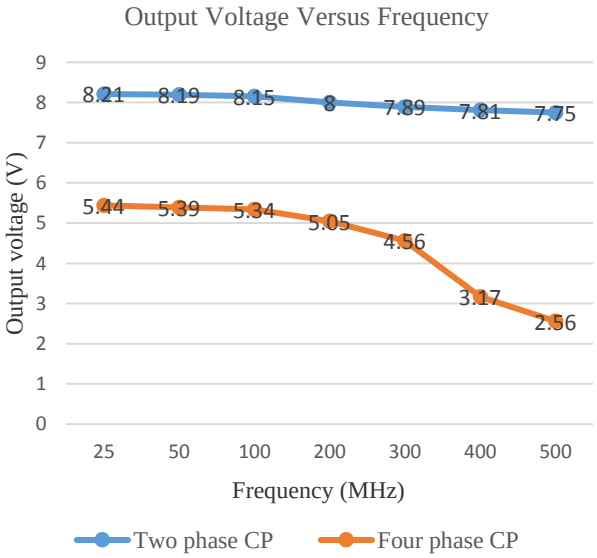

Figure 8: Output voltage versus frequency

Figure 9 shows the result of the output voltage of sweeping the NMOS width parameter. The correlation between width over output voltage has been observed. The minimum value of width gave the better result. On the other hand, PMOS transistor has been fixed to 25µm since it only involved in the inverter parts of the circuit design. There are no significant changes of PMOS output voltage occur when the width is varied. The optimized length of transistor value is 0.15µm and the correlation of output voltage over length as shown in Figure 10. Utilising small length of transistor size is more efficient since it may reduce the on-resistance. A higher value of on-resistor contributes deterioration of charge pump performance.

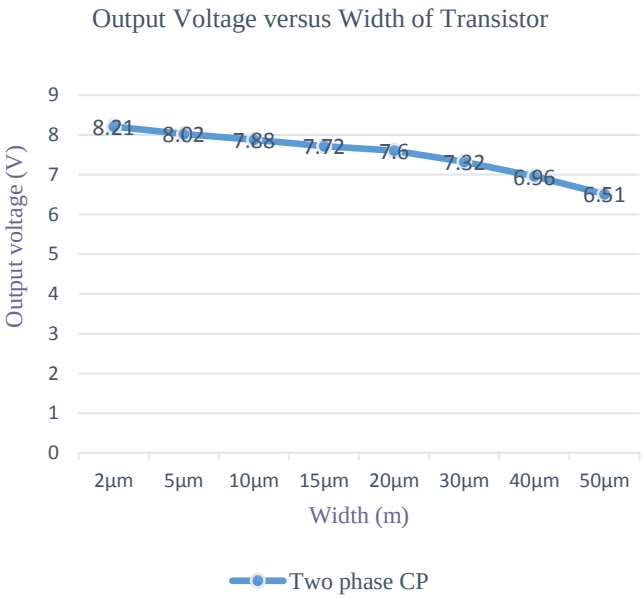

Figure 9: Output voltage versus width of transistor

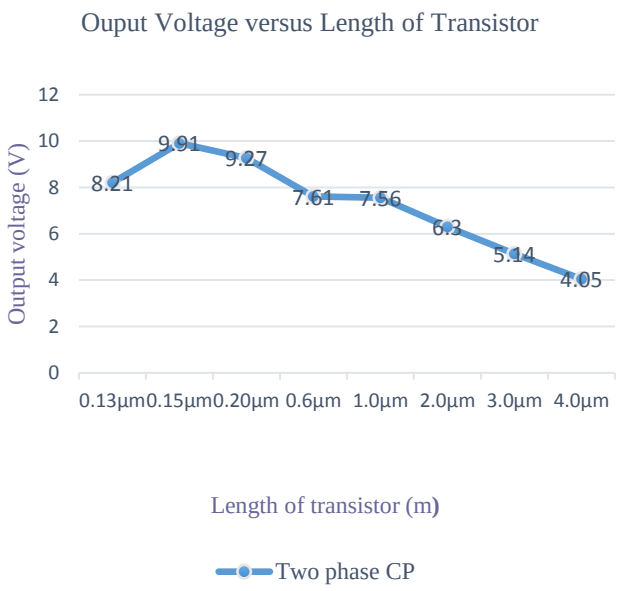

Figure 10: Output voltage versus length of transistor

The correlation between stage capacitor and load capacitor have been presented in Figure 11. The stage and load capacitance have been swept. The higher output voltage is obtained at 6pF and 1pF respectively. By utilising smaller capacitance in CP design, significantly reduce the chip area size. The important issue to consider in a practical design of a CP is rise time. It is depicted as the output voltage of the CP with respect to time. The rise time of CP is a consequence of stage and load capacitance. Relation of the rise time over capacitance has been shown in Figure 12. It can be concluded that smaller stage and load capacitance achieve faster rise time than the bigger size of capacitance.

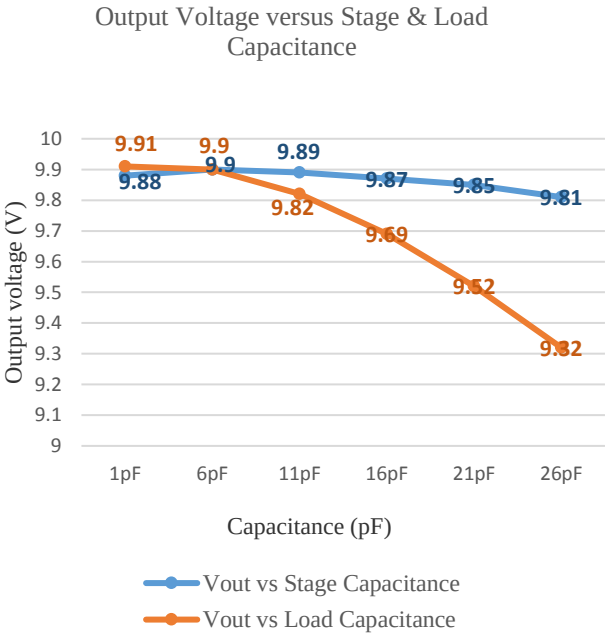

Figure 11: Output voltage versus stage and load capacitance

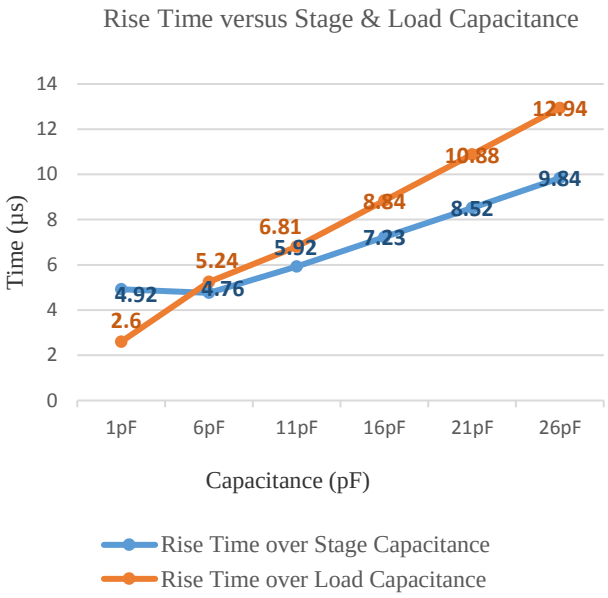

Figure 12: Rise time versus stage and load capacitance

VI. CONCLUSION

In this paper, evaluation on charge transfer blocks of two and four-phase CP topologies have been performed in terms of its output voltage and leakage current. Two-phase CP achieves higher output voltage compared to four-phase CP. However, four-phase has lower leakage current due to the effectiveness of bulk control. The gate-oxide, V_{GS} overstress occurred on two-phase as the voltage across gate-source and drain-source is higher than V_{DD}. Optimization on two-phase topology has been performed to evaluate output voltage on the transistor sizing, frequency, stage and load capacitance and rise time. Increasing the operating frequency resulting in lower pumping voltage. Applying a small length of transistor size is more efficient on the output voltage where it reduces the effect of on-resistance. Evaluation of stage and load capacitance is crucial as they are dominant in chip size area and rise time. After all the optimization procedure were taken, the output voltage has been successfully increased from 8.21V to 9.91V.

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