Control Factors Optimization on Threshold Voltage and Leakage Current in 22 nm NMOS Transistor Using Taguchi Method

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***Abstract*— In this article, Taguchi method was used to optimize the control factor in obtaining the optimal value which is also known as response characteristics, where the threshold voltage (V_{th}) and leakage current (I_{leak}) for NMOS transistor with a gate length of 22 nm is taken into account. The NMOS transistor design includes a high permittivity material (high-k) as a dielectric layer and a metal gate which is Titanium Dioxide (TiO_2) and Tungsten Silicide (WSi_X) respectively. The control factor was optimized in designing the NMOS device using the Taguchi Orthogonal Array Method where the Signal-to-Noise Ratio (SNR) analysis uses the Nominal-the-Best (NTB) SNR for V_{th}, while for I_{leak} analysis, a Smaller-the-Better (STB) SNR was used. Four manufacturing control factors and two noise factor are used to optimize the response characteristics and find the best combination of design parameters. The results show that the Halo implantation tilting angle is the dominant factor where it has the greatest factor effect on the SNR of the I_{leak} with 55.52%. It is also shown that the values of V_{th} have the least variance and the mean value can be set to 0.289 V ± 12.7% and I_{leak} is less than 100 nA/µm which is in line with the projections made by the International Technology Roadmap for Semiconductors (ITRS).**

***Index Terms*—22 Nm NMOS Tio_2/Wsi_x; High-K/Metal Gate; Threshold Voltage; Leakage Current; Taguchi Method.**

I. INTRODUCTION

Advances in research and development in the complementary metal-oxide-semiconductor (CMOS) technology caused a huge increase in the semiconductor technology growth. Since silicon dioxide (SiO_2) was used as an effective gate dielectric layer over the decades, the downscaling CMOS dimension into nanoscale regime causes the decreasing of gate length dimension and the thickness of the SiO_2 gate layer also effected. This can cause many disadvantages in CMOS characteristics such as the gate leakage current increase leading to short channel effects (SCEs) phenomenon [1]. Therefore, a lot of researchers switch to the high permittivity (high-k) dielectric to replace SiO_2 as a CMOS dielectric gate since it offers many advantages than SiO_2 layer [1, 2]. The International Roadmap for Semiconductor Technology (ITRS) provides a list of informative device characteristics for researchers as a guide to reduce the MOSFET dimension.

In our previous work, only control factors on the V_{th} of the 22 nm gate length NMOS was successful studied as the V_{th} is one of the physical parameters that influence the functionality of the CMOS device [3]. In this paper, the research continued using Taguchi Method by studying the V_{th} and I_{leak} of the device. Since V_{th} and I_{leak} are one of the important physical parameters, there are several methods to obtain the good profile and characteristic of the device by changing the fabrication's parameter of the device [4]. V_{th} is the minimum gate voltage required to create a channel between source and drain. When the CMOS device becomes smaller, it also makes the channel length between source and drain become short and it will lead current leaks through the source and drain channel even the transistor is in off position. To increase the V_{th}, the I_{leak} should also be kept as low as possible in order to maximize the device performance [5]. Each technique in order to reduce the I_{leak} can cause short channel effect, so the designer must scale the device very carefully in obtaining the optimized device.

This paper will explain the optimization process on control factors of NMOS transistor using L_9 Taguchi method which uses an orthogonal array to evaluate the entire control factor with only a small number of experiments [6]. This method consists of SNR in order to analyze the experimental data in identifying the optimal parametric combinations in a simple way [7]. In this experiment, the SNR that involved are SNR (NTB) and SNR (STB). SNR (NTB) is to find and optimize the control factors so that the final value could be the same or as close as the target value which is also identified as the nominal value. While SNR (STB) is analysis to achieve the value to be smaller or minimum as could. SNR (NTB) belongs to V_{th} where we want to optimize the control factor to be as close to the target value, while SNR (STB) belongs to I_{leak} where our target is to achieve minimum I_{leak} [7, 8]. The research objective is to meet the ITRS prediction specification for 22 nm gate length NMOS transistor with the V_{th} value of 0.289V ± 12.7% and the lowest I_{leak} value as could with the maximum value of 100 nA/µm [10].

II. MATERIALS AND METHODS

A. Fabrication using TCAD Simulation Tools

NMOS device was virtually designed with the ATHENA module. The sample was initiated by the production of a P-well based wafer with the dose of boron ions for $3.75x10^{12}$.

The next step was to produce a thickness of 130 Å Shallow Trench Insulator (STI) consist of Boron Difluorite (BF_2) that functioned as the threshold-adjustment implantation. The TiO_2 was then deposited as the high-k material with 2 nm thickness followed by an etching process to produce a gate length of 22 nm. WSi_x which is the metal gate material in this research was produced to form metal gate structure [8].

Then, the device was annealed at a temperature of 850 °C while Halo implantation was carried out to obtain optimum performance which indium is implanted with a dose of $20.45x10^{12}$ ions / cm^2 and 35° tilting angle and was varied to obtain the best target value. Spacer structure which located at source and drain regions is then formed. The source-drain implantation process with doses of arsenic and phosphorus ion took place. The following process has been the development of the Borophosphosilicate glass layer (BPSG). Then, the wafer was being annealed at 850 °C. The process of compensation implantation by phosphorus dose in order to improve electrical profile then took place.

To complete the device structure, the metal gate contact is formed by the aluminum layer. At this stage, the simulation design of the 22 nm NMOS device is completed, as illustrated in Figure 1 and Figure 2 which shows the list of material and the doping profile of the device respectively. Finally, the transistor went through to the analysis process on the electrical characteristics using ATLAS simulation tools in term of V_{th} and I_{leak} with referring to the prediction of ITRS.

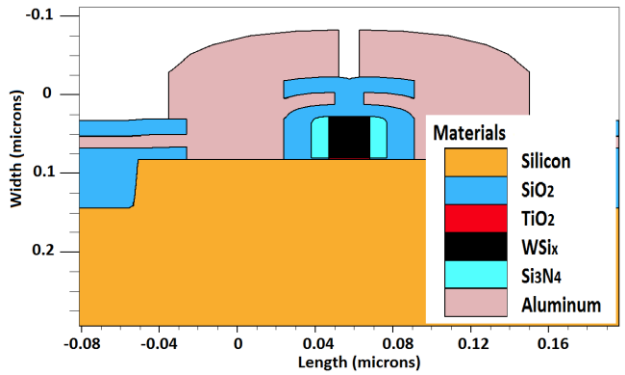

Figure 1: The NMOS transistor with TiO_2/WSi_x gate structure

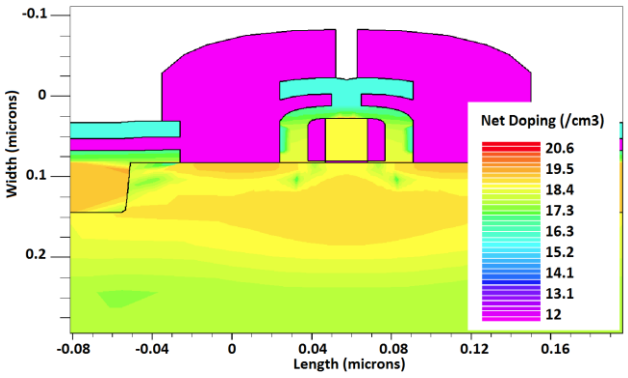

Figure 2: The doping profile of the NMOS transistor

B. The L_9 Taguchi Orthogonal Array Method

The optimizations of the NMOS device can be successful implemented by changing control factor individual. The list of all control factors and noise factors with their levels that involved in the experiment are listed in Table 1 and Table 2 respectively. The L_9 Taguchi orthogonal array experimental layout can be referred to [11].

Table 1
Control Factors

Factor	Control Factor	Unit	Level		
			1	2	3
A	Halo Implantation Dose (10^{12})	Atom/cm^3	20.40 (A_1)	20.45 (A_2)	20.50 (A_3)
B	Halo Implantation Tilting Angle	Degree	33 (B_1)	35 (B_2)	37 (B_3)
C	Oxide Growth Annealing Temperature	°C	808 (C_1)	810 (C_2)	812 (C_3)
D	Metal Gate Annealing Temperature	°C	848 (D_1)	850 (D_2)	852 (D_3)

Table 2
Noise Factors

Factor	Noise Factor	Unit	Level 1	Level 2
X	PSG Annealing Temperature	°C	900 (X_1)	902 (X_2)
Y	BPSG Annealing Temperature	°C	850 (Y_1)	852 (Y_2)

III. Result and Discussion

The control factors were optimized using Taguchi Method and best design will be predicted and verified. The results of V_{th} and I_{leak} obtained were analyzed in order to determine the optimum control factors for the device.

C. Electrical Characteristics of NMOS Transistor

The electrical characteristic of the designed NMOS transistor is shown in Figure 3 and Figure 4 respectively. Figure 3 shows the graph of Id versus Vd and Figure 4 shows the graph of Id versus Vg.

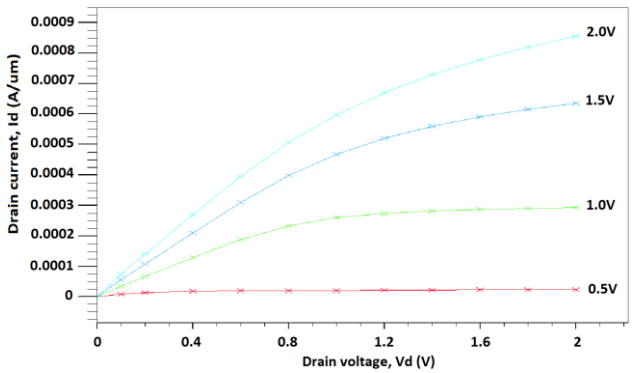

Figure 3: Id versus Vd

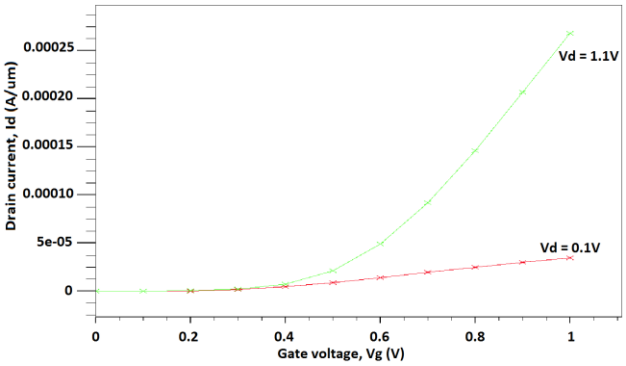

Figure 4: Id versus Vg

D. V_{th} and I_{leak} Analysis using Taguchi Method

The L_9 Taguchi method analysis for V_{th} and I_{leak} in this experiment consist of a total 36 simulation runs respectively. The completed simulation results for both V_{th} and I_{leak} are shown in Table 3 and Table 4 respectively.

Table 3
V_{th} Value for NMOS Device

Exp.	Threshold Voltage (Volts)			
	X_1Y_1	X_1Y_2	X_2Y_1	X_2Y_2
1	0.27584	0.27452	0.27594	0.27462
2	0.24246	0.24132	0.24249	0.24133
3	0.30813	0.30713	0.30855	0.30756
4	0.23408	0.23341	0.23409	0.23343
5	0.28755	0.28620	0.28801	0.28666
6	0.43549	0.43380	0.43568	0.43399
7	0.33013	0.32890	0.33080	0.32958
8	0.30311	0.30185	0.30320	0.30193
9	0.40376	0.40229	0.40380	0.40233

Table 4
I_{leak} Values for NMOS Device

Exp.	Leakage Current (nA/μm)			
	X_1Y_1	X_1Y_2	X_2Y_1	X_2Y_2
1	3.74140	3.78127	3.73861	3.77841
2	5.08231	5.13054	5.08083	5.12903
3	2.72900	2.75393	2.71674	2.74158
4	5.97259	6.03354	5.97091	6.03182
5	3.27597	3.31484	3.26188	3.30061
6	0.96864	0.97895	0.96759	0.97788
7	2.21109	2.22659	2.20086	2.21631
8	2.76319	2.79723	2.76131	2.7953
9	1.24103	1.25096	1.24068	1.2506

After completed the experiment, the next step was to analyze the control factors that give the most contribution on the device characteristics. One of the processes is to determine the SNR analysis of the experiment. As mention before, the V_{th} analysis in this experiment is referred to SNR (NTB) where the aim of the analysis is to discover the level of control factors that gives the final result value with closely or same to a target value. In this case, the target value for V_{th} is 0.289V. While for the I_{leak} analysis, the SNR of Smaller-the-Better (STB) is best uses where in the best device performance practice, the better device is the device with less I_{leak} and the best device is 100% performed with zero I_{leak}. But on a real device, it is impossible to achieve zero I_{leak}. Therefore, there is a limit value for the working device where the maximum acceptance of I_{leak} value is 100 nA/μm.

For The SNR (NTB), η_{NTB} can be expressed as [11]:

$$\eta_{NTB} = 10Log_{10}\left[\frac{\mu^2}{\sigma^2}\right] \quad (1)$$

where: μ_{NTB} = the mean
σ_{NTB} = the variance.

While the I_{leak} of the device is optimized using SNR (STB), η_{STB} can be expressed as:

$$\eta_{STB} = -10Log_{10}\left[\frac{1}{n}\sum_{i=1}^{n} y_i^{\,2}\right] \quad (2)$$

where: n = number of tests
Y_i = the experimental value of the I_{leak}.

By applying the formula given in Equation (1) and Equation (2), the η_{STB} and η_{NTB} were calculated and given as in Table 5.

In the SNR analysis, the best performance of control factor combinations is indicating by the experiment that resulted with higher SNR value. Referring to Table 5, the SNR analysis for V_{th} value shows that row 3 and row 4 gives the highest SNR values of 53.87 dB and 55.71 dB respectively. While for I_{leak}, the highest SNR values of 180.24 dB and 178.09 dB were obtained for row 6 and row 9 respectively. These values indicate that the control factor combinations give the best insensitivity for the response characteristics. As a reminder, for the orthogonal experiment, the effect of each control factor on the SNR at each experiment can be separated out. The SNR for each level of the control factors is summarized in Table 6 and Table 7, both for the V_{th} and the I_{leak}.

E. Analysis of Variance (ANOVA)

In the Analysis of Variance (ANOVA), the priority of the control factors with respect to the V_{th} and I_{leak} were examined to define the accuracy of the optimum combinations. It also can be used to investigate the percentage of contribution in the performance characteristics influenced by control factors. The result of ANOVA for SNR (NTB) and SNR (STB) can be obtained in Table 8. The percentage of factor effect on SNR indicates the priority of a control factor to minimize variation. The high percentage of a factor effect on both characteristics means it has the most influence on the stability of the device [5, 12].

Based on Table 8, it shows that for Factor A which is Halo implantation dose, the factor effect percentage for I_{leak} is higher (21.50%) than that obtained for the V_{th} (8.97%) analysis. While the Halo implantation tilting angle (Factor B) has the greatest effect on the I_{leak} with 55.52% compared to the V_{th} (32.75%) and can be considered as the dominant factor. Factor C (oxide growth annealing temperature) affects the V_{th} with a value of 17.41% more than the I_{leak} (10.15%). Last but not least, for the Factor D (metal gate annealing temperature), the control factor influenced more in V_{th} compare to I_{leak}. Therefore, referring to Table 6 and Table 7, the level values with the highest SNR are selected to be the best settings for the 22 nm NMOS device which is A_3 B_2 C_2 D_3. Their best setting of control factor values is shown in Table 9.

Table 5
SNR Analysis

Exp No.	SNR (dB)	
	Threshold Voltage	Leakage Current
1	51.12	168.50
2	51.27	165.84
3	53.87	171.26
4	55.71	164.43
5	50.86	169.66
6	52.92	180.24
7	52.21	173.10
8	52.31	171.12
9	53.54	178.09

Table 6
SNR (NTB) for V_{TH}

Factor	SNR NTB (Mean), dB		
	Level 1	Level 2	Level 3
A	52.09	53.17	52.69
B	53.01	51.48	53.44
C	52.12	53.51	52.31
D	51.84	52.14	53.97

Table 7
SNR (STB) for I_{LEAK}

Factor	SNR STB (Mean), dB		
	Level 1	Level 2	Level 3
A	168.53	171.44	174.10
B	168.68	176.53	168.87
C	173.28	169.45	171.34
D	172.08	173.06	168.94

Table 8
Result of ANOVA

Factor	Factor Effect on SNR (NTB) (%)	Factor Effect on SNR (STB) (%)
A	8.97	21.50
B	32.75	55.52
C	17.41	10.15
D	40.87	12.83

Table 9
Best Setting of the Control Factors

Factor	Level	Best Value
A	3	$20.5x10^{12}$
B	2	35
C	2	810
D	3	852

Table 10
Final Simulation with Added Noise

Noise (°C)	V_{th} (V)	I_{leak} (nA/µm)
(X_1,Y_1)	0.30266	2.77693
(X_1,Y_2)	0.30140	2.81094
(X_2,Y_1)	0.30271	2.77537
(X_2,Y_2)	0.30144	2.80936

These final control factors were then simulated with different parametric values of the noise factors to get the optimal result of V_{th} and I_{leak} as noted in Table 10. Finally, the control factor combination of A_3 B_2 C_2 D_3 X_1 Y_2 shows the best combination where the V_{th} value of 0.3014V resulted in the closest value to the ITRS prediction by 4.29% (ITRS range: ±12.7%), and in the same time I_{leak} resulted with almost 97% away and lower from maximum value as predicted from ITRS. Well said, both these values are in line with the ITRS predictions. As a result, Taguchi Method is proven to be a capable method to predict the optimum solution in obtaining the optimal fabrication recipe for a 22 nm TiO_2/WSi_x planar NMOS with compliant V_{th} and I_{leak} values.

IV. Conclusion

As a conclusion, the best fabrication control factor settings for a 22nm TiO_2/WSi_x planar NMOS transistor using Taguchi method was successfully achieved. The Halo tilting angle has been identified to be the dominant factor in determining the value of both the V_{th} and the I_{leak}. The parametric combination of the process factors which include noise factors have resulted in the successful development of the nanoscale NMOS device with the combination of control factor A_3 B_2 C_2 D_3 X_1 Y_2 was the best combination in order to achieve the best V_{th} which closest to the nominal value and minimum I_{leak} where these values comply with the specifications given in ITRS and these values also reported by another researcher [11, 12].

Our future work involves developing the device using more fabrication's process parameters. We will also optimize both the V_{th} and the turn-on/turn-off current for the 22nm gate length NMOS device using extended Taguchi's method in the future.

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