V_{TH} and I_{LEAK} Optimization Using Taguchi Method at 32nm Bilayer Graphene PMOS

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***Abstract*—A 32nm top-gated bilayer Graphene PMOS transistor was optimized and analyzed to find the optimum value of performance parameters besides investigating the process parameter that affects the performance of the bilayer Graphene transistor the most. Firstly, ATHENA and ATLAS modules which can be found in Silvaco TCADS Tools were employed to simulate the virtual device fabrication process and to confirm the electrical features of the device, respectively. L9 Taguchi robust analysis was then applied to enhance the device process parameters for the finest threshold voltage (V_{TH}) and lowest leakage current (I_{LEAK}) following the International Technology Roadmap for Semiconductor (ITRS) 2011 prediction. The parameters being optimized were the Halo implantation, Halo tilting angle, S/D implantation and compensation implantation which were varied at three levels and two levels of noise factor. The noise factors include sacrificial oxide layer temperature and BPSG temperature. The results of this work show that compensation implantation and Halo implantation are the most dominant factors in affecting the V_{TH} and I_{LEAK} respectively. Optimized results show an excellent device performance with V_{TH} of -0.10299V which is 0.0097% closer to ITRS2011 target and I_{LEAK} is 0.05545673nA/um which is far lower than the prediction.**

***Index Terms*—ITRS2011; Graphene; ATLAS; ATHENA; L9 Taguchi Method.**

I. INTRODUCTION

Nourishing the Moore's Law while meeting the demands for low power high performance in electronic systems have led to an invention of a novel device structures and implementation of a novel materials. This invention has been advised by the International Technology Roadmap for Semiconductors (ITRS) for a successful device scaling in the following 15 years [1]. In terms of a planar geometry, MOSFET device has changed from a conventional SiO_2/Poly-Si MOSFET to a High-k metal gate. Recently, 2-dimensional carbon material known as graphene has slowly gained popularity in the design of planar MOSFET. Due to its excellent properties, single layer and bilayer Graphene have been applied as the channel material for transistor device. Monolayer graphene was first exploited due to the outstanding gate control over the channel. However, it was then restricted due to an absenteeism of energy gap [2]. Bilayer graphene was then introduced together with the utilization of pairing High-k metal gate as the top gate in order to create the bandgap, modulates the drain current and limits the carrier mobility through the channel. Tunneling Field Effect Transistors (FETs) was also introduced to produce such a smooth path of either electrons or holes to be inoculated into graphene channel and thus achieved a unipolar conduction [3] just by increasing the dopant level of Silicon S/D which forms Schottky Tunneling junction.

At this stage, the top-gated bilayer graphene has been simulated [4] in evaluating the device performance and now will undergo the optimization steps using the robust analysis of Taguchi method. The purpose was to investigate the manner in which different parameters affect the S/N ratio and mean factor of a device performance. The results also outline how well the whole process is operating. This at once will help for the production of a high-quality device at low cost to the manufacturer. The top-gated that was utilized in this research are Hafnium Dioxide (HfO_2) and Titanium Silicide ($TiSi_2$).

In this paper, the optimization of the process parameter of top-gated bilayer Graphene transistor was explored and benchmarked against the International Technology Roadmap for Semiconductor (ITRS) 2011. The dependencies of process parameters on the device performance were analyzed and discussed. The paper is prepared as follows: a brief introduction is in section I. The experiment descriptions which include the fabrication procedures, semi analytical approach for bilayer graphene and Taguchi method are described in section II. In section III, the results are analyzed and discussed. The concluding observations are presented in section IV.

II. EXPERIMENT DESCRIPTIONS

A. Virtual Fabrication of 32nm Bilayer Graphene PMOS

Bilayer Graphene transistor of a 32nm gate length was virtually fabricated thru ATHENA. The steps of the fabrication follow the same conventional top-down transistor compatible process flow with a variation in several process parameters which lie within doping density and annealing temperature in order to get the result as benchmarked by International Technology Roadmap for Semiconductor (ITRS) prediction. Firstly, a highly-doped Boron concentration of Silicon wafer (100) was prepared before it was oxidized to a SiO_2 layer. It was done to form the n-well and to make sure that the Boron atoms were well spread in the wafer which minimized the channeling effect. It was then

annealed to repair the lattice damage [5] before the Shallow Trench Isolator (STI) processes took place to separate the neighboring devices. The wafer was then oxidized in a dry Oxygen before smearing the low-pressure chemical vapor deposition process (LPCVD) for depositing a Nitride layer. Next was placing a photo resist which was developed using a photolithography technique before the Nitride layer and pad oxide was etched to complete the trench preparation. The active region lies under the protected area of Si_3N_4 mask [6, 7]. A highly doped of bilayer Graphene was then atomically placed on top of the SiO_2 layer. Material characteristics of Graphene layer used in this work followed the established simulation in [8-11]. The high dopant concentration offered a smooth path for either electrons or holes to be injected into the channel at a time and achieved a unipolar conduction at once.

A High-k metal gate layer with a length of 32nm was then placed on top of the Graphene layer with a thickness of 0.67nm for Hafnium Dioxide (HfO_2; k~22) and a thickness of 38nm for Tungsten Silicide ($TiSi_2$). Halo was implanted at a dopant level of 10^{13}atom/cm^3 to suppress the hot electron effect followed by highly doped of Boron for source-drain implantation with a dopant level of 10^{13}atom/cm^3 to accrue the Schottky channeling effect. The whole implantation process was tilted at various tilting angle to make sure that all sides of the device were implanted properly and hence boost the transistor performance [7]. Next, a layer of Boron Phosphor Silicate Glass (BPSG) was deposited and annealed on the surface substrate to form a premetal dielectric (PMD) which acts as an insulator for multilevel interconnection. BPSG was then etched to create source-drain contacts. The first step of metallization was achieved by placing and etching the Aluminum on the contacts before depositing the second level of the intermetal dielectric (IMD) layer of BPSG on the surface. The IMD was then etched and the whole process of virtually designing the transistor finished right after the Aluminum was placed again onto the contacts [6].

The fabrication recipe is summarized in Table 1. The completed device and its close-up views for 32nm bilayer Graphene PMOS are shown in Figure 1(a) and (b). The doping profile of the device can be view in Figure 2. The device was then ready for the simulation of the electrical characteristic performance which was measured through ATLAS module.

B. Semi Analytical Approach for Bilayer Graphene

In this research, the simulation of the device considered all the physical effects of Graphene material. The whole operation was presumed to function at room temperature (T=300K) with a bandgap is set at 0.55eV [12], permittivity of 2.4 [13], carrier mobility with top-gated material, a large value of 100ns for radiative recombination rate of electron and holes [14], and the effective field of Eeff=0.4MV/cm [13] while the electron and hole densities of states were calculated and was attained from [14]:

$$Nc = \frac{8\pi m_e kT}{h^2}\ln\left(1 + e^{-(Ec-Ef)/kT}\right)$$
$$Nv = \frac{8\pi m_h kT}{h^2}\ln\left(1 + e^{-(Ef-Ev)/kT}\right) \quad (1)$$

The effective mass of the electrons and holes of Graphene were set at me≈0.06 mo, mh≈0.03mo and mo is the free electron mass. The value of the mass was obtained from the established research in [14].

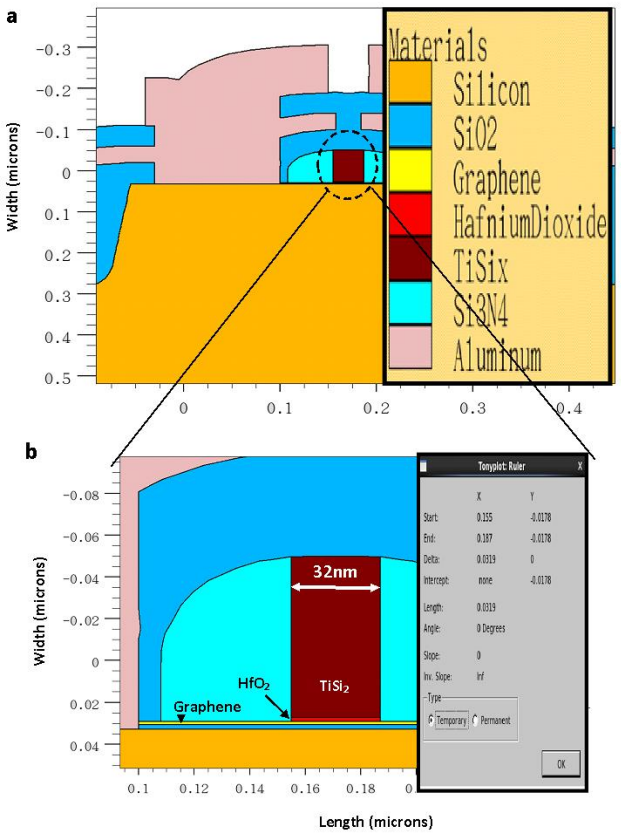

Figure 1: (a) A complete of 32nm PMOS virtual transistor; (b) zoom in gate length of 32nm PMOS technology

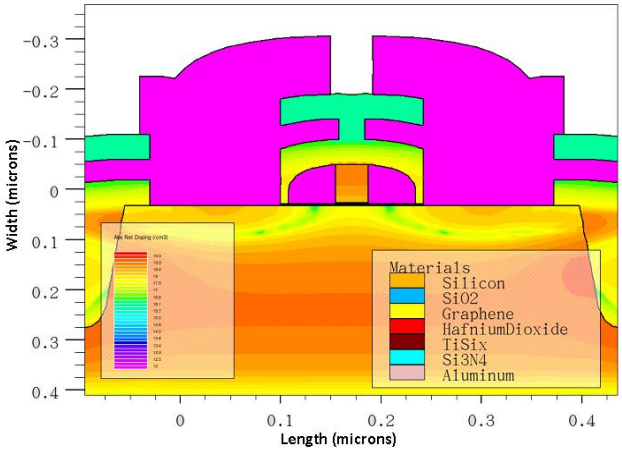

Figure 2: Doping profile of 32nm PMOS transistor

C. Taguchi Method to Parameter Design

L9 Taguchi approaches were introduced to extract maximum significant data with least number of experiments. It is an experimental design optimization which utilizes Orthogonal Arrays (OA) for creating a matrix of experiments without violating some limitation. The goals are to helps inventors to learn and analyze the impact of various manageable factors on the normal of quality characteristics and the distinctions efficiently. In this research, four control factors (CF) and two noise factor (NF) were chosen based on established research papers in [16]. The factors were identified as the most influential parameters for V_{TH} and I_{LEAK}. The values for CF and NF at each level are as depicted in Table 2 and Table 3 correspondingly.

Table 1
Bilayer PMOS Fabrication Recipe

Process Step	p-type MOSFET Parameters
Substrate	• Silicon • <100> orientation
Retrograde well implantation	• 200Å oxide screen by 970°C, 20min of dry oxygen • $4.5x10^{11}$ cm^{-3} Phosphorous • 30min, 900°C diffused in Nitrogen • 36min, dry Oxygen
STI isolation (X)	• 130Å stress buffer by 900°C, 25min of dry oxygen • 1500Å Si_3N_4, applying LPCVD • 1.0um photoresist deposition • 15min annealing at 900°C
Gate oxide	• diffused dry oxygen for 0.1min, 815°C
Vt adjust implant	• $1.75x10^{11}$ cm^{-3} Boron difluoride • 5KeV implant energy, 7° tilt • 20min annealing at 800°C
Bilayer graphene deposition	• 0.00068um Graphene
High-K/Metal gate deposition	• 0.002um HfO_2 • 0.0771um $TiSi_2$ • 17min, 900°C annealing
Halo implantation (A, B)	• $4.876x10^{13}$ cm^{-3} Phosphor • 19.79° tilt
Sidewall spacer deposition	• 0.047um Si_3N_4
S/D implantation (C)	• $1.41x10^{13}$ cm^{-3} Boron • 10KeV implant energy • 7° tilt
PMD deposition (D, Y)	• 0.05um BPSG • 20min, 850°C annealing • $1.1x10^{12}$ cm^{-3} Phosphor • 60KeV implant energy • 7° tilt
Metal 1	• 0.04um Aluminum
IMD deposition	• 0.05um BPSG • 15min, 950°C annealing
Metal 2	• 0.12um Aluminum

III. Results and Analysis

A. Analysis Signal-to Noise (S/N) Ratio for V_{TH} and I_{LEAK}

Nine sets of experiments which consist of 36 simulations were done utilizing the three levels of CF and two levels of NF. The simulation results for V_{TH} and I_{LEAK} are shown in Table 4 and Table 5 respectively.

Table 2
Control Factors and Levels

Symbol	Process Parameter	Unit	Level 1	Level 2	Level 3
A	Halo Implant Dose	$atom/cm^3$	$5x10^{13}$	$5.23x10^{13}$	$5.4x10^{13}$
B	Halo Tilting Angle	°	19.75	19.79	19.83
C	S/D Implant Dose	$atom/cm^3$	$1.4x10^{13}$	$1.41x10^{13}$	$1.42x10^{13}$
D	Compensation Implant Dose	$atom/cm^3$	$1.0x10^{12}$	$1.1x10^{12}$	$1.2x10^{12}$

Table 3
Noise Factors and Levels

Symbol	Noise Factor	Unit	Level 1	Level 2
X	Sacrificial Oxide Layer Temperature	°C	900 (X1)	910 (X2)
Y	BPSG Temperature	°C	850 (Y1)	852 (Y2)

Table 4
V_{TH} Results for Bilayer Graphene PMOS

Exp. No	Threshold Voltage, V_{TH} (V) X1, Y1	X1, Y2	X2, Y1	X2, Y2
1	-0.023926	-0.0242152	-0.0230908	-0.0238221
2	-0.0238026	-0.0245344	-0.023411	-0.0242489
3	-0.0241218	-0.0248551	-0.23411	-0.0244673
4	-0.112418	-0.113556	-0.111947	-0.1131
5	-0.08211	-0.0852978	-0.083088	-0.08485
6	-0.115845	-0.116968	-0.115349	-0.116506
7	-0.15459	-0.155785	-0.154144	-0.155337
8	-0.15533	-0.18825	-0.186178	-0.187694
9	-0.157944	-0.159142	-0.157496	-0.158694

Table 5
I_{LEAK} Results for Bilayer Graphene PMOS

Exp. No	Leakage Current, I_{LEAK} (nA/um) X1, Y1	X1, Y2	X2, Y1	X2, Y2
1	0.123	0.323	0.328	0.325
2	0.324	0.321	0.326	0.323
3	0.322	0.320	0.319	0.321
4	0.112	0.111	0.113	0.112
5	0.111	0.149	0.152	0.150
6	0.108	0.107	0.109	0.108
7	0.0684	0.0677	0.0688	0.068
8	0.0680	0.0484	0.0493	0.0487
9	0.0659	0.0651	0.0662	0.0655

The results were then used to determine the factor that gives the most significant effect on the device performance through Signal-to-Noise (S/N) ratio calculation. The V_{TH} analysis belongs to the nominal-the-best quality characteristic while its I_{LEAK} belongs to the smaller-the-best quality characteristics. This statistical method was used to get the nominal value of V_{TH} as well as the lowest possible I_{LEAK}. The S/N ratio of nominal-the-best, $\boldsymbol{\eta}_{NTB}$ can be expressed as [17]:

$$\eta_{NTB} = 10 \log_{10}\left(\frac{\mu^2}{\sigma^2}\right) \quad (2)$$

and

$$\mu = \frac{Y_i + \cdots + Y_n}{n} \quad (3)$$

$$\sigma^2 = \frac{\sum_{i=1}^{n}(Y_i - \mu)^2}{n-1} \quad (4)$$

where n is the number of experiments, Yi is the experimental value of V_{TH}, μ is mean and σ is variance. The S/N ratio of smaller-the-best for I_{LEAK}, $\boldsymbol{\eta}_{STB}$ can be expressed as [17]:

$$\eta_{STB} = -10 \log_{10}\left[\frac{1}{n}\sum(Y_1^2 + Y_2^2 + \cdots Y_n^2)\right] \quad (5)$$

where n is the number of experiments, Yi is the experimental value of I_{LEAK}. The $\boldsymbol{\eta}$ (S/N ratio) of each simulation for V_{TH} and I_{LEAK} were then measured by applying the formula in Equation (2) and Equation (5). In this calculation, the effects of S/N ratio can be parted out at each level because the experimental design is orthogonal. The values are as depicted in Table 6. It shows that at experiment number 4, 6 and 7 scores a very high S/N ratio which also declares that the CF combinations at this level were the best for characteristics response [7].

The S/N ratio of each level of CF for V_{TH} and I_{LEAK} and the calculation of the overall mean of S/N ratio are summarized in Table 7 and Table 8 respectively. The value of S/N ratio specifies the significance of a CF to lessen the variation. The

higher value of the ratio, the better the characteristic quality of V_{TH} and I_{LEAK} and hence, the greater the impact on the device performance [7, 16].

B. Analysis of Variance (ANOVA) for V_{TH} and I_{LEAK}

The most common statistical analysis to measure the percentage of contribution of a factor that significantly affects the device performance is the analysis of variance (ANOVA) [9, 15]. The analysis also includes the sum of square (SS), the degree of freedom (DF), the mean square, and the percentage of factor effect on the S/N ratio. The results of ANOVA for V_{TH} and I_{LEAK} are as shown in Table 9 and Table 10 respectively. As mention before, the highest value of S/N ratio of a factor indicates that the factor has the most dominant effect on the device performance.

Based on the result of ANOVA for V_{TH}, compensation implant factor scored the highest value on S/N ratio with a 30% contribution and thus was set as the dominant factor. Halo implant factor, on the other hand, was set as an adjustment factor as it scored the lowest in S/N ratio (16%) and highest in mean (92%). Halo implant dose was varied in the next confirmation simulation within the dopant level in level 1 and level 3 values which were within $5x10^{13}atom/cm^3$ and $5.4x10^{13}atom/cm^3$ to get the V_{TH} closer to the ITRS2011 target. The analysis of ANOVA for I_{LEAK} shows that Halo implant factor was the most dominant factor with 38% of contribution followed by S/D implant factor (22%), Halo tilting angle factor (21%) and compensation implant factor (19%). This means a small change in Halo implant dopant will either increase or reduce the leakage current significantly.

Table 6
S/N Ratio for V_{TH} and I_{LEAK}

Exp. No	S/N Ratio (dB)	
	V_{TH}	I_{LEAK}
1	0.730	190.80
2	34.0	189.80
3	36.9	95.93
4	44.0	199.01
5	16.1	196.97
6	44.2	199.34
7	46.5	203.32
8	21.0	205.31
9	46.6	203.65

Table 7
S/N Response for V_{TH}

Symbol	Control Factor	S/N Ratio (dB)			Overall Mean S/N	Max-Min
		L1	L2	L3		
A	Halo Implant Dose	23.85	34.76	38.02	32.21	14.17
B	Halo Tilting Angle	30.39	23.67	42.57		18.90
C	S/D Implant Dose	21.98	41.52	33.13		19.54
D	Compensation Implant Dose	21.15	41.56	33.93		20.41

Table 8
S/N Response for I_{LEAK}

Symbol	Control Factor	S/N Ratio (dB)			Overall Mean S/N	Max-Min
		L1	L2	L3		
A	Halo Implant Dose	158.84	198.44	204.09	187.13	45.25
B	Halo Tilting Angle	197.71	197.36	166.31		31.05
C	S/D Implant Dose	198.48	197.49	165.41		33.07
D	Compensation Implant Dose	197.14	197.48	166.75		30.73

Table 9
Results of ANOVA for V_{TH}

Performance Parameter	Control Factor	DF	SS	Mean Square	F-Value	Factor Effect (%)	
						S/N ratio	Mean
V_{TH}	Halo Implant Dose	2	330	165	8	16	92
	Halo Tilting Angle	2	550	275	13	26	3
	S/D Implant Dose	2	577	289	14	28	5
	Compensation Implant Dose	2	638	319	15	30	1

Table 10
Results of ANOVA for I_{LEAK}

Performance Parameter	Control Factor	DF	SS	Mean Square	F-Value	Factor Effect of Variance (%)
I_{LEAK}	Halo Implant Dose	2	3648	1824	19	38
	Halo Tilting Angle	2	1950	975	10	21
	S/D Implant Dose	2	2124	1062	11	22
	Compensation Implant Dose	2	1868	934	10	19

C. Optimal Results through Confirmation Simulation

Numbering equations consecutively with equation numbers in confirmation simulation was the final step in Taguchi method where the best combination of control factors was simulated again at four different noise factors. The best combination factors were chosen based on the highest-level score on S/N ratio. For V_{TH}, the highest score of S/N ratio for factor A was at level 3 (38.02dB), factor B at level 3 (42.57dB), factor C at level 2 (41.52dB), and factor D at level 2 (41.56dB). Since factor A was set as an adjustment factor in ANOVA, the dopant value was swept. Hence, the best combination factor for optimum V_{TH} is A(sweep), B3, C2, and D2. The best combination factor for the lowest I_{LEAK} was A3, B1, C1, and D2 as the factors score highest at level 3 (204.09dB) for factor A, level 1 (197.71dB) for factor B, level 1 (198.48) for factor C and level 2 (197.48dB) for factor D. The best setting parameter and its value which were determined by Taguchi method are as tabulated in Table 11.

Final simulations at four different noise factors were done using the best value of each parameter and the results are as depicted in Table 12. The finest V_{TH} value achieved is 0.10299V at noise factor of X1 (900°C) and Y1 (850°C) with 0.0097% nearer to ITRS2011 target compared to V_{TH} before optimization with 0.1786% to the target. In this case, the lower the percentage, the better the performance. The V_{TH} η_{NTB} is 67.1dB which is within the range of 67.01dB to 67.17dB (67.09±0.08dB). The lowest I_{LEAK} attained after optimization is 0.05545673nA/um at noise factor of X1

(900°C) and Y2 (852°C) correspondingly. The I_{LEAK} η_{STB} is 236.5dB which is also within the range of 236.43dB and 236.59dB (236.51±0.08dB). Both I_{LEAK} results of either before or after optimization show a lower value than the target. The final result of the V_{TH} and I_{LEAK} were then compared to the ITRS2011 prediction and of before optimization. The results are as depicted in Table 13. From the results, both V_{TH} and I_{LEAK} meets the ITRS2011 target and scores better after the optimization took place.

Table 11
Best Setting Parameter for V_{TH} and I_{LEAK}

Symbol	Control factor	Unit	Best value	
			V_{TH}	I_{LEAK}
A	Halo Implant Dose	atom/cm^3	5.4x10^{13}	5.4x10^{13}
B	Halo Tilting Angle	°	19.83	19.75
C	S/D Implant Dose	atom/cm^3	1.41x10^{13}	1.4x10^{13}
D	Compensation Implant Dose	atom/cm^3	1.1x10^{12}	1.1x10^{12}

Table 12
Results of Confirmation Simulation for V_{TH} and I_{LEAK}

Performance Parameter	Noise Factor (°C)				S/N Ratio (%)
	X1, Y1	X1, Y2	X2, Y1	X2, Y2	
V_{TH} (V)	0.10299	0.103833	0.102237	0.103364	67.1
I_{LEAK} (nA/um)	0.0666354	0.05545673	0.0555348	0.0548829	236.5

Table 13
Simulation Results versus ITRS2011 Prediction

Performance Parameter	ITRS Prediction	Non-Optimized Result	Optimized Result
V_{TH} (V)	-0.103 ± 12.7 %	-0.103184	-0.10299
I_{LEAK} (nA/um)	< 150	0.130034	0.05545673

IV. CONCLUSION

The virtual design of 32nm top-gated bilayer Graphene PMOS and its semi-analytical model is succinctly presented. The design is suitable for the study of the design parameter for performance analysis. Halo implantation, Halo tilting angle, S/D implantation and compensation implantation are the four parameters that were chosen as the control factors for L9 Taguchi analysis. With the exploitation of Taguchi, it assists the researchers and designers to evaluate which parameter is influencing the device's performance the most and simultaneously contributed to the enhancement of the design's reliability. In this research, compensation implant and Halo implant are the dominant factors in V_{TH} and I_{LEAK} respectively. Having said that, a slight change in the dopant value will affect the device performance entirely. The optimized results show that both V_{TH} and I_{LEAK} meets the requirement of high-performance planar device as aimed by ITRS2011.

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