Totem-Pole Bridgeless Boost PFC Rectifier Using Series-Parallel Resonant Network

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***Abstract*—A new series-parallel resonant bridgeless boost (SPBBR) power factor correction (PFC) rectifier is proposed in this paper. It is based on a totem-pole bridgeless boost (TPBLB) configuration which allows bi-directional current to flow during resonance to provide soft-switching for all semiconductor devices. Therefore, no additional active switch is needed. The resonant is produced by a resonant network which is placed before the output capacitor. A detailed analysis of the converter operation and control is presented. Design considerations and parameter values determination are also given. Simulation results is used to verify the theoretical analysis of the SPBBR.**

***Index Terms*—Bridgeless Boost Rectifier (BBR); Series-Parallel Resonant; Totem-Pole; Zero Current Switching (ZCS).**

I. INTRODUCTION

The power factor correction (PFC) boost rectifier is the most popular topology amongst the rectifiers. It is a combination of a diode-bridge rectifier with a dc/dc boost rectifier. The circuit is simple and regulated output voltage and high power factor voltage can be easily achieved [1]–[3]. Figure 1 shows the typical circuit of continuous current mode (CCM) boost PFC converter with average current mode control [4]. Figure 2 shows the simulated waveforms of the circuit shown in Figure 1, where the inductor current follows the shape of the input voltage. The peak of the input current and the width of the pulse width modulation (PWM) signal are changed according to the input voltage.

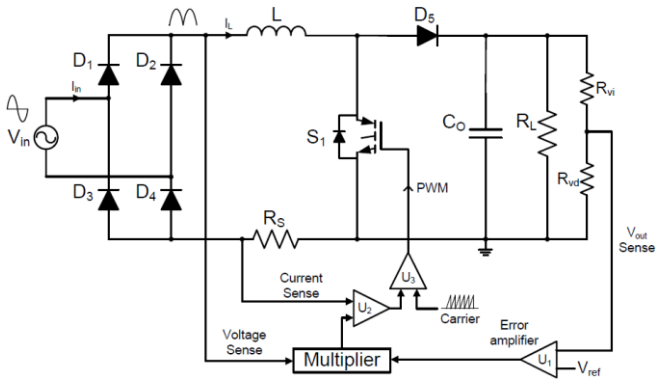


Figure 1: Typical circuit of CCM boost PFC rectifier

However, the conduction losses are significantly high across the diode-bridge especially at a lower input voltage and higher output power [5]. The conduction losses caused by the diode-bridge rectifier is because two diodes need to be permanently active in the current path which causes conduction losses. Therefore, overall converter efficiency is also decreased. The conduction losses caused by the conventional diode-bridge boost rectifier can be reduced further by reducing the number of device(s) in a current path. The number of device reduction topologies have been proposed by a number of researchers in past three decades [6]–[8]. The proposed device reduction converter is known as bridgeless converter where physically, the diode-bridge configuration is no longer exist in the converter.

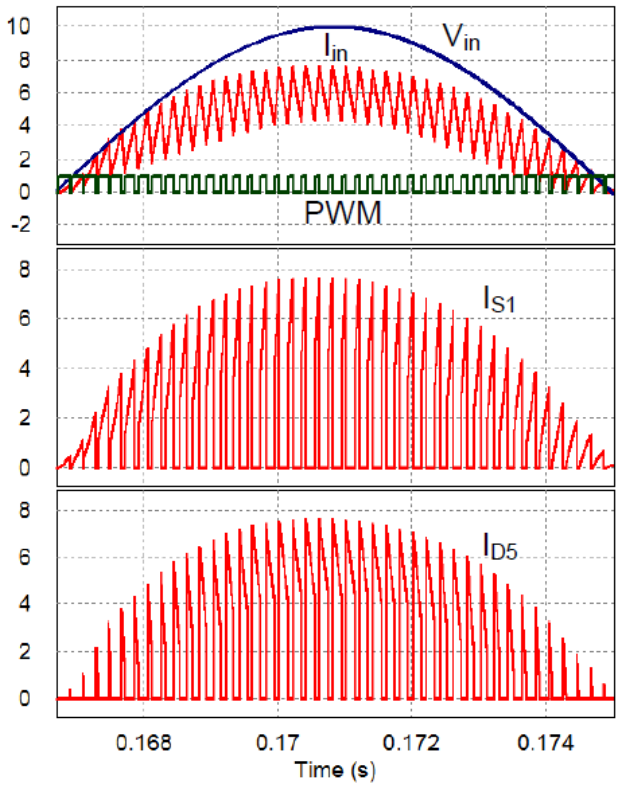


Figure 2: Typical PFC boost rectifier in CCM related waveforms.

The bridgeless topology can also be configured as other dc/dc converter such as buck, cuk and buck-boost [9]–[11]. In bridgeless topologies, the number of devices in a current path is less than the number of devices in diode-bridge converter. There is no significant improvement for bridgeless topologies over the conventional diode-bridge converter in terms of the size of the passive component. However, the elimination of the diode-bridge means that the number of conducting devices in the current path is reduced. Hence, the efficiency will also increase.

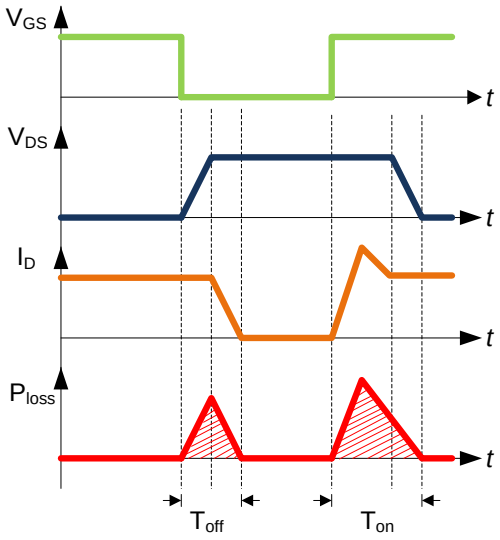


Figure 3: Losses in between switching transition.

II. Bridgeless Boost Rectifier with Soft-Switching

Bridgeless boost rectifiers (BBR) has the ability to achieve high power factor using a basic closed-loop control technique. Even though conduction losses are reduced in BBR topologies, the BBR topologies still suffer from switching losses which occur at every time the switch is on and off. The switching losses occur due to the BBR is switched by using the hard-switching technique. The hard-switching technique offers a simple control and switching circuit which means the overall cost and the complexity of the controller are reduced. However, the drawback of hard-switched BBR more dominant compared to their advantages such as higher device stress, higher switching loss and high rate of change of current and voltage over time as shown in Figure 3.

The switching losses can be reduced by applying the soft-switching technique to the hard-switched BBR. The principal of the soft-switching is where the switch/device commutation occurs when its voltage or current is zero. This paper will discuss, analyse, and examine the effect of BBR when the soft-switching technique is applied.

Soft-switching technique may be divided into two categories, namely zero-current-switching, (ZCS) and zero voltage-switching, (ZVS). To achieved ZVS, the switch voltage must be forced to zero before the switch current starts flowing. A MOSFET body-diode or IGBT co-packed-diode will allow the current to flow in reverse direction through the switch. The current flow through the body-diode or co-packed-diode will clamp the voltage across the switch to a negligible voltage level such that turn-on switching losses are significantly reduced [1]. However, ZVS cannot be achieved during turn-off but the area of the switching transition can be reduced by adding a capacitor across the switch to bring down the voltage rising rate which is also called low-loss turnoff. In order to eliminate the capacitive losses during turn-on, ZVS is preferable due to MOSFETs have a larger drain-source capacitance (C_{ds}) [12].

For ZCS, switch current must be zero before the gate voltage is increased by directing the current away from the switch. Negative voltage potential can also be imposed across the switch to direct the current away from the switch. However, ZCS cannot be achieved during the switch turn-on transition due to an inductor is usually placed in series with a switch. Therefore, the ZCS can only be achieved during turn-off. The current rising rate of the switch could be reduced by the series inductance, hence, minimizing the overlapping between the current rise and voltage fall. This technique is suitable for an IGBT which known to have a tailing current problem [1].

In this paper, a ZCS BBR with high power factor is introduced. In order to achieve soft-switching operations, the proposed ZCS BBR combines a totem-pole bridgeless boost rectifier (TPBBR) topology [8] with passive L-C networks. The L-C resonant networks are placed before the output capacitor.

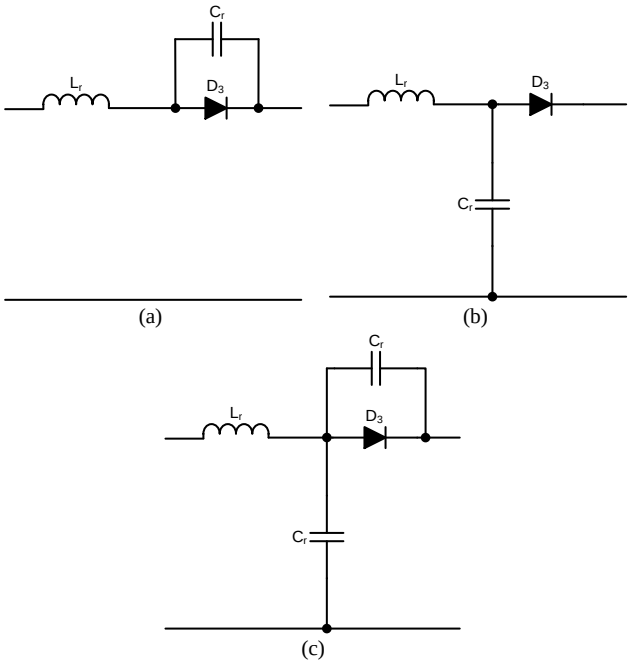


Figure 4: Resonant network configurations. (a) Series resonant network, (b) Parallel resonant network, and (c) Series-parallel resonant network.

The L-C resonant network is classified into three categories namely series resonant, parallel resonant and series-parallel resonant networks. The category is classified according to the connection of the resonant inductor and resonant capacitor as shown in Figure 4. Series resonant TPBBR and parallel resonant TPBBR have been proposed in [8] and [13] respectively. In this paper, TPBBR with series-parallel resonant network configurations (SPBBR) will be analysed.

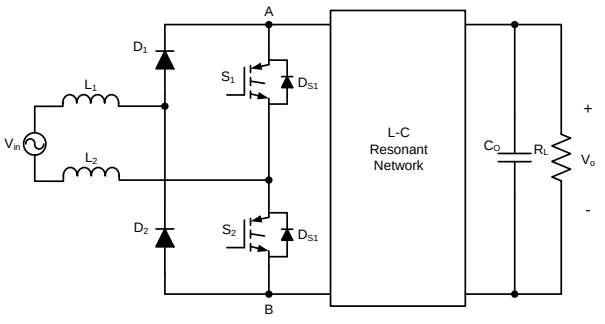


Figure 5: A TPBBR topology with L-C resonant network.

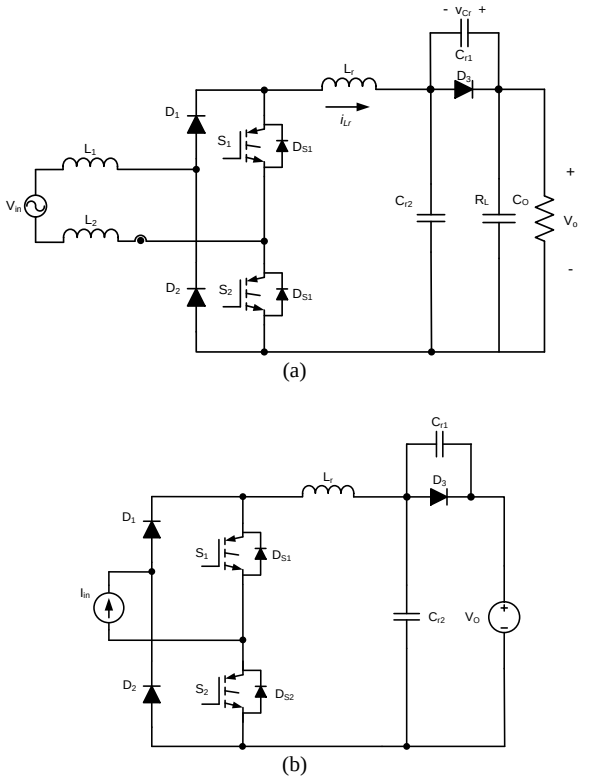


Figure 6: (a) Proposed SPBBR converter topology (b) Equivalent circuit of the proposed SPBBR converter topology during steady-state.

III. PROPOSED CONVERTER OPERATION

The concept of a BBR converter with soft-switching is by allowing the current to flow bi-directionally from high voltage point to low voltage point which occurs during the resonant. High voltage point is marked as A and low voltage point is marked as B as indicated in Figure 5. The bidirectional current flow can be realized by arranging S_1 on top of S_2 which also known as 'totem-pole' arrangement. The current flow from high voltage point to low voltage point through S_1 and S_2 when both switches are turned on and vice versa when both switches are turned off.

The proposed SPBBR converter circuit is shown in Figure 6(a) while the equivalent circuit of the converter during steady-state operation is shown in Figure 6(b). L_r, C_{r1} and C_{r2} network provides ZCS for S_1 and S_2 and causes both switches and diode D_3 to turn-on softly. Only a slow recovery diode type is needed for D_1 and D_2. This is because the diodes are always conducted for half cycle line period. The SPBBR converter has a similar operation principle for each half cycle line period. Therefore, it is adequate to explain the circuit analysis during positive half cycle only. It will reflect the circuit analysis during the negative half cycle. The following assumptions have been made to further simplify the analysis.

i. SPBBR converter is operated in steady-state.
ii. L_1 and L_2 are large. It is assumed as constant dc current source.
iii. C_o is large. It is assumed as a constant dc voltage source.
iv. D_2 is off during the positive half cycle.

Figure 7 illustrates the ideal key waveforms of the SPBBR converter, while Figure 8 shows the equivalent circuits of the SPBBR converter during the positive half cycle.

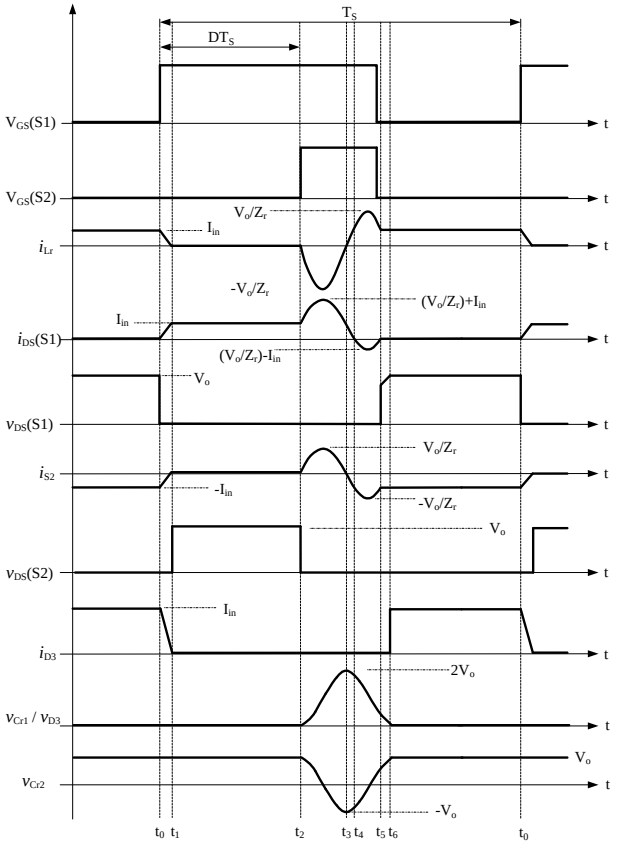


Figure 7: Ideal key waveforms of the proposed SPBBR converter.

A. $t_0 \le t \le t_1$

It is assumed that D_1, D_3 and D_{S2} were conducting while D_2, S_1, and D_{S1} were not conducting. i_{Lr} is increased to the level of the input current, I_{in} while v_{Cr1} and v_{Cr2} are zero. At $t=t_0$, S_1 is turned on softly and body diode of S_2 is turned off at ZCS. L_r is discharged from Iin through D_3–V_O–D_{S2}–D_{S1} to zero at $t=t_1$. L_r causes D_3 to turn off at ZCS. The time interval can be described as:

$$t_{01} = t_1 - t_0 = \frac{I_{in} L_r}{V_O} \tag{1}$$

B. $t_1 \le t \le t_2$

In this interval, I_{in} continues flowing through D_1 and S_1, while the other switches are off. $i_{Lr}(t)$, $v_{Cr1}(t)$ and $v_{Cr2}(t)$ are zero. This interval will determine the shape of the input current waveform as described in Equation (2)

$$t_{12} = t_2 - t_1 = DT_S - t_{01} \tag{2}$$

where T_s is the switching period and D is the duty cycle.

C. $t_2 \le t \le t_3$

The resonance begins when S_2 is turned on. Iin continues flowing through D_1 and S_1, while i_{Lr} increases negatively through S_1–S_2–C_{r1} and reaches its peak. The peak voltage is determined by V_o=Z_r. At $t=t_3$, the peak voltage decreases to zero. v_{Cr1}, charges to its peak at $t=t_3$ while v_{Cr2} discharges to -V_o through L_r–S_1–S_2. V_o causes D_3 reverse-biased and opened. The time interval is determined as

$$t_{23} = t_3 - t_2 = \frac{\pi}{\omega_r} \tag{3}$$

where

$$\omega_r = \frac{1}{\sqrt{L_r(C_{r1}+C_{r2}}} \quad (4)$$

$$Z_r = \sqrt{\frac{L_r}{C_{r1}+C_{r2}}} \quad (5)$$

D. $t_3 \le t \le t_4$

The resonance continues in this interval. The resonant continues to resonate for another half period through L_r–C_{r1}–V_o–D_{S2}–D_{S1} until $t=t_4$. At this instant, $i_{Lr} = I_{in}$, while v_{Cr1} is decreasing and v_{Cr2} is increasing. The current that flows through S_1 decreases sinusoidally until zero. The time interval can be described as

$$t_{34} = t_4 - t_3 = \frac{\sin^{-1}\frac{I_{in}Z_r}{V_O}}{\omega_r} \quad (6)$$

E. $t_4 \le t \le t_5$

During this interval, S_1 is turned off. The resonance continues resonating from the previous interval via L_r–C_{r1}–V_o–D_{S2}–D_{S1} while I_{in} flows through D_1–L_r–C_{r1}–V_o–D_{S2} and back to the source. C_{r2} continues to discharge while resonating from the previous state. To achieve ZCS, the peak value for period t_{45} must satisfy the condition in Equation (7):

$$\frac{V_O}{Z_r} \ge I_{in} \quad (7)$$

If the condition in Equation (7) is exceeded, more than double amount of the input current will flow through S_1 during resonance. Hence, this will double the rating and cost of the component. To achieve ZCS with lower peak current through S_1, the ratio of V_o=Z_r is required to be close as possible to I_{in}. Values of C_{r1}, C_{r2} and L_r can be obtained according to Equation (7) as long as V_o is regulated. When the I_{S1} turns off with ZCS, this interval reached its end. The time interval is:

$$t_{45} = t_5 - t_4 = \frac{\pi - 2\sin^{-1}\frac{I_{in}Z_r}{V_O}}{\omega_r} \quad (8)$$

F. $t_5 \le t \le t_6$

Resonance process is stopped at $t=t_5$ when i_{Lr}=I_{in}. I_{in} flows through D_1–L_r–C_{r1}–V_o–D_{S2} and D_1–L_r–C_{r2}–D_{S2}. All switches are off. Therefore, v_{Cr1} decreases linearly to zero and v_{Cr2} increases linearly to V_o at $t=t_6$. During this time interval

$$t_{56} = t_6 - t_5 = \frac{2V_O(C_{r1}+C_{r2})}{I_{in}}\cos[\pi - \sin^{-1}(\frac{I_{in}Z_r}{V_O})] \quad (9)$$

G. $t_6 \le t \le t_0$

At this interval, v_{Cr1} is zero and v_{Cr2} is fully charged to V_o. D_3 starts to conduct. I_{in} flows through D_1–L_r–D_3–V_o–D_{S2}. The same process repeated after it reaches $t=t_0$. process

$$t_{60} = t_0 - t_6 = T_S - DT_S - [\frac{2\pi - \sin^{-1}(\frac{I_{in}Z_r}{V_O})}{\omega_r}] + \frac{2V_O(C_{r1}+C_{r2})}{I_{in}}\cos[-\sin^{-1}(\frac{I_{in}Z_r}{V_O})]] \quad (10)$$

The functionality of the switches in SPBBR converter is fully utilized by exchanging the role of the switch at every half cycle. The resonant conduction time is determined by

$$T_{res} = t_5 - t_2 = \frac{2\pi - \sin^{-1}(\frac{I_{in}Z_r}{V_O})}{\omega_r} \quad (11)$$

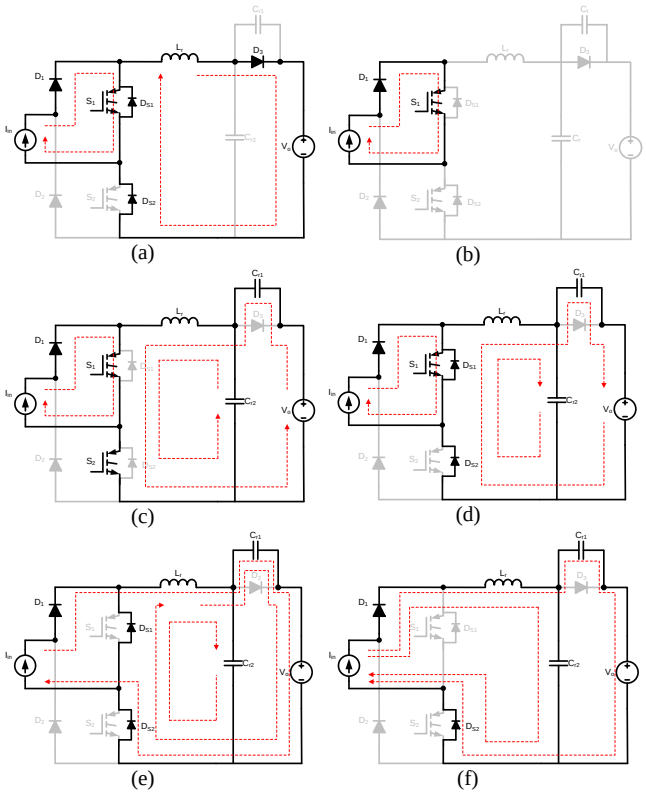
where T_{res} is resonance period between t_{25}. The minimum value of T_{res} is $T_{res}=2$ and the maximum value of T_{res} is when I_{in} is zero. It is suggested that set T_{res} at $0.75T_{res}$ when I_{in} = 0.

IV. SPBBR Parameters Determination

The specifications of SPBBR is shown in Table I. Based on the specifications, the parameters for the SPBBR can be determined.

Table 1
Proposed SPBBR Converter Specifications

Parameters	Values
Output power, P_{out}	400 W
Input Voltage, v_{in}	90 - 240 V_{rms}
Input Current, i_{in}	4.44 A
Output voltage, V_{out}	400 V_{dc}
Input frequency, f_{in}	50 Hz
Switching frequency, f_s	45 kHz



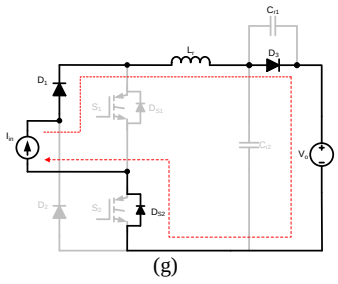


Figure 8: Equivalent circuit of the proposed TPBLB converter during positive half cycle (a) Interval 1 (b) Interval 2 (c) Interval 3 (d) Interval 4 (e) Interval 5 (f) Interval 6 (g) Interval 7.

A. Determination of L_r and C_r

In practice, resonance frequency, fr, is set to be higher than switching frequency by ten folds or higher [14]. Therefore, the characteristics of the boost converter output operated in CCM will not be affected. The condition as in Equation (7) will ensure that the ZCS and soft turn-on could be achieved. The limit of Lr needs to be set according to the (12).

$$L_r \le \frac{I_{in}}{2\pi f_r V_O} = 73.5\times10^{-6} \tag{12}$$

By manipulating Equation (4) and satisfying Equation (7), C_{r1} and C_{r2} can be obtained.

$$\frac{1}{\sqrt{L_r(C_{r1}+C_{r2})}} = \omega_r = 2\pi f_r = 2\pi 10 f_s = 1.44\times10^{6} \tag{13}$$

$$\sqrt{\frac{L_r}{(C_{r1}+C_{r2})}} \le \frac{V_O}{I_{in}} = 106.06 \tag{14}$$

L_r should be less than or equal to 73.5 H. Therefore, Lr=42 H is chosen. The obtained L_r is substituted into Equation (13) to obtain a total resonant capacitance (C_{r1} + C_{r2}) equal to 12 nF. Therefore, C_{r1} = C_{r2} = 6 nF. Two 6.8 nF resonant capacitors are selected to produce a total resonant capacitance of 13.6 nF. T_{res} could be obtained by substituting Z_r into Equation (11). The L_r and C_r rating are as follows:

$$v_{C_r} \ge 2V_O \tag{15}$$

$$i_{L_r} \ge \frac{2V_O}{Z} \tag{16}$$

Table 2
Proposed SPBBR Converter Parameters

Parameters	Values/Model
Boost inductors, L_1 and L_2	1 mH
Resonant inductor, L_r	42 uH
Resonant capacitors, C_{r1} and C_{r2}	6.8 nF
Output capacitors, C_O	680 uF
Output resistor, R_O	400 – 1.6 kΩ

V. SIMULATION RESULTS

PSIM® is used to simulate the workability of the proposed SPBBR converter. Table 2 shows the parameters of the SPBBR. The gate signals for S1 and S2 are shown in Figure 9(a) and 9(b) respectively. The resonant network voltage and current waveforms are shown in Figure 9(c), 9(i) and 9(j) respectively, are similar as analysed in the SPBBR converter operations and confirmed that the analyses are valid. The soft switching for S1 and S2 are shown in Figure 9(d) until Figure 9(g). D3 is turned off at ZCS as shown in Figure 9(h) and 9(i). The input supply voltage, input supply current and it respective Fast Fourier Transform (FFT) are shown in Figure 10. It shows that the ability of SPBBR to achieve high power factor. The power factor and the FFT are improved when the power is increasing.

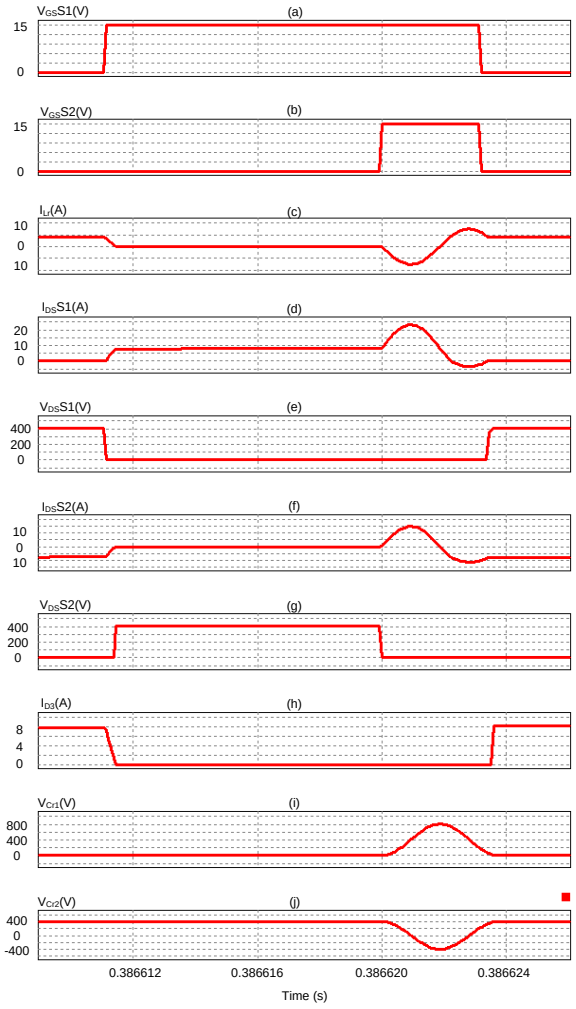
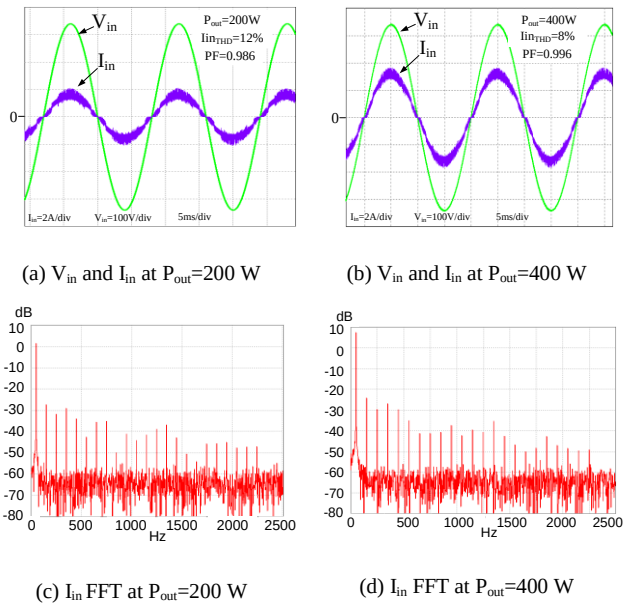


Figure 9. The SPBBR simulation results at 240 Vin_{rms} (a) Gate signal for S1. (b) Gate signal for S2. (c) i_{Lr} . (d) Current through S1. (e) Voltage across S1. (f) Current through S2. (g) Voltage across S2. (h) Current through diode D3. (i) Voltage across resonant capacitor C_{r1}/diode D3 and (j) Voltage across resonant capacitor C_{r2}.

VI. CONCLUSION

A new SPBBR converter topology has been presented. A detailed analysis of the converter operation under series-parallel resonant network configuration has been described. The SPBBR has been analysed and the performance of the converter has been validated by using simulation. The performance of the converter has been evaluated by assessing the power factor and the total harmonic distortion of the input parameters. The SPBBR is able to work within different load condition. With the addition of the resonant networks, the input voltage and current are not affected. The THD of the SPBBR is within the acceptable limit.



(a) V_{in} and I_{in} at P_{out}=200 W (b) V_{in} and I_{in} at P_{out}=400 W

(c) I_{in} FFT at P_{out}=200 W (d) I_{in} FFT at P_{out}=400 W

Figure 10. Simulation results of input supply voltage, input supply current, and corresponding FFT for SPBBR at different loads

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