A Low Power, High-Accuracy, 1-V CMOS Potentiostat for Amperometric Sensors

Mudasir Bashir, SreehariRao Patri, KrishnaPrasad KSR
National Institute of Technology, Warangal, India-506004.
mudasir.mir7@gmail.com

***Abstract*—In this paper, a three-electrode, low power potentiostat for biomedical and chemical sensor applications is implemented. A modified regulated cascode current mirror employing split length technique is used as an interface between the potentiostat circuit and sensor electrode, resulting in better performances in terms of input and output impedances, linearity, bandwidth and gain. The potentiostat is implemented for both single-ended and fully differential configurations using UMC 65 nm CMOS technology, having chip areas of 0.014 mm^2 and 0.086 mm^2, respectively. The circuit results in detection of reduction-oxidation (redox) current of 50 nA to 4.8 µA and 0.1 nA to 7.2 µA, while consuming power of (0.06 to 3) µW and (1.2 to 18) µW for single-ended and differential potentiostat configurations, respectively. Differential potentiostat results in better linearity and dynamic range than single ended.**

***Index Terms*—Amperometric Sensor; Current Mirror; Potentiostat; Electrochemical Cells; Transimpedance Amplifier.**

I. INTRODUCTION

Recent interests and developments in Lab on Chip (LOC) concept and ubiquitous computing has reinforced the demand of implantable and fully integrated sensors for chemical and biological applications inside human body. Amperometric electrochemical sensors (AES) are commonly used in pH level detection, neural recording, DNA identification, glucose determination or protein classification or lactose variation in blood streams [1]. An AES is a three-electrode device, as shown in Figure 1, consisting of a working electrode (WE), a reference electrode (RE) and a counter electrode (CE) or auxiliary electrode (AE). The CE supplies the required current for an electrochemical reaction at WE and RE measures the potential developed across the solution [2]. The performance of AES is not only impelled by microelectrode material and structures, but also by its electrical operating conditions. A potentiostat acts as a control amplifier ensuring that no current flows through RE, while maintaining the potential across RE and WE static. The sensor output is readout as the current flowing through CE and WE. Therefore, the AES requires a decent potentiostat as a part of CMOS smart front end along with the analog-to-digital converter (ADC).

Recently, many current-based potentiostat topologies have been developed to achieve low power dissipation, higher accuracy and smaller die areas [2-6]. The main principle of these current-based potentiostats is to sense the AES current (I_{sensor}) and mirror it to output, where this mirrored current (I_{mirror}) is measured, and then given to trans-impedance amplifier (TIA) for amplification. The primary design issues related to the current copying circuits are: mismatch errors between the transistors; minimum input voltage (V_{MIN}) for devices to work in active region; and, equivalent output impedance (r_{out}). In this paper, a modified regulated cascode current mirror is adopted which outperforms the performance of the present potentiostat replicating circuits. The potentiostat is realized in 65 nm CMOS technology with both single ended (SE) and fully-differential (FD) output TIA configurations.

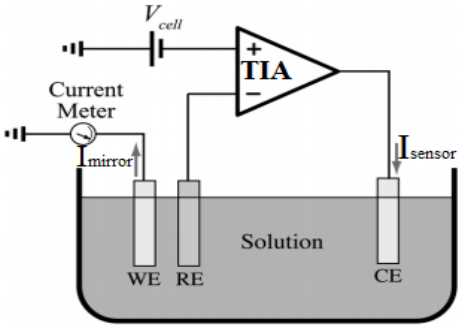

Figure 1: A three-electrode AES with potentiostat.

A concise recapitulation about the literature and present potentiostats topologies used in electrochemical sensors is presented in Section II. In Section III, the operation of proposed SE potentiostat is described followed by FD topology. Section IV summarizes the post-layout simulation results and comparison is done between SE and FD potentiostat configurations. Finally, section V concludes with the summary.

II. REVIEW OF EXISTING TOPOLOGIES OF AES

The amperometric electrochemical sensors employ a two or three electrode arrangement and are extensively used as a complete or an integral part of chemical and biomedical sensing elements. These are treated as a subclass of voltametric electrochemical sensors whose operation depends on the electrolyte concentration and the corresponding sensor current (I_{sensor}) and potential developed [2]. A schematic of three electrode AES and its simplified electrical equivalent model is shown in Figure 2. The solution impedances are neglected due to their small values while as the faradic resistances of CE and WE are represented by R_c and R_w, respectively. The capacitances associated with these resistors are represented by C_C and C_w. The faradic reaction induced between the electrode and solution and the resistance of WE (R_w) is given by:

$$V_{CELL} = V_{WE} - V_{RE} \quad (1)$$

$$R_W = {}^{V_{CELL}}/_{I_F} \quad (2)$$

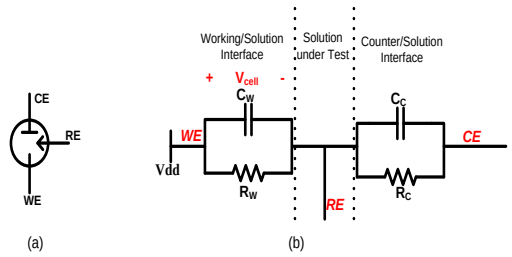

Figure 2: (a) Three electrode AES, (b) Electrical equivalent model [3].

A typical potentiostat for AES is shown in Figure 3. When the reduction-oxidation (redox) voltage across RE and WE become equal to the redox potential of analyte concentration, a current (I_{sensor}) gets generated which is proportional to the concentration of analyte. The output swing of the operational amplifiers (op-amps) limits the output range of the AES. Also, the three op-amps result in more power consumption and area.

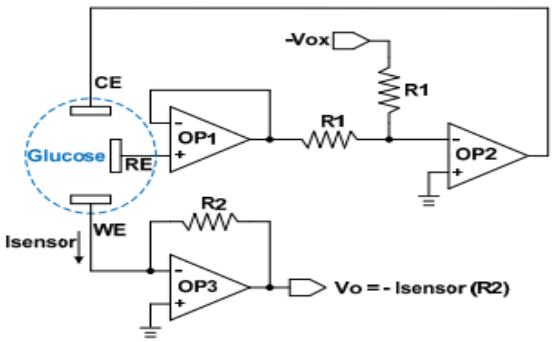

Figure 3: SE Potentiostat.

With an endeavor to develop miniature implantable AES, the usage of op-amps was reduced. In this regard, most of the potentiostats reported recently use op-amps only as control amplifiers [1], [3-6], [8-10]. The I_{sensor} is amplified and processed using current mirrors. In [3],]a current based technique in which a simple current mirror (SCM) is used for copying the sensor current and then the copied current is measure instead of the sensor current directly, as shown in Figure 4. The transistors MO_1 and MO_2 are prone to mismatches resulting in poor accuracy. Also, the MO_1 adding one more stage to the control amplifier results in stability issues. One more configuration is reported in [3], where a drive transistor (M_1) acts as a voltage follower thus mitigating the stability issues but results in decrease of V_{gs} of M_1 which in turn reduces the output swing at CE. In [4] and [5], shown in Figure 5(a), Wilson current mirror is used as a current buffer for improving the accuracy but results in low output impedance and higher V_{MIN}. In [6], shown in Figure 5(b), a wide swing cascode current mirror is used to achieve higher matching, accuracy and low power consumption but results in increase of V_{MIN}.

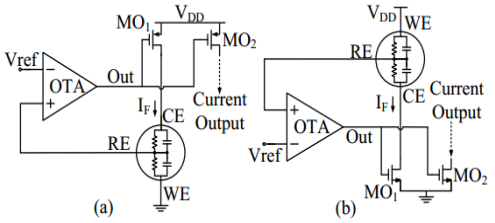

Figure 4: A potentiostat with (a) positive E_i, and (b) negative E_i [3].

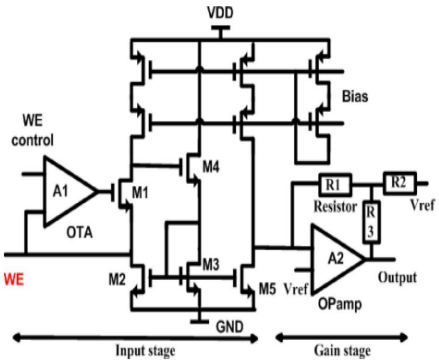

Figure 5(a): Low input impedance based potentiostat [4].

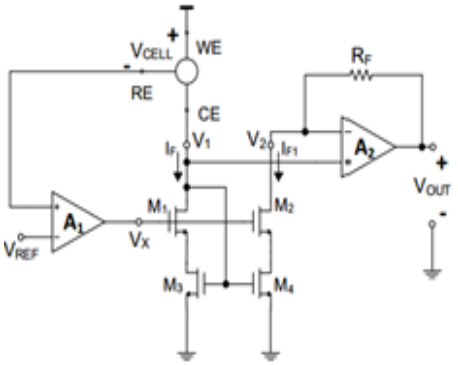

Figure 5(b): High accuracy based potentiostat[6].

III. Proposed Potentiostat Topology

The purpose of implementing this topology is to improve the performance of the present potentiostat topologies by replacing the present current copying circuits with a circuit having superior performances.

A. Single Ended Potentiostat

The block diagram of single-ended (SE) potentiostat topology is shown in Figure 6. The control amplifier (OP1) sources or drives the current into or from the CE, maintaining the voltage between RE and WE same as voltage bias (V_{bias}). The current mirror copies the sensor current from the CE and later gives it to amplifying part which converts it into voltage signal. The highlights of this topology are: RE is directly connected to input of OP1, thus blocking the current flow into RE; The connection between the output of OP1 and gate terminal of mirror transistor prevents the loading of OP1 due to large capacitor of CE; Finally, the noise level at the output of TIA gets reduced because of direct connection between WE and V_{DD}.

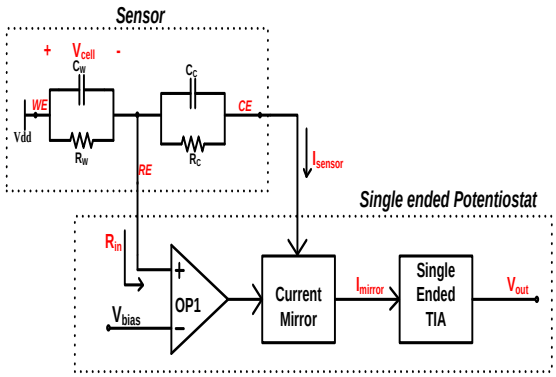

Figure 6: Block Diagram of SE potentiostat.

1. Amperometric Electrochemical Sensor

In AES applications, the potentiostat circuit uses three electrodes electrochemical cell for sensing the signal, as explained in Section II. The equivalent circuit of AES is shown in Figure 2(b). The impedance of the electrochemical cell is given as:

$$Z_{CE-RE} = R_c \parallel {}^{1}/_{sC_c} \tag{3}$$

$$Z_{RE-WE} = R_w \parallel {}^{1}/_{sC_w} \tag{4}$$

The transfer function of the SE potentiostat with electrochemical cell can be expressed as:

$$\frac{V_{RE-WE}}{V_{bias}} = \frac{1}{1+\frac{1}{A_v}\left(1+\frac{R_cC_c(R_w+sC_w)}{R_wC_w(R_c+sC_c)}\right)} \tag{5}$$

where Z_{CE-RE} and Z_{RE-WE} are impedances between CE-RE and RE-WE respectively. Typically, $R_w \gg R_c$, and $C_w \gg C_c$. In this work, R_w can vary from 100KΩ to 10MΩ, R_c= 1KΩ, C_w= 1µF and C_c=1nF.

2. Amperometric Electrochemical Sensor

In the MOS current mirrors like simple, cascode and Wilson, the value of V_{MIN} become larger when the output resistance is increased. One circuit that reduced V_{MIN} while increasing r_{out} is the regulated cascode (RGC) current mirror. The regulated cascode consists of M_2, M_3 and M_4. M_1 and M_2 forms a simple current mirror (SCM); however, because of M_4, the value of V_{DS2} will not be much different than V_{DS1}, resulting in good accuracy. M_5, M_6 and M_7 provide a bias current for M_4, which tracks the output current (I_{mirror}). M_6 and M_7 also mitigate the mismatch effects. For I_{D4} to track the I_{mirror}, the value of V_{GS2} is kept large enough at higher I_{mirror}, so that M_2 is always in saturation. The schematic of the RGC along with improved circuit is shown in Figure 7. In order to further increase the output impedance, the split-length technique is used. The M_3 acts as a self cascode transistor with large effective channel length. M_{3a} is in saturation whereas M_{3b} can be in saturation or triode region. In this case, M_{3b} acts as a resistor working in triode region. For proper operation, the aspect ratio (W/L) of M_{3a} is greater than that of M_{3b}. The small signal equivalent circuit of RGC and modified RGC and the circuits for the calculation of output impedance of RGC and modified RGC are shown in Figure 8 and Figure 9, respectively.

$$\left({}^{W}/_{L}\right)_{3a} = m\left({}^{W}/_{L}\right)_{3b};\ m > 1 \tag{6}$$

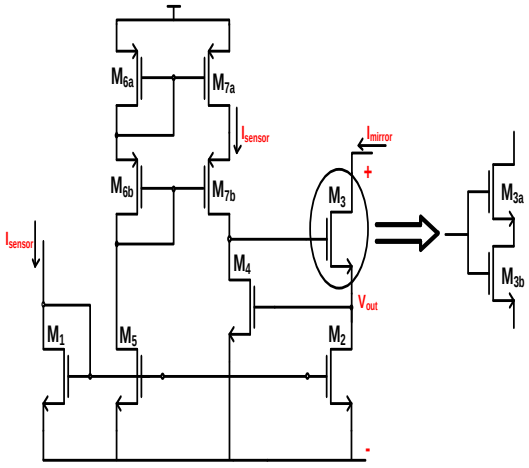

Figure 7: Simple and Modified RGC current mirror.

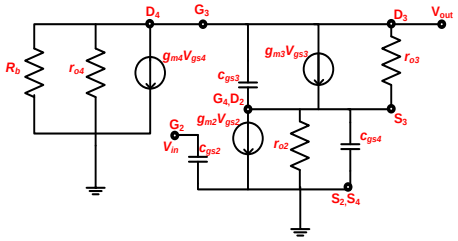

Figure 8(a): Small signal equivalent of simple RGC.

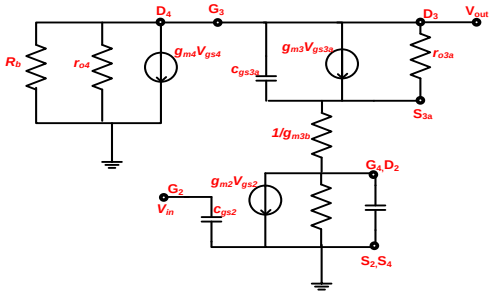

Figure 8(b): Small signal equivalent of Modified RGC.

3. Amperometric Electrochemical Sensor

The output impedance of RGC can be calculated from Figure 9(a), using Kirchhoff's current and voltage laws (KCL and KVL) at ports (a), (b) and (c). Therefore, we get

$$\frac{V_{out}-V_{s3}}{r_{o3}} + g_{m3}(V_{d4}-V_{s3}) - I_{mirror} = 0 \tag{7}$$

$$V_{s3}\left\{\frac{(1+sC_{gs4}r_{o2})}{r_{o2}} + \frac{1}{r_{o3}} + sC_{gs3}\right\} - g_{m3}(V_{d4}-V_{s3}) - \frac{V_{out}}{r_{o3}} - sC_{gs3}V_{d4} = 0 \tag{8}$$

$$V_{d4}\left\{\frac{R_b+r_{o4}}{R_br_{o4}} + sC_{gs3}\right\} - sC_{gs3}V_{s3} + g_{m4}V_{s3} = 0 \tag{9}$$

$$I_{mirror} \cong V_{s3}\left({}^{1}/_{r_{o2}} + sC_{gs4}\right) \tag{10}$$

where V_{s3} is the source terminal voltage of M_3.

From the above equations, the output impedance of RGC is given as:

$$Z_{out} = \begin{Bmatrix} r_{o2}\left(R_b + r_{o4} + sC_{gs3}R_b r_{o4}\right) + g_{m3}r_{o3}r_{o2} \\ \left(R_b + r_{o4}\right) + r_{o3}\begin{pmatrix} R_b + r_{o4} + \\ sC_{gs3}R_b r_{o4} \end{pmatrix} \\ \dfrac{\left(1 + sC_{gs4}r_{o2}\right) + g_{m3}g_{m4}r_{o2}r_{o3}r_{o4}R_b}{\left(1 + sC_{gs4}r_{o2}\right)\left(R_b + r_{o4} + sC_{gs3}R_b r_{o4}\right)} \end{Bmatrix} \quad (11)$$

when $s = 0$, the output resistance R_{out} is:

$$R_{out} = (1 + g_{m3}r_{o3})r_{o2} + r_{o3} + g_{m3}g_{m4}(r_{o4} \parallel R_b) \quad (12)$$

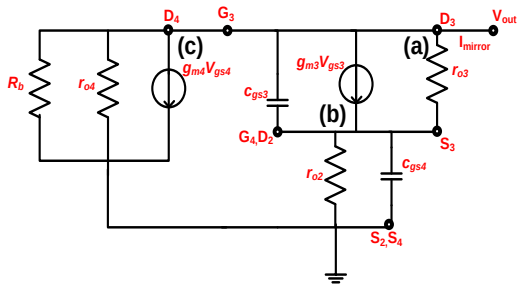

Figure 9(a): Equivalent circuit of RGC for output impedance calculation.

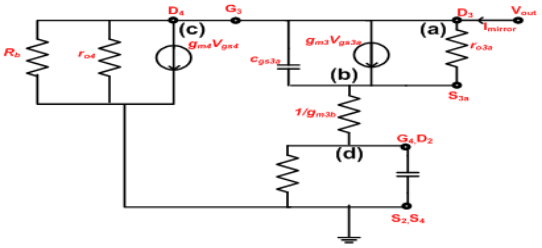

Figure 9(b): Equivalent circuit of modified RGC for output impedance calculation.

The output impedance of modified RGC can be calculated from Figure 9(b). Using KCL and KVL at nodes (a), and (c), we get:

$$\frac{(V_{out} - V_{s3a})}{r_{o3a}} + g_{m3a}(V_{d4} - V_{s3a}) - I_{mirror} = 0 \quad (13)$$

$$V_{d4}\left\{\frac{R_b + r_{o4}}{R_b r_{o4}} + sC_{gs3a}\right\} - sC_{gs3a}V_{s3a} + g_{m4}V_{g4} = 0 \quad (14)$$

At nodes (b) and (d), the node voltages are given by:

$$V_{s3a} = I_{mirror}\left\{\frac{1 + r_{o2}(g_{m3b} + sC_{gs4})}{g_{m3b}(1 + sC_{gs4}r_{o2})}\right\} \quad (15)$$

$$V_{g4} = I_{mirror}\left\{\frac{r_{o2}}{(1 + sC_{gs4}r_{o2})}\right\} \quad (16)$$

Using Equations (13) to (16), the output impedance is given by:

$$Z_{out} = \begin{Bmatrix} \left(1 + r_{o2}\left(g_{m3b} + sC_{gs4}\right)\right)\begin{Bmatrix} \left(R_b + r_{o4}\right) \\ \left(1 + g_{m3a}r_{o3a}\right) \\ + sC_{gs3a}R_b r_{o4} \end{Bmatrix} \\ + g_{m3b}r_{o3a}\left(1 + sC_{gs4}r_{o2}\right) \\ \left(R_b + r_{o4} + sC_{gs3a}R_b r_{o4}\right) \\ \dfrac{g_{m3a}g_{m3b}g_{m4}r_{o2}r_{o3a}r_{o4}R_b}{g_{m3b}\left(1 + sC_{gs4}r_{o2}\right)\begin{pmatrix} R_b + r_{o4} \\ + sC_{gs3a}R_b r_{o4} \end{pmatrix}} \end{Bmatrix} \quad (17)$$

$$R_{out} = \begin{Bmatrix} g_{m3b}\{(1 + g_{m3a}r_{o3a})r_{o2} + r_{o3a}\} + \\ (1 + g_{m3a}r_{o3a}) \\ \dfrac{+ g_{m3a}g_{m3b}g_{m4}r_{o2}r_{o3a}(r_{o4} \parallel R_b)}{g_{m3b}} \end{Bmatrix} \quad (18)$$

when $s = 0$

$$R_{out} = \begin{Bmatrix} g_{m3b}\{(1 + g_{m3a}r_{o3a})r_{o2} + r_{o3a}\} + \\ (1 + g_{m3a}r_{o3a}) \\ \dfrac{+ g_{m3a}g_{m3b}g_{m4}r_{o2}r_{o3a}(r_{o4} \parallel R_b)}{g_{m3b}} \end{Bmatrix} \quad (19)$$

Equation (19) can be represented as:

$$R_{out} = R_{out,simple} + \left(\frac{g_{m3a}}{g_{m3b}}\right)r_{o2} + \frac{1}{g_{m3b}} \quad (20)$$

where,

$$R_{out,simple} = (1 + g_{m3a}r_{o3a})r_{o2} + r_{o3a} + g_{m3a}g_{m3b}g_{m4}r_{o2}r_{o3a}(r_{o4} \parallel R_b) \quad (21)$$

Comparing Equation (12) and Equation (20), it is concluded that the output impedance of the modified RGC is more than that of simple RGC. A comparison of performances of different MOS current mirrors is given in Table 1.

Table 1
Performance Comparison of Different Types of Current Mirrors [7]

MOS current mirror	Accuracy ($I_{in} = I_{out}$)	R_{out}	V_{MIN}
Simple*	Poor	$r_o = 1/\lambda I_{out}$	$V_{DS(sat)}$
Cascode*	Good	$g_m r_o^2$	$2V_{DS(sat)}$
Wilson*	Good	$\frac{g_m r_o^2}{2}$	$V_{GS} + V_{DS(sat)}$
Regulated cascode*	Good	$g_m^2 r_o^2$	$V_{DS(sat)}$
Modified regulated cascode	Good	$g_m^2 r_o^4$	$V_{DS(sat)}$

B. *Transimpedance Amplifier*

For the conversion of current to voltage, a resistive type transimpedance amplifier (TIA) with negative feedback, shown in Figure 10, is employed. The TIA should be highly linear and the output voltage of TIA should not saturate

within the desired range of input current (I_{sensor}) [7]. A T-network resistor is used as negative feedback which minimizes the effects of varying transconductance (g_m) of transistor and also conceals the variation of open loop gain with the input level, resulting in good linearity. The resistive T-network increases the gain while maintaining the same bandwidth. The gain of TIA is given by:

$$Gain = -\left[R_1 + \left(1 + \frac{R_1}{R_2}\right) R_3\right] \tag{22}$$

where R_2 is much smaller than R_1 and R_3.

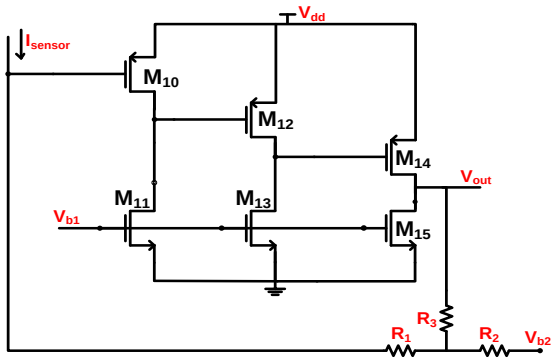

Figure 10: A resistive-type SE TIA.

C. Complete Single Ended Potentiostat Configuration

The complete circuit configuration of SE potentiostat for AES is shown in Figure 11. The cell voltage (V_{cell}) between WE and RE is supervised by a control amplifier (OP1) stage. The output of OP1 forms a negative feedback loop at RE through gate terminal of current mirror, making a virtual short at RE, thus controlling the voltage at RE terminal. For improving the stability of AES, the CA is implemented using a simple folded cascode amplifier, because of its tunable dominant pole. From Eq 1, the V_{bias} and V_{DD} should be strictly matched. Therefore, the V_{bias} is obtained from V_{DD} by using voltage divider concept (M_a and M_b). The transfer function $\left(\frac{V_{RE}}{V_{bias}}\right)$ is given by:

$$\frac{V_{RE}}{V_{bias}} = \frac{1}{1 + A_{OP1}\left(\frac{g_{mA}}{1 + g_{dsA}R_{WE} + g_{mA}\left(\frac{1 + g_{mA}R_{WE}}{g_{ds1}}\right)\left(R_{WE} \parallel {}^{1}/_{g_{m1}}\right)}\right)} \tag{23}$$

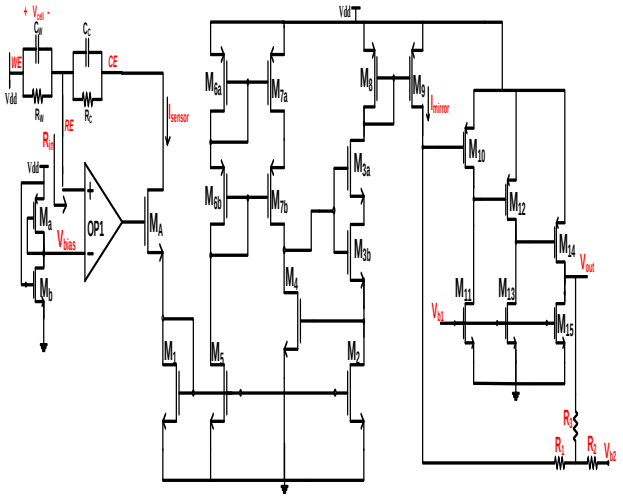

Figure 11: Complete circuit configuration of SE potentiostat.

The noise has a less impact on the cell potential (V_{cell}) due to the presence of very large impedance between solution under test and WE. However, at the output of circuit, the noise affects the detectable signal range. For the sake of simplicity, the flicker noise has not been taken into consideration. The noise power spectral density at RE is given by:

$$\overline{V_{nRE}^2 V_{n1}^2}\left(\frac{A_o g_{mA} R_W}{(1 + {}^{s}/_{p_1})(1 + sR_W C_W) - A_o g_{mA} R_W}\right) + \overline{I_{nW}^2}\left(\frac{R_W(1 + {}^{s}/_{p_1})}{(1 + {}^{s}/_{p_1})(1 + sR_W C_W) - A_o g_{mA} R_W}\right) \tag{24}$$

$$A_{OP1} = \frac{A_o}{(1 + {}^{s}/_{p_1})} \tag{25}$$

The circuit diagram of FD potentiostat is shown in Figure 12. The operation of this topology is similar to SE potentiostat configuration except the output voltage, which is differential in this case. The FD potentiostat is majorly used in fully- differential data converters [7]. A differential current is generated from the RGC current mirror for the differential input of TIA. For proper conversion of sensor current to voltage at output (V_{o+} and V_{o-}), a resistive T-network is used as negative feedback. A three-stage amplifier (OP2) is employed, as shown in Figure 13, for wider dynamic output voltage range. The gain of this amplifier is given by:

$$Gain = 2(R_{eq}) \tag{26}$$

where $$R_{eq} = R_1 + R_2 + \frac{R_1 R_2}{R_3} \tag{27}$$

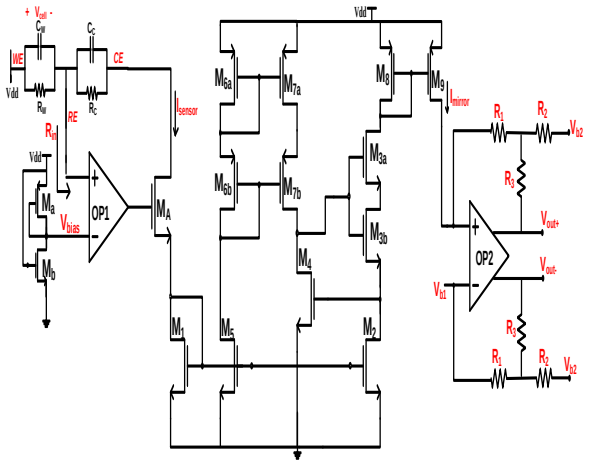

Figure 12: Circuit diagram of FD potentiostat.

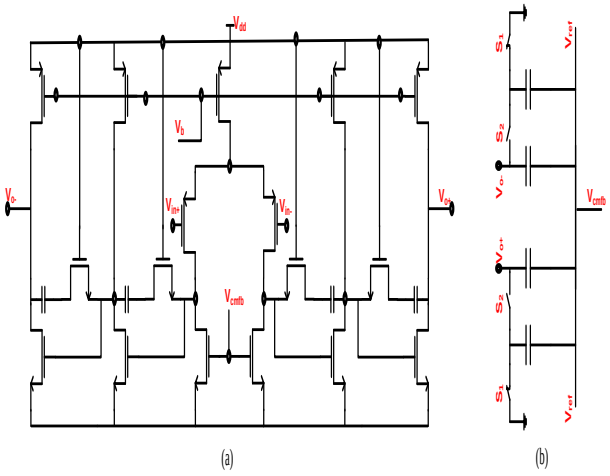

Figure 13 (a): Amplifier in FD TIA, and (b): CMFB circuit.

IV. Results and Discussions

The potentiostat circuit is designed using 65 nm CMOS standard process. The layout of both the SE and FD potentiostats is shown in Figure 14. The total area for SE and FD configuration are 0.014 mm^2 and 0.086 mm^2, respectively (excluding the ESD pads).

The DC response of RGC and modified RGC is shown in Figure 15. It is concluded that the RGC and modified RGC have similar characteristics. The output voltage swings from 1 V to 0.65 V, approximately for both the configurations. Therefore, the operating conditions for both the circuits are same. Figure 16, shows the output impedance of RGC and modified RGC. The output impedance of modified RGC is much greater than the simple RGC.

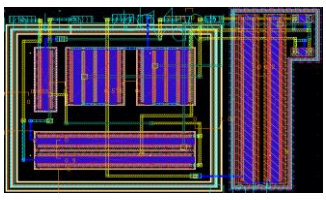

Figure 14 (a): Layout of SE potentiostat.

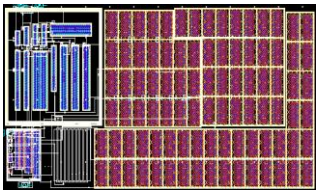

Figure 14 (b): Layout of FD potentiostat.

The loop gain of SE TIA is 113.36 dB and that of FD TIA is 78.5 dB with a phase margin of 73 degrees. The noise performance of both the TIA configurations is shown in Figure 17. At DC level, the SE TIA has an input inferred noise of 126 pV^2/Hz and that of FD TIA is 357 pV^2/Hz.

The typical values of model resistors and capacitors for an electrochemical cell are given in Section II**.** All these values are kept constant except R_{WE}. In order to generate multiple input sensor currents through RE, the R_{WE} is varied from 270KΩ to 10MΩ. The potentiostats (including TIA) works at 1-V power supply having a power consumption of (0.06-3) µW and (1.2-18) µW for SE and FD circuits, respectively. The post layout simulation reveals that the dynamic detectable range for SE potentiostat is 50 nA to 4.8 µA, and that of FD potentiostat is 0.1 nA to 7.2 µA. Also, the dynamic range (DR) of AES is given by:

$$DR\ (dB) = 20log\left({}^{I_{max}}/_{I_{min}}\right) \tag{28}$$

Therefore, the dynamic range of FD circuit is more than that of SE circuit.

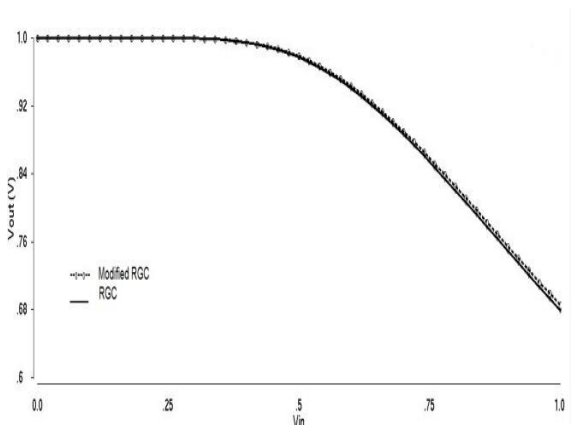

Figure 15: DC response of RGC and modified RGC amplifier.

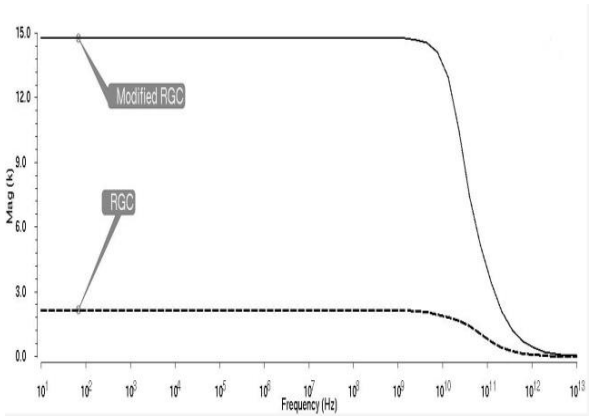

Figure 16: Variation of output impedance of RGC and modified RGC with frequency.

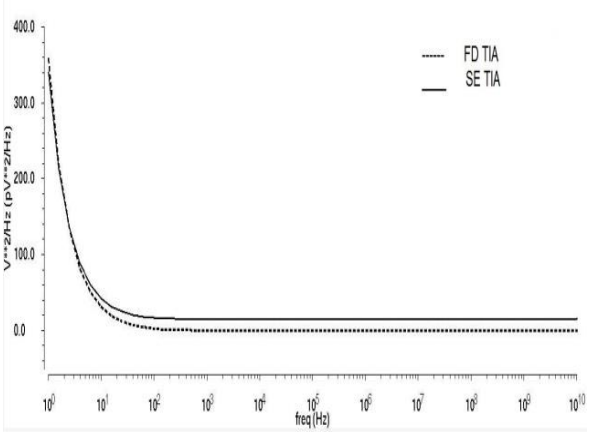

Figure 17: Input referred noise performance of SE and FD TIAs configurations

Figure 18, depicts the accuracy of (V_{RE}/V_{REF}) which fluctuates from 0.99995 to 0.9997, when the R_{WE} is varied from 270 KΩ to 10 MΩ. It is concluded, that the feedback loop across RE electrode and control amplifier (OP1) works well to keep V_{REF} equal to V_{RE}. The percentage current error is found for the potentiostat with sensor current range of 10 pA to 10 µA. As can be seen from Figure 19, the potentiostat results in a maximum error of 0.35m for sensor current of 10 µA. Table 2 gives a comparison of the performance of proposed topology with the recent works. The proposed potentiostat circuit for AESs has a wider sensor current range, besides having low power consumption and area with acceptable linearity.

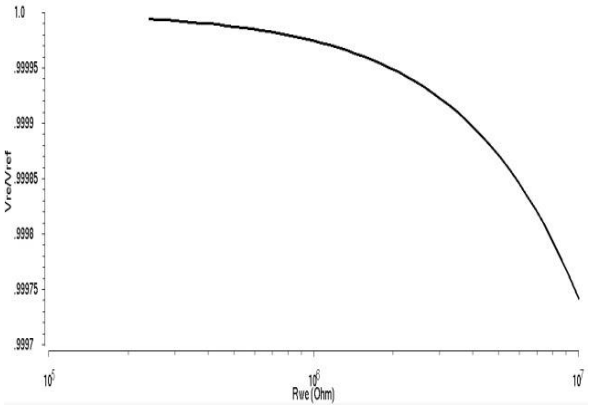

Figure 18: Accuracy of V_{RE}/V_{REF}

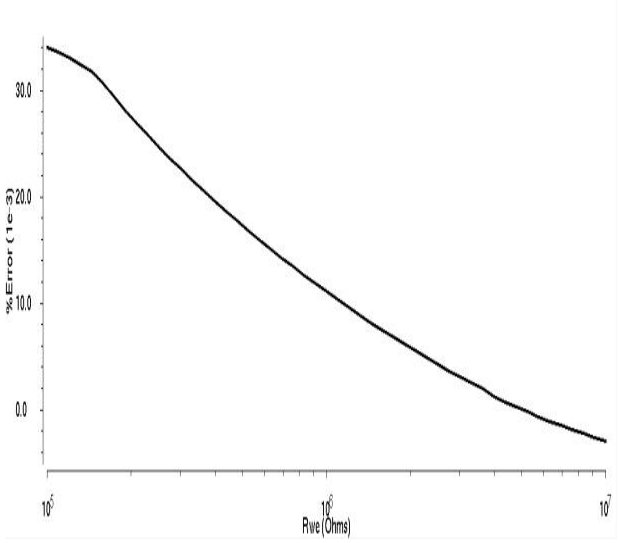

Figure 19: Percentage error in sensor current

V. CONCLUSION

In this paper, a 1-V potentiostat is developed and implemented in 65nm CMOS process. The proposed potentiostat introduces a modified regulated cascode current mirror for replication of sensor current to a readout circuit. The modified RGC resulted in higher output impedance, smaller V_{MIN} and good linearity. The potentiostat has a detectable current sensor range of 50 nA-4.8 µA for SE potentiostat and 0.1 nA-7.2 µA for FD potentiostat, respectively. The circuit has an area of 0.014mm^2 and 0.086mm^2 and power consumption of (0.06- 3) µW and (1.2-18) µW for SE and FD configurations, respectively. The potentiostat is suitable for implantable or portable biomedical and chemical sensor applications. Also, the small signal analysis is done for the modified regulated.

ACKNOWLEDGEMENTS

This work has been performed using the resources of Mixed Signal Laboratory developed at NIT Warangal, Telangana under Special Manpower Development Program for VLSI design and related software (SMDP-II) project funded by Department of Information Technology, Ministry of Communication and Information Technology, Government of India.

Table 2
Comparison with Related Works

	[1]	[3]	[9]	[10]	This Work*	
Year	2015	2009	2009	2015	2016	
Process (µm)	0.35	0.18	0.18	0.5	0.065	0.065
Supply Voltage (V)	1	1.8	1.8	1.8	1	1
Detector Sensor Range	70nA-2.6µA	1nA-1µA	1nA-6µA	10nA-2µA	50nA-4.8µA	0.1nA-7.2µA
Power Consumption (µW)	22	50	12.3	3.5-10	0.06-3	1.2-18
Readout Circuit	SE	SE	FD	SE	SE	FD
Output Signal	Frequency	Frequency	Voltage	Frequency	Voltage	Voltage
Core Area	0.13mm^2	0.02mm^2	0.04mm^2	0.06mm^2	0.014mm^2	0.086mm^2

REFERENCES

[1] L. Zuo, S. K. Islam, I. Mahbub and F. Quaiyum, "A Low-Power 1-V Potentiostat for Glucose Sensors," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 62, no. 2, pp. 204-208, Feb. 2015.

[2] Allen J. bard, Larry R. Faulkner, Electrochemical Methods: Fundamentals and Applications, 2nd Edition, New York: Wiley, 2001.

[3] M. M. Ahmadi and G. A. Jullien, "Current-Mirror-Based Potentiostats for Three-Electrode Amperometric Electrochemical Sensors," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 7, pp. 1339-1348, July 2009.

[4] S. Hwang and S. Sonkusale, "CMOS VLSI Potentiostat for Portable Environmental Sensing Applications," in *IEEE Sensors Journal*, vol. 10, no. 4, pp. 820-821, April 2010.

[5] J. Kim and W. B. Dunbar, "Nanopore-application CMOS potentiostat design with input parasitic compensation," in *Electronics Letters*, vol. 50, no. 8, pp. 578-579, April 10 2014.

[6] R. Trakoolwattana and A. Thanachayanont, "1-V low-power high-accuracy CMOS potentiostat circuit for amperometric sensor," *Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON), 2014 11th International Conference on*, Nakhon Ratchasima, 2014, pp. 1-4.

[7] Randall L. Geiger, Phillip E. Allen, Noel R. Strader, VLSI: Design techniques for Analog and Digital Circuits, 2nd Edition, New Delhi: Tata McGraw-Hill Edition, 2010.

[8] S. M. Martin, F. H. Gebara, T. D. Strong and R. B. Brown, "A Fully Differential Potentiostat," in *IEEE Sensors Journal*, vol. 9, no. 2, pp. 135-142, Feb. 2009.

[9] M. H. Nazari and R. Genov, "A fully differential CMOS potentiostat," *2009 IEEE International Symposium on Circuits and Systems*, Taipei, 2009, pp. 2177-2180.

[10] Melika Roknsharifi, Syed Kamrul Islam, Kai Zhu, Ifana Mahbub," A low power, highly stabilized three electrode potentiostat for biomedical implantable systems", *Analog Integrated Circuit Signal Process.* , vol. 83, pp. 217-229, April 2015.