Development Design of Fault-Tolerant Soft-Core Based on Error Correction Code in FPGA

Mohd Hafiz Sulaiman, Sani Irwan Md Salim, Masrullizam Mat Ibrahim
Faculty of Electronic and Computer Engineering,
Universiti Teknikal Malaysia Melaka (UTeM), Melaka, Malaysia.
sani@utem.edu.my

Abstract—**This paper presented the development of Fault-tolerant soft-core that was implemented based on Error Correction Code (ECC). A simulation of behavioral module was carried out using Xilinx ISE Design Suite Software. The design focuses on Fault-Tolerant Hamming Code, Single-Error-Correction Double-Error-Detection (SEC-DED) Code and Triple Modular Redundancy (TMR) code that is synthesizable in the Field of Programmable Gate Array (FPGA) Verilog. The faults have been injected into the Fault-Tolerant module. The experiment results were compared as the error detection and the error recovered simulated as simulation results.**

Index Terms—**Fault-Tolerant; ECC; Hamming; SEC-DED; TMR; FPGA.**

I. INTRODUCTION

This paper presents three types of Fault-Tolerant (FT) designs. Due to its design, there are many elements that need to be addressed. The important element is the reliability system such as fault tolerance [1]. Fault-Tolerant is a system that corrects the existence of failure in the hardware or software error [2,3]. There are many failure and error produce from the hardware and software. It is almost to obtain the correct data from the hardware and software that have been used [4]. Fault injection is a famous technique in assessing the reliability of the system [5]. This paper proposed the use of fault injection method simulated in the Fault-tolerant system. Developing the fault tolerance is one of the most concerned issues in industries. In a computing system, it is a system with the capability to continue the correct execution of its programs and input/output (I/O) functions in the presence of a certain set of operational faults [6,7]. FT also is associated with redundancy [8]. There are three forms of redundancy mentioned in [9] that are the space redundancy of additional hardware, information redundancy for additional information and time redundancy for multiple sequential execution or verified code. In Fault-tolerant system, Error Correction Code (ECC) is particularly desirable for its development.

This paper focused on the implementation of Fault-tolerant module such as parity codes and error correction code [10]. ECC is used in the system of Fault-tolerant to detect and correct the presence of data error [11]. ECC is an algorithmic system used to detect and correct the data that are incorporated with extra bits parity [12]. ECC can be divided into two, which are the block code and the convolution code. Examples of a block code are such as Hamming, single-error-correction double-error-detection (SEC-DED) and triple modular redundancy (TMR). These three types of fault-tolerant module are implemented in FPGA.

The rest of the paper is organized as follows. Section II describes the Fault-tolerant configuration, Section III shows the results and analysis. Finally, Section IV provides the conclusion of the paper.

II. FAULT-TOLERANT CONFIGURATION

This section presents the review of the configuration of Fault-Tolerant. Figure 1 illustrates the flowchart in designing Fault-Tolerant Module.
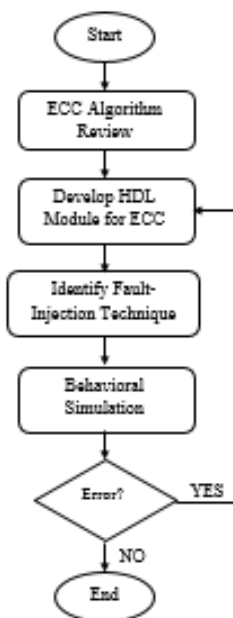

Figure 1: Flowchart Fault-Tolerant Design

A. ECC Algorithm Review

The algorithm of the types Error Correction Code are revised to gain understanding before designing. The concept of the code is important to make sure the system operation is corrected.

B. HDL Module for ECC

The Fault-Tolerant are designed using the Xilinx ISE design software [13]. These modules are designed and simulated using the Xilinx ISE Design Suite v13.2 software. There are three types Fault-Tolerant design mentioned in this paper, namely the Hamming, SEC-DED and TMR. The schematic register-transfer level (RTL) of Fault-Tolerant module design for Hamming, SEC-DED and TMR is illustrated in Figure 2, Figure 3 and Figure 4.

C. *Fault-Tolerant Injection Technique*

In the system, the error may occur everywhere. Fault-injection technique. is one method to test the fault-tolerant system. In this fault-tolerant, there are three types of injection error, which are the Stuck-at-0, Stuck at-1 and double bit-flip.
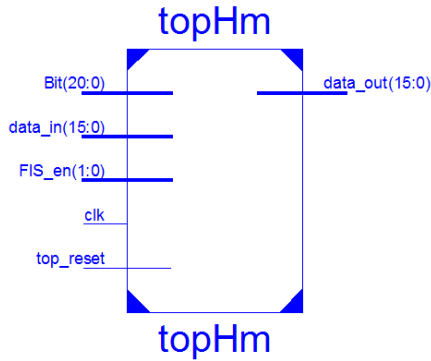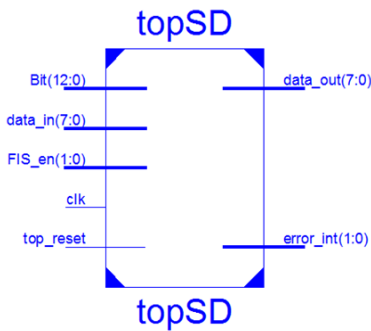

Figure 2: Hamming code Fault-Tolerant Design

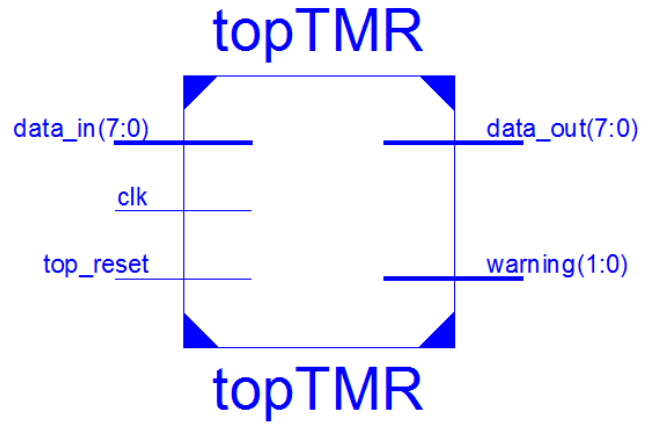Figure 3: SEC-DED code Fault-Tolerant Design

Figure 4: TMR code Fault-Tolerant Design

III. RESULTS AND ANALYSIS

In the system, the critical process is the testing that functions as verification either the system is a success or a failure. Figure 5, 6 and 7 illustrate a waveform results of the simulation using the Xilinx ISE software. The fault-tolerant of Hamming code and SEC-DED contains three blocks which are the encoder, FIS and decoder. The encoder functions as encoding the input data in hexadecimal to binary. The error was injected in the FIS block. After the error was corrected, the binary data were decoded back into the hexadecimal data. This process was carried out in decoder block. For Fault-tolerant TMR, it has a voter to vote two correct block outs of three.

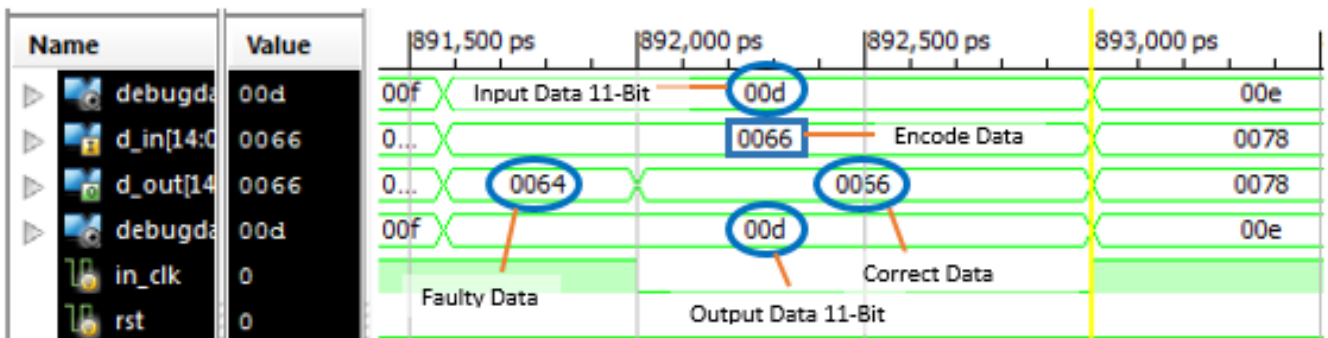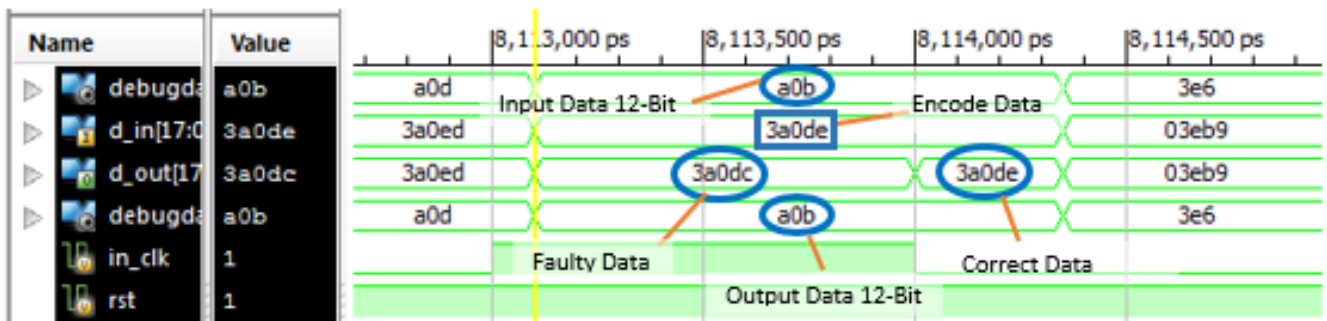

Figure 5: Waveform simulation results for Hamming
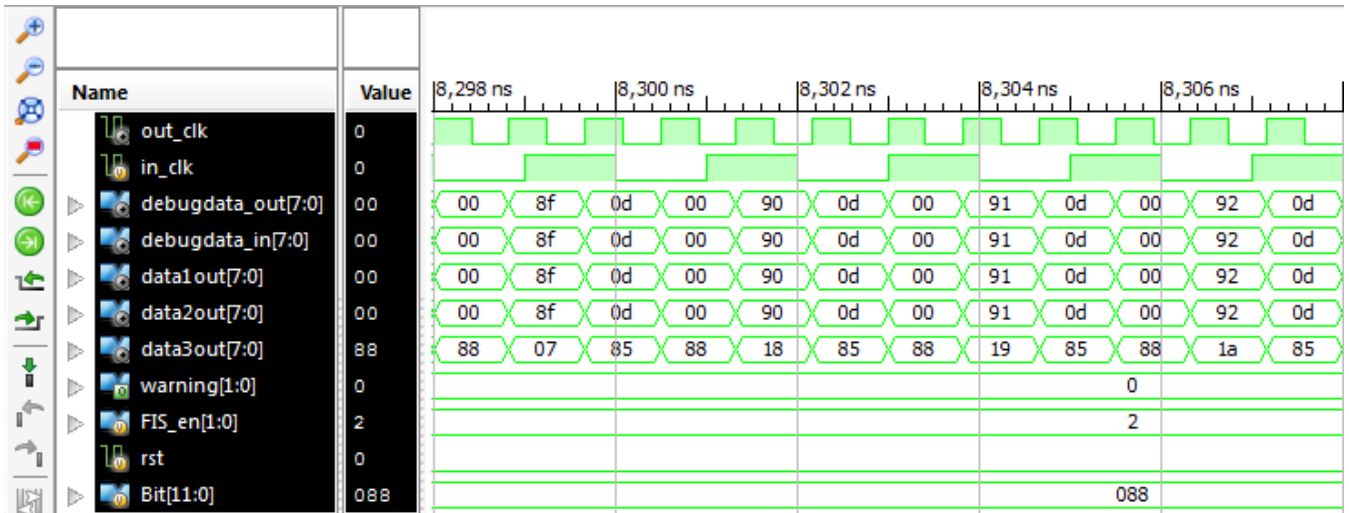

Figure 6: Waveform simulation results for Hamming

Figure 7:Waveform simulation results for TMR

Table 1 illustrates the results of Fault-Tolerant module Hamming Code, SEC-DED Code and TMR Code. All of the results achieved 100% for error detection in the simulation results, except the Hamming Code. This Hamming code only detected single error. However, the percentage for the Fault-Tolerant module Hamming Code and SEC-DED Code were in 67% for error recovered. This Hamming Code and SEC-DED code only corrected single error.

Table 1
Error Recovered simulation results

Types of ECC	Error Detection	Error Recovered
Hamming	67%	67%
SEC-DED	100%	67%
TMR	100%	100%

IV. CONCLUSION

In this research, the Fault-tolerant module was implemented in FPGA based on error correction code. The three types of Fault-Tolerant module were designed and compared. The result illustrates the fault-tolerant TMR code has the highest percentage of error recovered, that is 100%. The fault-tolerant Hamming and SEC-DED has the same percentage of 67%. However, in detection error, the fault-tolerant SEC-DED code and TMR code have the highest percentages, 100%, while the Fault-tolerant Hamming code has 67% only. This is because Hamming code could only detect single error.

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