Heart rate monitoring using ARM Soft Core Processor based System-on-Chip

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***Abstract*—Data acquisition systems are used for data or signal monitoring in many applications. In the biomedical field, signals such as from an ECG, EEG or PPG are monitored using data acquisition systems. A review of several ARM processor-based data acquisition systems for biomedical applications is presented here. A new ARM processor-based system-on-chip architecture is presented for heart rate monitoring applications, which is implemented in Altera Cyclone II FPGA. A PPG-based sensor is used to carry out heart rate monitoring. An experiment is carried out to verify the functionality of the system by monitoring the heart rate of a student. Based on the results, the monitored heart rate is within the average range for heart rate. According to the compilation report, the total logic elements used were 4740, and the total power estimated for the system in Cyclone II FPGA is 199.59mW.**

***Index Terms*— ARM; Cortex-M0; DE2-70 board; Quartus II; PPG.**

I. INTRODUCTION

Today, data acquisition systems are extensively used across numerous industries. Data acquisition systems are able to sample signals from a sensor or a signal source and store these signals in the form of data. These systems are mainly used for monitoring applications in which feedback can be generated by the system based on the acquired signal, via operations such as signal processing.

In the biomedical field, data acquisition systems are used to sample biological signals such as from an electrocardiogram (ECG), electroencephalogram (EEG) or photoplethysmogram (PPG). The system can typically store the biological signals in memory, transfer them to a personal computer (PC), and carry out processing on the data within the system [1-3]. This allows the signals to be analysed in real-time, and thus any occurrence of abnormal states can be resolved. A heart rate monitoring system is one such example, and allows a patient to receive immediate attention from a doctor when the detected signal is abnormal.

For the development of a data acquisition system, a microcontroller such as an ARM processor offers a solution for carrying out data acquisition [4]. In addition to this function, the microcontroller is also able to perform signal processing or data processing and to provide certain types of feedback to the system based on the conditions of operation. Due to its speed and flexibility, the field programmable gate array (FPGA) platform is widely used for data acquisition. The signal processing ability and performance of FPGA can be enhanced by an implementation of an ARM system-on-chip (SoC) using an FPGA platform [5].

In this work, an ARM Cortex-M0 DesignStart processor-based system is implemented with the Altera FPGA as a heart rate monitoring system. Section II discusses various existing heart rate monitoring systems, while Section III presents the methodology used here, which implements a heart rate monitoring system using the ARM Cortex-M0 DesignStart processor on an FPGA platform. In Section IV, the results of testing this heart rate monitoring system are presented, and these experimental results are analysed and discussed.

II. LITERATURE REVIEW

The authors of paper [6] present a real-time pulse-wave data acquisition system, implemented using an ARM processor. In this work, the Raspberry Pi, a single board computer, is used as a platform for data acquisition. The Raspberry Pi consists of an ARM 11 processor, which is used to perform data acquisition and processing. The platform also contains a high-definition multimedia interface (HDMI) peripheral which can display the processed signal on a monitor. An optical-based pulse sensor is used to measure the volumetric blood flow with heartbeat through a fingertip. A 10-bit analogue-to-digital converter (ADC) based on an ATmega328 microcontroller is used for signal data conversion. The microcontroller is interfaced with a single board computer, and has a maximum sampling rate of 76.9Ksps. Figure 1 illustrates this data acquisition system in a block diagram format. In this implementation, the acquisition data is imported to Labview software.

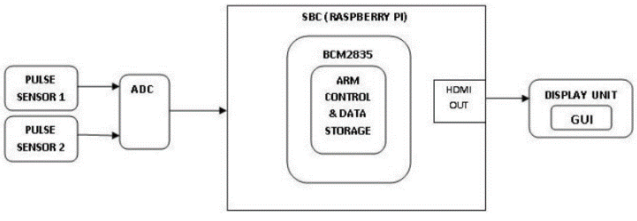

Figure 1: Block diagram of the data acquisition system used in [6]

In paper [7], the authors present the design of a heart rate variability (HRV) processor for a portable 3-lead ECG, in which the HRV processor is integrated into an ARM-based SoC. The main body of the proposed system involves three parts: an ADC controller, an HRV processor, and a lossless compression engine. The architecture of this proposed system is illustrated in Figure 2. An ADC controller is used to

retrieve ECG data from a three-channel ECG through the 10-bit ADC, and then to transfer the data to an HRV processor. The HRV processor performs real-time analysis of time–frequency HRV using a windowed Lomb periodogram. In order to transmit data to a PC or other terminal, a lossless compression engine is used to compress the ECG data. A Bluetooth module based on a universal asynchronous receiver/transmitter (UART) is used in this system for wireless transmission.

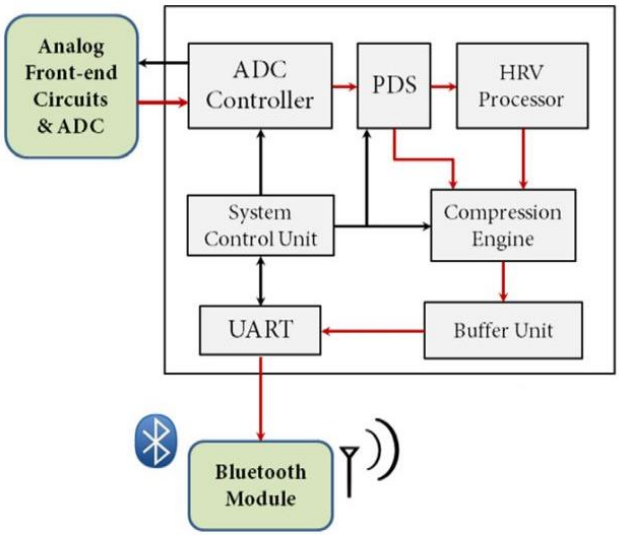

Figure 2: Block diagram of the ECG SoC [7]

The authors of paper [8] propose a non-amplifying ECG signal acquisition system based on a sigma-delta ADC. The system is implemented using a high performance mixed-signal processor, the ARM ADuC7060. This mixed-signal processor is integrated with two 24-bit sigma-delta ADCs and a 12-bit digital-to-analogue converter (DAC) in an ARM chip. The ECG signal is directly captured by the ADC without amplification, which can improve the sound to noise ratio (SNR) of the ECG signal. A DAC is used to provide a reference voltage in order to reduce common-mode interference. The system is communicated with a personal computer using a MAX3232 voltage level switch chip, with DC-to-DC isolator. The results show that this non-amplifying ECG signal acquisition system has high SNR and low nonlinear distortion.

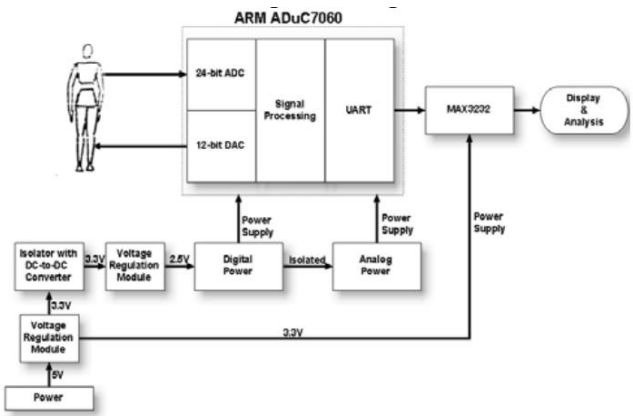

Figure 3: Block diagram of a non-amplifying ECG signal acquisition system [8]

A low power noise tolerant ECG processor for wearable healthcare system is introduced in paper [9]. The system architecture is illustrated in Figure 4, and consists of a 32-bit ARM Cortex-M0 microcontroller, an ECG sensing block, memory and other peripheral interfaces. The ECG sensing block is comprised of an AFE, 12-bit Successive-approximation-register (SAR) ADC, and a robust IHR monitor. A short-term autocorrelation (STAC) algorithm is implemented in IHR monitor to improve noise tolerance and reduce current consumption. The proposed system also used Near Field Communication (NFC) for individual optimization, program loading and logging data transfer from system to other NFC device.

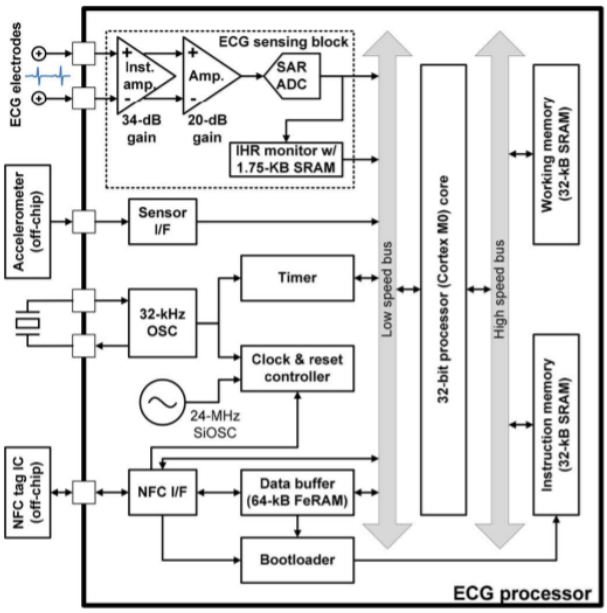

Figure 4: Block diagram of Cortex-M0 based ECG processor [9]

In paper [10], the authors propose a tracking and health indication system for soldiers, which uses an ARM7 processor. The proposed system provides monitoring of the vital signs of the soldiers, and also performs tracking of soldier locations. Vital signs such as respiration rate, body temperature and heart rate are provided to the army base unit with the location of the soldier, via wireless transmission with short message service (SMS) using a global system for mobile communication (GSM) modem. A global positioning system (GPS) module is used to identify the location of the soldier. Figure 5 gives a block diagram of this soldier tracking and health indication system.

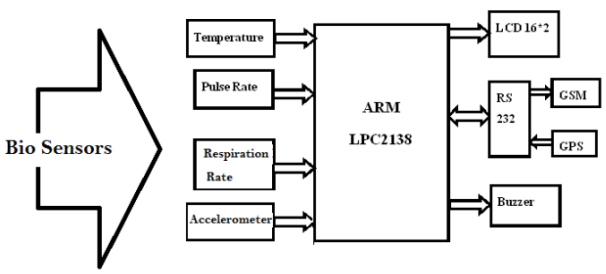

Figure 5: Soldier tracking and health indication system [10]

Table 1 summarizes the similarities and differences of ARM processor-based systems for data acquisition. Based on Table 1, data acquisition can be implemented using a processor such as a general ARM and mixed-signal processor, or through an application-specific integrated circuit (ASIC) approach. A data acquisition system can be developed on a microcontroller, a single board computer or integrated into SoC, with the choice of platform depending on the development costs of the system; a microcontroller platform requires a lower cost for implementation, while the cost of developing the SoC is higher. A comparison can be made between the ARM7, ARM9, ARM11, and Cortex-M0 processors. In terms of performance, the ARM11 processor is a more powerful processor [11]; however, the Cortex-M0 is more efficient in terms of power due to its architecture [11]. The ADuC7060, a mixed signal processor, can also be implemented in a data acquisition system, and the signal can be processed directly by the processor. The operating speed of this system is fully dependent on the processor model. The systems discussed above are applied in data acquisition applications such as ECG and health indicator monitoring.

Table 1
Comparison of existing ARM processor-based data acquisition systems

	[6]	[7]	[8]	[9]	[10]
Design approach	Processor	ASIC	Mixed signal processor	ASIC	Processor
Platform	Single board computer	System-on-chip	Micro-controller	System-on-chip	Micro-controller
processor	ARM11	ARM 9	ADuC7060	Cortex-M0	ARM 7
Speed	700MHz	32MHz	-	24MHz	-
App.	Blood flow	ECG	ECG	ECG	Soldier tracking and health indication

III. METHODOLOGY

In this section, the proposed methodology for implementing a heart rate monitoring system with an ARM soft-core processor SoC on FPGA will be explained. The SoC architecture used in this approach is illustrated in Figure 6. It consists of an ARM Cortex-M0 DesignStart Processor, an advanced high-performance bus (AHB) Lite, a timer module, a 16KB On-Chip memory, a UART and a general purpose input/output (GPIO). In this work, the GPIO is connected to 16 light emitting diodes (LEDs) and an 8-bit successive approximation ADC. The ADC is connected to a pulse sensor in order to receive analogue input.

The methodology of implementation of the SoC within FPGA is illustrated in Figure 7. The methodology is divided into two parts: the software implementation and the hardware implementation. Once the system specification was selected, an ARM Cortex-M0 DesignStart soft core processor, AHB Lite and several peripherals were integrated together using Quartus II software. This integration used the intellectual property core provided by the ARM website [12]. Several modifications to the Verilog code of the integrated system were made in order to meet the required specifications.

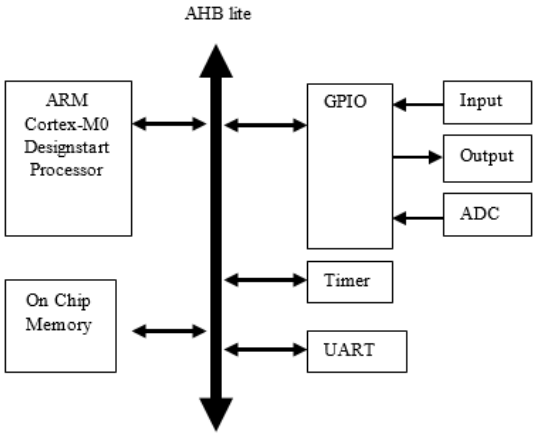

Figure 6: Block diagram of the ARM Cortex-M0 DesignStart processor-based SoC

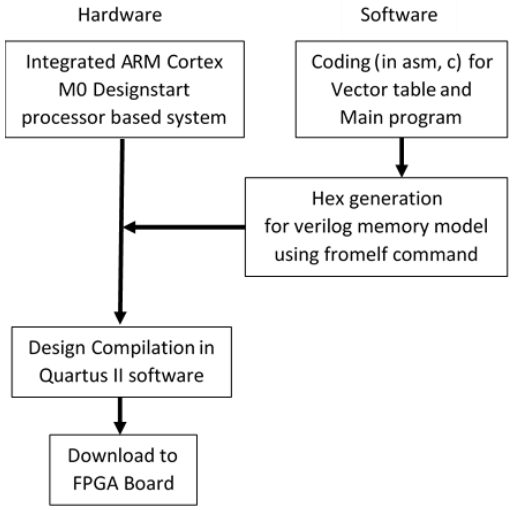

Figure 7: Methodology of implementing the ARM processor-based SoC within FPGA

For the software implementation, Kiel µVision software, a toolchain for the ARM processor, is used to compile the exception vector table and application program (main program). The exception vector table holds all exception vector addresses, including the stack pointer and interrupt request [13]. The application program contains the algorithm for heart rate monitoring. It also holds the instructions for activities within the system. Once compilation was complete, a hex code for the Verilog memory model was generated via the "formelf" command. The integration system, along with the hex code, was synthesized and compiled using Quartus II software. A design configuration file was produced which could be downloaded into the FPGA chip. In this work, the Altera Cyclone II EP2C70F896C6 FPGA chip was used on an Altera DE2 board as a development platform for evaluating the functionality and performance of the SoC. The maximum operating speed for the FPGA in this development board was 50 MHz, which also acts as a limit to the operational speed of the processor.

In this work, the ADC0804 from National Semiconductor, an 8-bit successive approximation ADC, was used to convert the analogue signal to digital data. The configuration of the

ADC circuit, in a self-clocking and free-running configuration, is illustrated in Figure 8 [14]. The ADC converts the analogue signal into 8-bit digital data, with a conversion time of approximate 100µs. An optical-based non-invasive heart rate monitoring pulse sensor was used, which was suitable for PPG applications [15]. This optical-based pulse sensor uses the emitted light from the LED to illuminate a target, such as human skin, and receives the reflected light from the target via a light sensor. The pulse sensor uses a 5V supply and its output signal ranges between 0V and 5V. This fitted perfectly with the analogue input of the selected ADC.

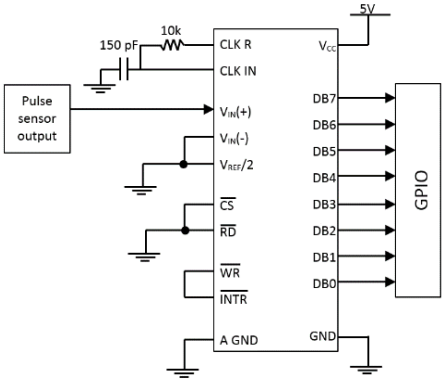

Figure 8: Free-running configuration of the ADC0804

A beat-finding algorithm was used in the SoC within the application program. A flow chart illustrating this beat-finding algorithm is presented in Figure 9. The algorithm starts by reading the input signal from the pulse sensor via ADC. The number of peaks can be detected from this input signal. A threshold is then set in order to identify whether the peaks of the signal are generated by a heartbeat pulse. Once a pulse is detected, time between two peaks, or the inter-beat interval, is stored. Using ten inter-beat intervals, a formula is applied to calculate the beats per minute (BPM). The heart rate is then sent to a PC or other device via UART, and is also stored in on-chip memory for further use.

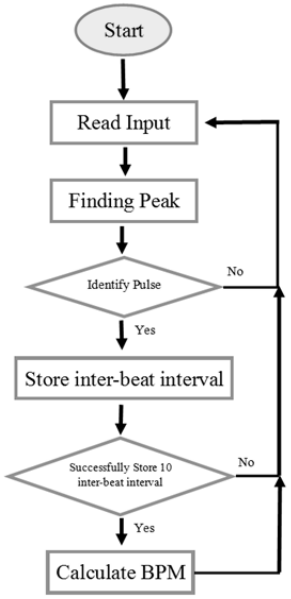

Figure 9: Flow chart of the beat-finding algorithm for heart rate monitoring

IV. Result and Discussion

In this section, the implementation of the SoC and the experimental results from the heart rate monitoring system are presented and discussed. The ARM Cortex-M0 DesignStart processor-based SoC was compiled successfully using Quartus II and Kiel µVision software. During compilation, the Altera Cyclone II EP2C70F896C6 FPGA was selected as a synthesis and compilation target. The design configuration file was successfully downloaded into the selected FPGA development platform.

An experiment was carried out to evaluate the functionality of the heart rate monitoring system. With the design configuration file loaded into the FPGA development platform, the SoC was then embedded into the platform. The ADC and pulse sensor were connected to the platform, and a heart rate monitoring system was developed. Figure 10 shows the FPGA development platform with pulse sensor and ADC connected. The system output was observed via the 16 LEDs and the UART communication to a PC. The 16 LEDs indicate the analogue signal in a form of hexadecimal value, while the UART communication to the PC displays the heart rate of the target. Figure 11 presents the heart rate results from the SoC via UART communication. RealTerm, a serial terminal software, was used to display the results.

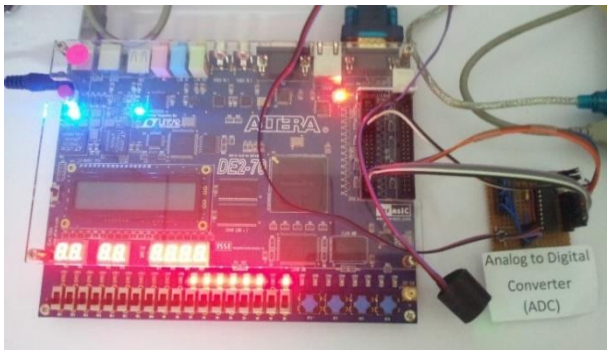

Figure 10: SoC using the FPGA platform with ADC and pulse sensor

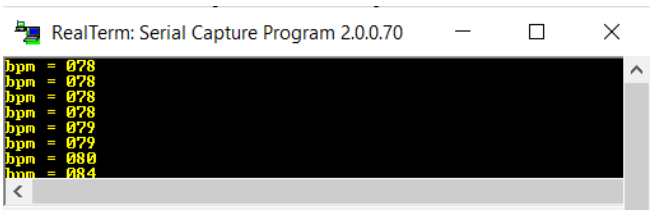

Figure 11: UART terminal of the PC displaying the data received from the SoC

In order to evaluate the heart rate monitoring system, three measurement method was chosen which are by counting radial pulse through wrist in a minute, OMRON blood pressure monitor HBP-1300, and proposed heart rate monitoring system. A 26-year-old male student was selected to perform different activities during heart rate measurement. Heart rate measurement was taken during the student is resting and after walking for 100m. The measured heart rate was tabulated in Table 2. The results of the measurements show that the student had a normal resting heart rate of between 70 and 90 BPM; this is an average heart rate for a

26-year-old male person [16]. Karvonen Formula [17-19] is used to calculate target heart rate (THR) which is expressed below:

$$THR = \left((HR_{max} - HR_{rest}) \times \%intensity\right) + HR_{rest} \qquad (1)$$

where: HR_{max} = Maximum heart rate
HR_{rest} = Resting heart rate
$\%intensity$ = Percentage of training intensity

Based on Karvonen Formula [19], the intensity of target heart rate for walking has a range of 40-50%. Hence, the measurement heart rate for walking is acceptable because it doesn't exceed the target heart rate. The percentage differences between different heart rate measurement methods is calculated and tabulated in Table 3. Based on Table 3, heart rate measured by the proposed system had better accuracy as compared to radial pulse counting method. The differences for resting and walking activities are 3.75% and 1.04%, respectively.

Table 2
Heart rate measurement of 26 year old student with different measurement methods (beats per minute)

	OMRON HBP-1300	Radial pulse counting	Proposed heart rate monitoring system
Resting	80	75	78
Walking	95	92	93

Table 3
Comparison of different methods for heart rate measurement in percentage difference

	% of OMRON HBP-1300 vs. Radial pulse counting	% of OMRON HBP-1300 vs. proposed system
Resting	6.25%	2.5%
Walking	3.15%	2.11%

The compilation report shows that the SoC occupied 4,740 logic elements within the Altera Cyclone II EP2C70F896C6 FPGA. A power analysis was carried out on the SoC architecture using PowerPlay Power Analyzer, and was conducted based on vectorless estimation toggle rate for each signal. Based on the report from the Power Analyzer [20], the total power dissipation reported was 199.59 mW, while the core static thermal power dissipation and I/O thermal power dissipation were 154.97 mW and 44.62 mW respectively. Table 4 shows the total logic elements occupied and the various measures of power dissipation in the FPGA.

Table 4
Total logic elements and power dissipation for the ARM processor-based system

Total Logic Elements	Total Thermal Power Dissipation	Core Static Thermal Power Dissipation	I/O Thermal Power Dissipation
4,740	199.59 mW	154.97 mW	44.62 mW

V. CONCLUSION

In this paper, the implementation of a heart rate monitoring system using an ARM Cortex-M0 DesignStart soft-core processor-based SoC is described. The SoC architecture was implemented in FPGA hardware and interfaced with an ADC and a pulse sensor. A beat-finding algorithm was loaded onto the SoC system to perform heart rate monitoring. An experiment was carried out to evaluate the functionality and performance of the SoC, and the results show the measured heart rate of the male student is within the average range for heart rate for an individual of his age. This demonstrates the functionality of the heart rate monitoring system. Based on the power analysis report, the SoC system has a total power consumption of 199.59 mW.

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