New Synthetic Grounded FDNR with Electronic Controllability Employing Cascaded VDCCs and Grounded Passive Elements

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***Abstract*— This research article proposes a synthetic ground connected frequency-dependent negative resistance (FDNR) simulator with electronic tuning facility. The presented simulator is realized by using two voltage differencing current conveyors (VDCCs) along with three grounded passive components (one resistance and two capacitances). Due to use of all grounded passive element, this circuit is suitable for IC integration. The negative resistance offered by proposed simulator circuit can be control by varying the bias currents of used VDCCs. The presented circuit configuration simulates pure FDNR with no need to meet any passive component matching condition. The behavior of designed synthetic FDNR circuit in non-ideal environment is found not deviated from the ideal behavior with low active and passive sensitivity indexes. To find the behavior of presented circuit at high frequencies, the parasitic analysis has been carried out considering the terminal parasitics employed VDCCs. The usability of realized synthetic FDNR is validated by constructing second order low-pass, band-pass and band-reject filters. To verify the mathematical analysis, the presented configuration is simulated under PSPICE simulation environment.**

***Index Terms* — Electronic Tuning Facility; Grounded Synthetic FDNR; Grounded Passive Elements; No Matching Conditions.**

I. INTRODUCTION

The concept of frequency-dependent negative resistance (FDNR) was proposed in [1], which is a very helpful circuit component for designing and synthesis of active elements based filters. Various FDNR simulation circuits using different active elements were proposed in reported literature [2-22]. The FDNR simulation circuits to simulate "FDNR in floating state" were reported in [2-16]. These circuit configurations experience one or more of subsequent disadvantages (i) no electronic tuning facility[2-6, 9-15] (ii)employment of more than two active components [2, 4-9, 11-14, 16] (iii) employment of more than three passive components [3, 7, 9, 11-13] (iv)employment of "capacitance(s) in floating state" [2-5, 10, 13-14] (v) employment of "resistance(s) in floating state" [2-5, 13, 14] and (vi) need of current copy terminals in used active elements[10]. These presented "FDNRs in floating state" can be converted into grounded FDNRs simply by grounding one of the floating end.

In addition to synthetic "grounded FDNRs' realized from floating FDNR simulation structures, several grounded only synthetic FDNRs were also proposed by various researchers [17-22].

A synthetic grounded FDNR constructed using single current conveyor (CCII) and six passive elements was reported in [17] but this simulator undergo many disadvantages features such as excessive requirement of passive components, employment of floating capacitance, unavailability of resistance tuning through electronic means and need of matched passive components. A synthetic grounded FDNR realized using three current controlled current conveyors (CCCIIs) was presented in [18]. Although current controllability of CCCII makes this realization "electronically tunable" but employment of three CCCIIs requires more area on chip in integration. A grounded FDNR simulation structure using two current feedback operational amplifiers (CFOAs), two floating resistances and two grounded capacitances was proposed in [19] but this structure does not has the benefit of electronic tuning and need matched components for lossless FDNR realization. The configurations reported in [20], employs single FDCCII but all these circuits need matching components and do not have facility of resistance tuning through electronic means. Single CFOA based two synthetic grounded FDNRs were presented in [21] but both these structures have floating capacitances and passive element matching constraints. In [22], a single dual–X terminal current conveyor (DX-CCII) based synthetic grounded FDNR was presented. But use of floating capacitance and resistance with no facility of electronic tuning makes this simulator not very useful. A grounded FDNR employing single operational transresistance amplifier (OTRA), two resistances, two capacitances and one voltage buffer was reported in [23], but this configuration requires component matching for realizing lossless grounded FDNR. Employment of floating capacitances is one another drawback of this circuit. A grounded FDNR with electronic control facility using two voltage differential buffered amplifier (VDBAs) was reported in [24] but use of floating resistances and capacitances makes this configuration unsuitable for integration. One another grounded FDNR simulator with electronic tuning employing five operational transconductance amplifiers (OTAs) was proposed in [25] but but use of excessive number of active element makes this configuration bulky and require large area on chip in monolithic integration.

Therefore, the objective of this paper is to present a new synthetic grounded FDNR circuit which is constructed by employing two VDCCs, single grounded resistance and two grounded capacitances.

This configuration offers several useful attributes such as; low requirements of active and passive components (two

VDCCs, two capacitances and one resistance), all the passive elements are grounded, electronic tuning facility of realized negative resistance, no requirements of matching components, low values of sensitivity indexes and no effect on circuit behavior in non-ideal environment. The maximum operational frequency of simulated FDNR is also evaluated considering the terminal parasitics of VDCCs.

II. Basic Idea of VDCC

The idea VDCC active element was invented in [26] and it was found that VDCC is a very useful and versatile active device with six current/voltage ports. It has current controlled input stage transconductance gain and appropriate voltage/current relationships among various ports.

In recent past several applications of VDCC in biquad filter designing [27], impedance simulators [28-30] and oscillator implementations [31-33] were presented by different researchers.

The block representation of conventional VDCC is shown in Figure 1.

The terminals N, P, W_N, W_P and Z are at high impedances while impedance of terminal X is low.

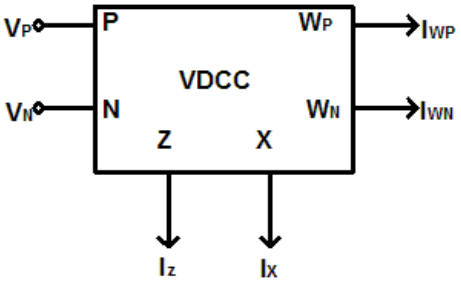

Figure 1: Circuit Symbol of VDCC

The voltage-current relationships among terminals of ideal VDCC are described by below given current-voltage hybrid matrix;

$$\begin{bmatrix} I_N \\ I_P \\ I_Z \\ V_X \\ I_{W_P} \\ I_{W_N} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \\ I_X \end{bmatrix} \quad (1)$$

Where, "g_m" is input stage transconductance gain and I_P, I_N, I_{WP}, I_{WN}, I_Z and I_X are currents at "P" terminal, "N" terminal, "W_P" terminal, "W_N" terminal, "Z" terminal and "X" terminal respectively. In the same manner V_P, V_N, V_Z and V_X are voltages at "P" terminal, "N" terminal, "Z" terminal and "X" terminal respectively.

The Popular implementation of VDCC using CMOS transistors is given in [28].

III. Proposed Synthetic Grounded FDNR

The proposed synthetic grounded FDNR is shown in Figure 2.

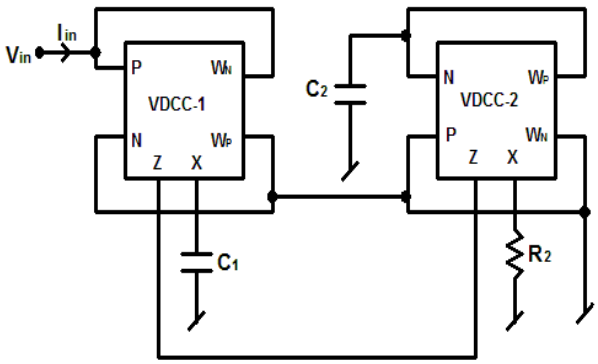

Figure 2: Proposed synthetic grounded FDNR using VDCCs

By the theoretical analysis of circuit given in Figure 2, the equivalent input admittance (Y_{eq}) of this configuration was evaluated as;

$$Y_{eq} = s^2 D_{eq} = \frac{s^2 g_{m1} C_1 C_2 R_2}{g_{m2}} \quad (2)$$

Where

$$D_{eq} = \frac{g_{m1} C_1 C_2 R_2}{g_{m2}} \quad (3)$$

So, Equation (2) clearly indicates that configuration shown in Figure 2 simulates the behavior of a grounded FDNR and the simulated negative resistance is inversely proportional to square of frequency. The value of realized negative resistance at some constant frequency can be varied by varying transcoductance gains gm1 and gm2 of VDCC-1 and VDCC-2.

IV. Non-Ideal Analysis

In non ideal environment, the defining equations of VDCC have been changed as follows;

$$\begin{bmatrix} I_N \\ I_P \\ I_Z \\ V_X \\ I_{W_P} \\ I_{W_N} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \alpha g_m & -\alpha g_m & 0 & 0 \\ 0 & 0 & 1/\beta & 0 \\ 0 & 0 & 0 & \gamma_{WP} \\ 0 & 0 & 0 & -\gamma_{WN} \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \\ I_X \end{bmatrix} \quad (4)$$

Where α is transconductance error, γ_{wp} and γ_{wn} are tracking errors in current transfer and β is tracking error in voltage transfer.

Considering Equation (4), non-ideal input admittance of presented synthetic FDNR can be found as;

$$Y_{eq_{non-ideal}} = s^2 D_{eq_{non-ideal}} = \frac{s^2 \alpha_1 \gamma_{WN1} \beta_2 g_{m1} C_1 C_2 R_2}{\alpha_2 \beta_1 \gamma_{WP2} g_{m2}} \quad (5)$$

where

$$D_{eq_{non-ideal}} = \frac{\alpha_1 \gamma_{WN1} \beta_2 g_{m1} C_1 C_2 R_2}{\alpha_2 \beta_1 \gamma_{WP2} g_{m2}} \quad (6)$$

Where γ_{wp1}, β_1 and α_1 are tracking errors in VDCC-1 and γ_{wn2}, β_2 and α_2, and are errors in VDCC-2. It can be concluded from Equation (5) that even in non-ideal environment, the proposed FDNR simulation configuration acts like a lossless grounded FDNR. Therefore, the behavior of realized configuration is not deviating from ideal behavior even considering non-ideal tracking errors. The sensitivities of realized negative resistance with respect to active and passive components and parameters were evaluated as;

$$S_{\gamma_{WN2}}^{D_{eq_{non\text{-}ideal}}} = S_{\gamma_{WP1}}^{D_{eq_{non\text{-}ideal}}} = 0 \tag{7}$$

$$S_{g_{m_1}}^{D_{eq_{non\text{-}ideal}}} = -S_{g_{m_2}}^{D_{eq_{non\text{-}ideal}}} = 1 \tag{8}$$

$$-S_{\beta_1}^{D_{eq_{non\text{-}ideal}}} = S_{\beta_2}^{D_{eq_{non\text{-}ideal}}} = 1 \tag{9}$$

$$S_{\alpha_1}^{D_{eq_{non\text{-}ideal}}} = -S_{\alpha_2}^{D_{eq_{non\text{-}ideal}}} = 1 \tag{10}$$

$$S_{C_1}^{D_{eq_{non\text{-}ideal}}} = S_{C_2}^{D_{eq_{non\text{-}ideal}}} = 1 \tag{11}$$

$$S_{C_1}^{D_{eq_{non\text{-}ideal}}} = S_{C_2}^{D_{eq_{non\text{-}ideal}}} = 1 \tag{12}$$

It can be seen from Equation (7) to Equation (12) that all the sensitivity indexes have magnitude equal to or less than unity.

V. Effects Of VDCC Terminal Parasitics

At high frequencies the terminal parasitics of VDCC become significant and manipulate the behavior of VDCC based circuits. In CMOS based implementation of VDCC [25], a combination of grounded parasitic resistance "R_P" and grounded parasitic capacitance "C_P" exist at terminal "W_P". Similarly the port "W_N" consist of a parallel combination of grounded parasitic capacitance "C_N" and grounded parasitic resistance "R_N". At "X" terminal a very low value series parasitic resistance "Rx" appears and at "Z" terminal a very high value ground connected parasitic resistance "R_Z" exists. Including parasitics of VDCC-1 and VDCC-2, the presented synthetic FDNR circuit has been shown in Figure 3.

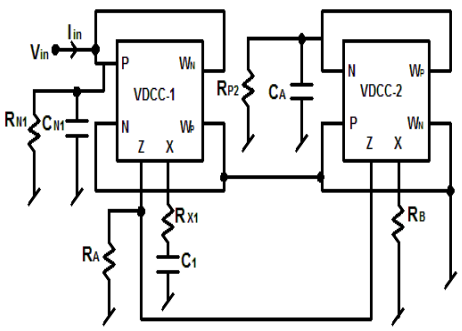

Figure 3: Proposed synthetic grounded FDNR including port parasitics of VDCC-1 and VDCC-2

where

$$R_A = \frac{R_{Z1}R_{Z2}}{(R_{Z1}+R_{Z2})} \tag{13}$$

$$C_A = C_{P2} + C_2 \tag{14}$$

$$R_B = R_2 + R_{X2} \tag{15}$$

The input admittance of configuration shown in Figure 3 can be found as;

$$Z_{in} = \frac{1}{\left[\dfrac{g_{m1}\left(\dfrac{1}{R_{P2}}+sC_A\right)\left(\dfrac{1}{R_{X1}}+sC_1\right)}{\dfrac{g_{m2}}{R_B}+\dfrac{\left(\dfrac{1}{R_{P2}}+sC_A\right)}{R_A}} + \frac{1}{R_{N1}} + sC_{N1}\right]} \tag{16}$$

The equivalent circuit of non-ideal model of proposed synthetic FDNR shown in Figure 3 can be found using Eq. (16) and shown in Figure 4.

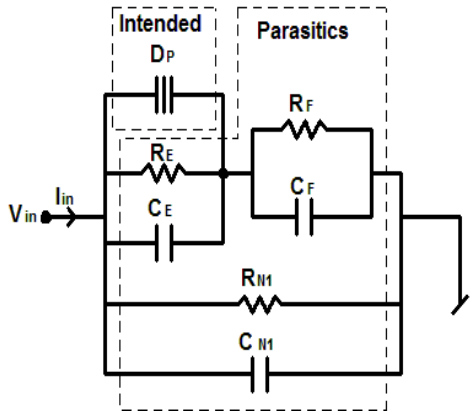

Figure 4: Equivalent circuit of configuration shown in Figure 3.

From Figure 4, it can be seen that the configuration shown in Figure 3 is realizing a complex circuit network which includes a floating FDNR with several additional lossy resistances and capacitances developed due to terminal parasitic impedances of VDCCs. So, circuit is no longer behaving like a grounded FDNR. The intended FDNR "D_P" can be defined as;

$$D_P = \frac{g_{m1}C_AC_1(R_2+R_{X2})}{g_{m2}} \tag{17}$$

The C_E, R_E, C_F and R_F are lossy passive elements. The values of these lossy elements are;

$$C_E = \frac{g_{m1}(R_2+R_{X2})}{g_{m2}}\left(\frac{C_1}{R_{P2}}+\frac{(C_2+C_{P2})}{R_{x1}}\right) \tag{18}$$

$$R_E = \frac{g_{m2}R_{P2}R_{X1}}{(R_2+R_{X2})g_{m1}} \tag{19}$$

$$C_F = \frac{R_{Z1}R_{Z2}g_{m1}C_1}{(R_{Z1}+R_{Z2})} \quad (20)$$

$$R_F = \frac{R_{X1}R_{Z1}R_{Z2}}{(R_{Z1}+R_{Z2})g_{m1}} \quad (21)$$

Therefore, it is clear that for high frequency applications, the terminal parasitics of VDCCs become effective and the behavior of presented simulator circuit is no longer like a lossless grounded FDNR. The maximum operating frequency up-to which the circuit behavior is unaffected by parasitics can be found as:

$$\omega_{0_{max}} \langle\langle \min\left[\frac{1}{R_{N1}C_{N1}}, \frac{1}{R_{P1}(C_{P2}+C_2)}\right] \quad (22)$$

VI. Application Examples

To show the workability of designed synthetic grounded FDNR, some application examples have been discussed. According to concept proposed in [1], a passive LCR networks can be transformed to CDR network without changing the transfer function. By using the method reported in [1], some CDR filters have been developed employing realized synthetic FDNR.

(i) A passive CDR network structure is shown in Figure 5, which realized second order low-pass transfer function (V_{out1}/V_{in}) as well as band-reject transfer function (V_{out2}/V_{in}). The active realization of this network using proposed grounded FDNR is shown in Figure 6. The voltage transfer functions of circuit shown in Figure 6 are;

$$T(s)_{LP} = \frac{V_{out1}}{V_{in}} = \frac{1}{s^2\frac{g_{m1}C_1C_2R_2R}{g_{m2}} + s\frac{g_{m1}C_1C_2R_2R}{g_{m2}C} + 1} \quad (23)$$

And

$$T(s)_{BR} = \frac{V_{out2}}{V_{in}} = \frac{\frac{s^2g_{m1}C_1C_2R_2R}{g_{m2}}+1}{\frac{s^2g_{m1}C_1C_2R_2R}{g_{m2}} + \frac{s\ g_{m1}C_1C_2R_2R}{g_{m2}C}+1} \quad (24)$$

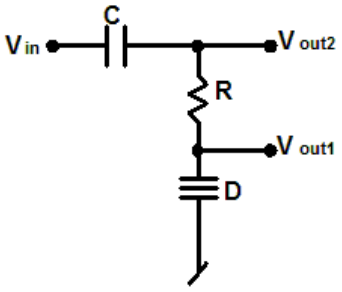

Figure 5: Passive dual function CDR filter.

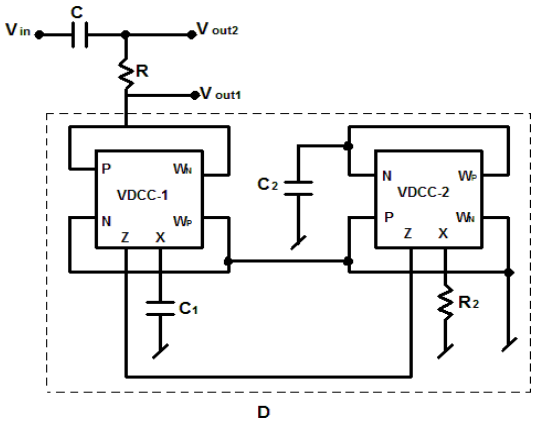

Figure 6: Proposed Synthetic FDNR based implementation of filter shown in Figure 5

(ii) A second order band-pass CDR filter is shown in Figure 7 and its active realization using presented grounded FDNR has been shown in Figure 8. The voltage transfer function of filter shown in figure 8 is found as;

.

$$T(s)_{BP} = \frac{V_{out}}{V_{in}} = \frac{sCR}{\frac{s^2g_{m1}C_1C_2R_2R}{g_{m2}} + \frac{sg_{m1}C_1C_2R_2R}{g_{m2}}+1} \quad (25)$$

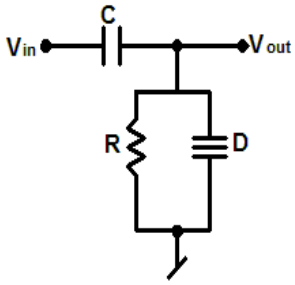

Figure 7: Second order CDR band-pass filter.

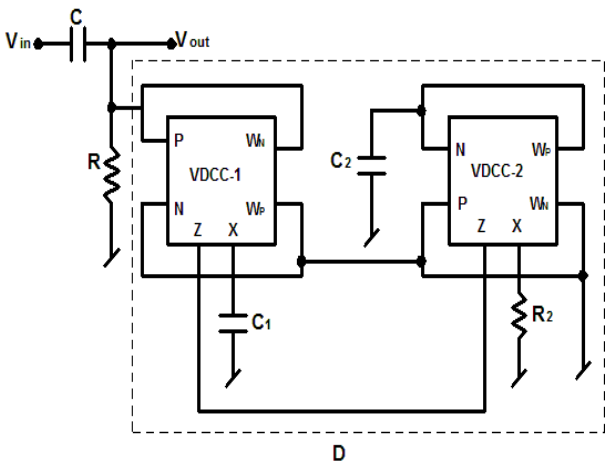

Figure 8: Proposed Synthetic FDNR based implementation of filter shown in Figure 7.

VII. Spice Simulation Results

The demonstration of working of presented synthetic grounded FDNR shown in Figure 2 has been done by

running PSPICE simulations using CMOS model of VDCC [28]. The passive component values used for simulation were; $C_1 = C_2 = 1nF$, $R_2 = 1kohm$, $g_{m1} = g_{m2} = 277.3\ \mu A/V$ with power supply of ± 0.9V DC. The magnitude response plot of input impedance of presented synthetic grounded FDNR is shown in Figure 9. This plot clearly illustrates that the magnitude response obtained by circuit simulation is very close to ideal magnitude response during the frequency range of 19.4 kHz to 1.52MHz. Similarly Figure 10 indicates that the simulated phase response plot of realized synthetic FDNR is closely matching with ideal phase value of -180^0 from 23.7 kHz to 514.4 kHz. At high frequencies, the simulated magnitude/phase responses start moving away from ideal responses due to parasitic of effects of VDCCs under consideration.

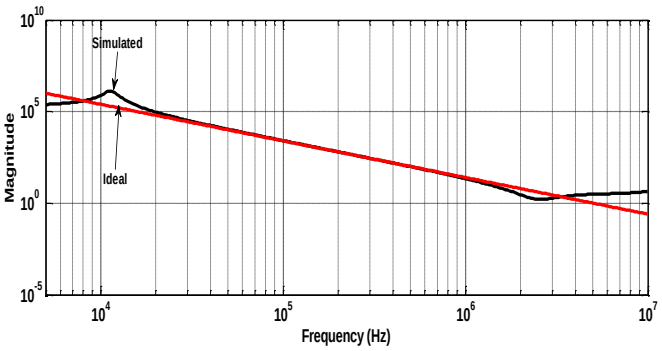

Figure 9: Magnitude response plot of input impedance of realized synthetic grounded FDNR

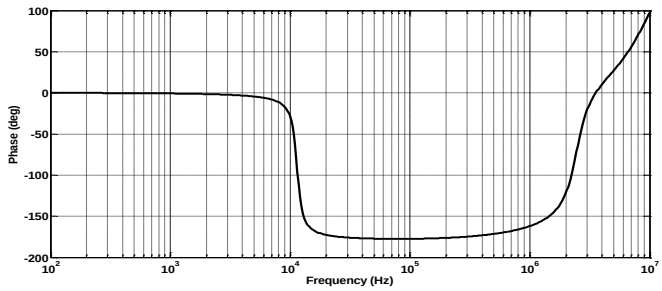

Figure 10: Phase response of input impedance of proposed synthetic grounded FDNR

To show the electronic tuning of presented synthetic FDNR, the simulations have been performed for different values of bias current I_{b2} of VDCC-2. The magnitude responses plots for bias current I_{b2} (of VDCC-2)=I_b= 60 µA, 40µA and 20µA have been shown in Figure 11, keeping bias current I_{b1} of both the VDCCs as 40µA and bias current I_{b2} of VDCC-2 as 25 µA.

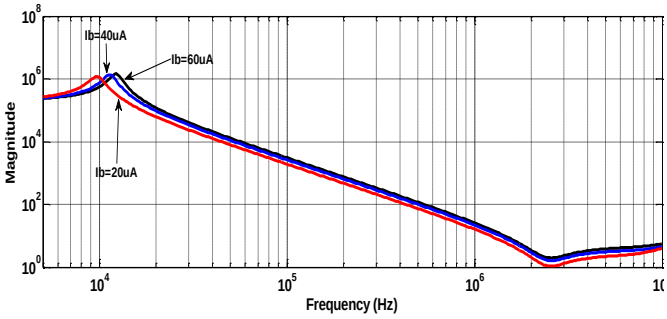

Figure 11: Magnitude response of input impedance of realized synthetic FDNR for different values of bias current.

The performance of second order dual mode CDR filter shown in Figure 6 is confirmed by simulating it using CMOS VDCC [28] with passive elements values; $R = R_2 = 1k\Omega$ and $C_1 = C_2 = C = 1nf$. The simulated low-pass response (V_{out1}/V_{in}) and band-reject response (V_{out2}/V_{in}) are shown in Figure 12 and Figure13 respectively. The low-pass response shown in Figure 12 has a pass-band ripple with cutoff frequency of 156.2 kHz. The ideal value of cutoff frequency is found 159.23 kHz. Hence simulated behavior has close match with ideal behavior.

On investigating the band-reject frequency response shown in Figure 13, it is found that the simulated central frequency is 158.21 kHz which is very near to ideal notch frequency value 159.23 kHz.

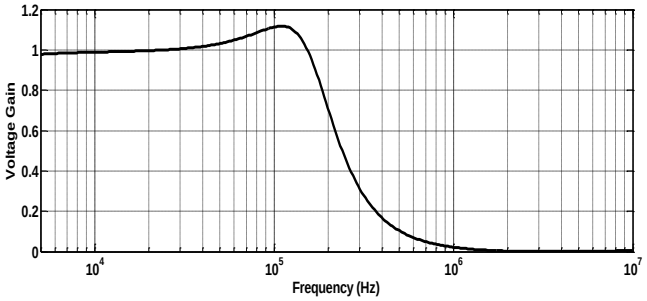

Figure 12: Simulated low-pass frequency response (V_{out1}/V_{in}) of circuit shown in Figure 6.

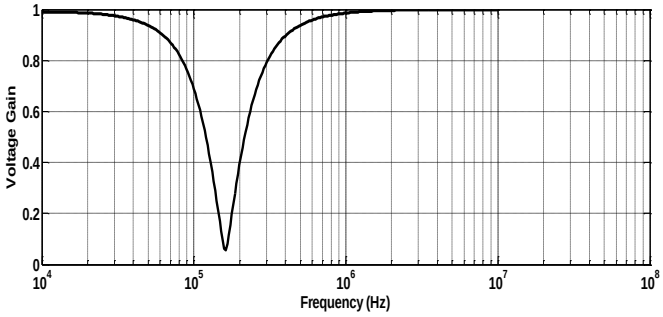

Figure 13: Simulated band-reject filtering response (V_{out2}/V_{in}) of circuit shown in Figure 6

The performance of second order CDR band-pass filter given in Figure 8 is also demonstrated by SPICE simulations. The component values used for simulation purpose were selected as; $R = R_2 = 1k\Omega$ and $C_1 = C_2 = C = 1nf$. The simulated band-pass filtering response (V_{out}/V_{in}) is shown in Figure 14, which clearly illustrate that maximum voltage gain is .95 with central frequency of 157.23 kHz. The ideal central frequency is found 159.23 kHz which is very close to simulated central frequency value.

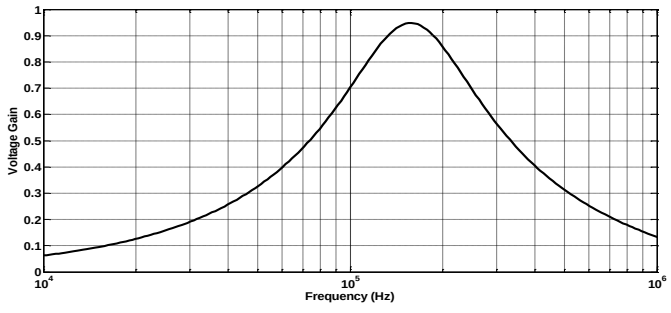

Figure 14: Simulated band-pass filtering response (V_{out}/V_{in}) of circuit shown in Figure 8.

VIII. CONCLUSION

A VDCC based synthetic grounded FDNR has been demonstrated. The proposed synthetic FDNR is constructed by employing two VDCCs and three grounded passive elements. The negative resistance realized by developed circuit can be varied by varying bias currents of VDCCs. Under ideal conditions the designed circuit simulates a lossless FDNR with no need to meet any component matching restriction. In non ideal environment with current/voltage tracking errors also the circuit behavior is not deviated from ideal behavior. All the active and passive sensitivity indexes of proposed circuit were found low. The influence of VDCC terminal parasitic impedances on realized circuit have been discussed and maximum usable frequency was evaluated. The working of realized FDNR simulator has been validated by second order filters design examples. The mathematical analysis of developed configurations, have been verified by SPICE simulations with TSMC CMOS technology at 0.18µm.

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