Low Power Design of MPPT Circuit Using Power Down System in 65nm CMOS Process

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***Abstract*— In the field of light energy harvesting, a great amount of power is wasted when the voltage of the photovoltaic cells does not reach the maximum power point at which the storage will charge at its most efficient manner. The most common solution is to build a maximum power point tracking (MPPT) circuit. However, this still needs improvement with very low energy produced indoor. Thus, aiming to reduce the power consumption of the conventional MPPT system, this study implemented a power down system that turns off idle blocks; hence, improving the performance of the conventional MPPT circuit. From several MPPT techniques, this study implemented the Fractional Open Circuit Voltage Method (FOCV), which has a lower cost and simple circuitry, neglecting the use of a microcontroller. Conventional FOCV-based MPPT systems are composed of a sampling circuit that sets the maximum power point voltage (VMPP) from the sampled open circuit voltage (VOC); and a comparator which assures that the accurate VMPP is stored at the output. From the simulation results, the conventional MPPT consumed a power of 324µW from the PV cell, which is higher than the 255µW consumed by this system. Therefore, the implementation of a power down system saved 21.2% more power than that of the conventional FOCV-based MPPT system. The size of the overall layout implemented in 65nm CMOS technology is 70.955 µm x 34.09 µm.**

Index Terms– Fractional Open Circuit Voltage; Indoor Light Energy Harvesting; Maximum Power Point Tracking; Photovoltaic Cell.

I. INTRODUCTION

Nowadays, electrical energy has been given an importance considering the consumption of this energy has become part of the peoples' day to day lives as it makes their life more convenient. This need has led to an intensive research on utilizing these energies and how it can be accessed from the surroundings. Recent advances show that it can provide solution in powering up different devices and with this kind of development, energy harvesting has been further developed to power up the large to smaller devices, particularly the wireless sensor nodes for accessibility. One of the commonly considered sources of the energy to be harvested is light [1][2]. By means of photovoltaic cells, light energy is converted to electricity [3]. Though, through various researches, it shows that the efficiency of directly storing this energy in a battery is low and that much of the energy is wasted [3][4]. To counter this problem, a Maximum Power Point Tracking (MPPT) circuitry is introduced to improve the efficiency of the light energy harvester systems.

Various algorithms are available in constructing a MPPT circuit. One of them is the constant voltage method or known as 'fractional open circuit voltage' (FOCV). It is the simplest of all methods as it does not require a microprocessor to be operational [5]. It relies on the fact that the MPP voltage of some photovoltaic (PV) cells is proportional to their open-circuit voltage [3] and on the periodic disconnection of the PV cell in the order that its open-circuit voltage is sampled [1][2][6-10]. Another algorithm is Perturb and Observe. The basic idea of Perturb and Observe method is to continually modify the operating voltage of the PV cell [1]. Given that the modification results in a power increase, the perturbation will be adjusted in the same direction. Consequently, if the result of the modification is a decrease in power obtained from the cell, the operating voltage will be adjusted on the opposite direction [5]. Among all the methods in tracking maximum power, fractional open circuit voltage is the simplest and easiest to implement and also has the lowest power consumption [6-10]. Even though this has the lowest power consumption, an improvement is still needed because of the low power generated indoor. In this scenario, improving the power consumption of the MPPT circuit is a must, and a solution that can be done is the implementation of a power down system in the MPPT circuit. This system turns off idle blocks, hence improving the performance of the whole MPPT circuit making the system significant for low-power applications such as the indoor light energy harvesting and the wireless sensor nodes.

A. Limitations

The MPPT design of this study is solely based on the FOCV method, which states that the maximum power point voltage is in linear relationship with the open circuit voltage through constant k. Also, there is no equivalent resistive load used in the output and the input is 1.2V with a ±50mV variation. This study is also limited with the deisgn and simulations implemented only using SYNOPSYS Custom Designer with TSMC 65nm 1P9M CMOS technology. Furthermore, this study is limited in the application of the amorphous silicon photovoltaic cell, specifically the CBC PV a-si solar cell [19] which is simulated to be an ideal solar cell.

II. CONVENTIONAL DESIGN OF MPPT

Maximum power point tracking is a technique used to maximize the power output of an energy harvester [5]. It is implemented by an electronic system that operates the harvester module, photovoltaic cell module, in a manner that allows it to produce the greatest possible power by varying the electrical operating point of the module [11]. This

method is usually implemented in PV cells as their voltage and current has a nonlinear relationship. With this method, PV cells are able to function at higher efficiency. Figure 1 below is the conventional maximum power point design.

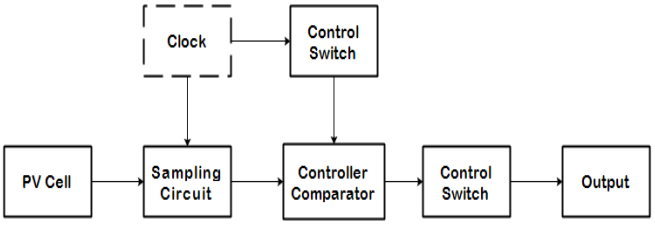

Figure 1: Conventional MPPT Circuit Architecture

Photovoltaic cells or 'solar cells' is basically a p-n semiconductor junction. It is an electronic device that directly converts light into electricity. Its electrical characteristics, such as current, voltage and resistance, varies when exposed to different conditions of light [4]. Two of the most common classifications of the solar cells are the monocrystalline solar cells and amorphous silicon solar cells [17][9].

In this study, the amorphous silicon is used. Amorphous silicon solar cells are thin-film solar cells. It has a wider band gap compared to other solar cells due to its random atomic structure. Therefore, it operates at a relatively high efficiency at low light intensity levels [1][17].This makes them suitable to be used in an indoor light condition [1][18]. The solar cell used in this paper is the CBC PV A-Si solar cell [19].

In this convention, the sampling circuit in Figure 2 samples a certain value of voltage and holds a sampled voltage at a specific time as the reference voltage. As shown below, resistors R1 and R2 that act as a voltage divider will set the value of voltage in ratio to K1 to be stored in the capacitor at maximum power point voltage. According to previous studies, the coefficient K1 is a constant in the range of 0.6 to 0.8. Once the constant K1 is known, Vmpp is obtained by measuring open circuit voltage (Voc) periodically [4]. Consequently, when the PMOS is switched 'on' by the oscillator, the capacitor will charge and when it is switched 'off' the capacitor will hold the voltage and the circuit is in hold mode [8].

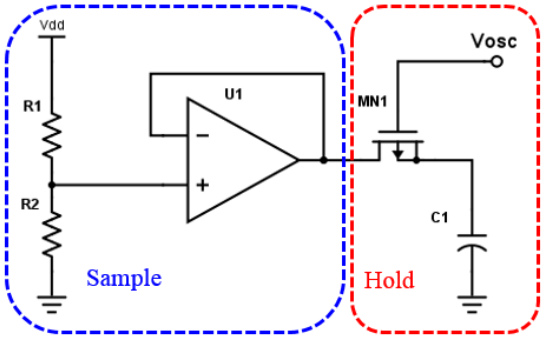

Figure 2: Sampling Circuit

In hold mode, the control switch, shown in Figure 3, is turned 'on' by the clock and the reference voltage is fed to the controller comparator.

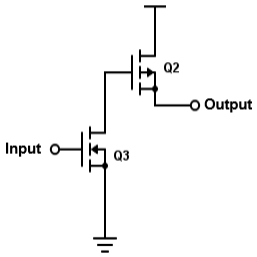

Figure 3: Control Switch

When the controller comparator is turned 'on', it compares the reference voltage to the threshold voltage and provides an 'active' output when the reference voltage against the threshold voltage provided by the voltage divider paralleled, is lower; else the output is 'low'. If the output is 'high', this will turn on the succeeding block which is the control switch. This serves as a check point to assure that the charging voltage of your energy storage capacitor will not try to charge unless the Vmpp voltage is reached [8].

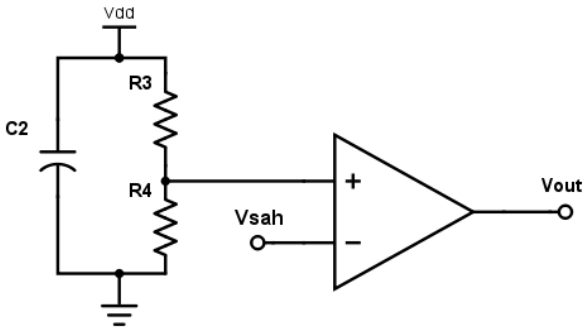

Figure 4: Controller Comparator

III. PROPOSED MPPT DESIGN

Figure 5 shows the proposed MPPT design circuit with the power down system. The major blocks that comprise the whole system are the power down system, sampling circuit and the comparator. The clock is assumed to be ideal, and it is not one of the main concerns of this study.

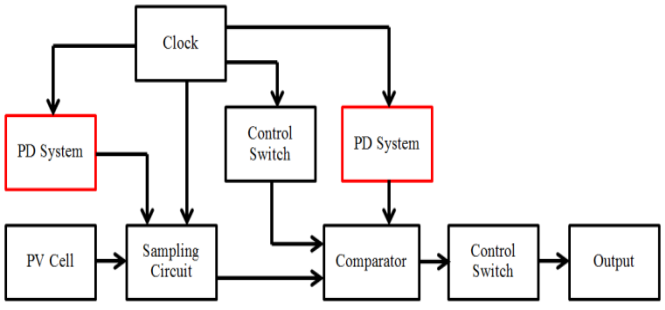

Figure 5: Proposed MPPT Circuit with Power Down System

The circuit starts with the sample and hold circuitry. It samples the voltage from the PV cell and holds it as reference for the following voltage comparator. The clock controls the sample and hold state and the switching of the dynamic power down system of the overall circuit. When the system is in 'hold' mode, the power down switches 'off'

the sampling block of the MPPT circuit. During its 'hold' mode, the control switch before the comparator block is turned 'on' and the capacitor will be charged at VOC value. The comparator then compares the held voltage to the maximum power point voltage (VMPP) from the charging capacitor. When the voltage reaches the maximum power point, the control switch after the comparator block is turned 'on' to charge the storage capacitor. Hence, the MPPT circuit charges the storage capacitor to a voltage equivalent to the VMPP based on the sampled open circuit voltage value from the photovoltaic cell.

A. Sampling Block

The sampling circuit shown in Figure 6 sets the reference voltage for the MPPT system. It consists of two resistors, a buffer amplifier, a transistor switch, and a capacitor. When Vclk is 'HIGH', the transistors MN1 and MP1 are 'ON' and the capacitor C1 is charging. At this state, the output voltage from the PV cell is sampled and the resistors R1 and R2 set the reference voltage to be of a certain fraction of the VOC, which is indeed the value of the VMPP. This voltage value is buffered which charges the capacitor C1 making the voltage across the capacitor (VSAH) also equals to the VMPP. The fractional value is known as the coefficient K1 and which, based on previous researches, is within the range of 0.6 to 0.8 volts. Based from the characteristics of the CBC-PV-01 A-Si PV module, the value K1 used in this study is equal to 2/3 or approximately 0.67 and the VMPP can be calculated from Equation (1) and Equation (2) below [19].

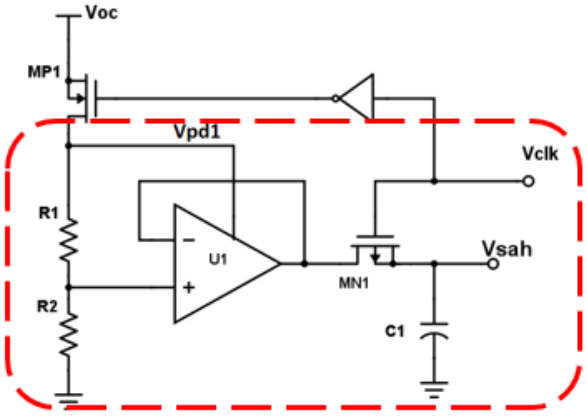

Figure 6: Sampling Circuit Implementation with Power Down

$$V_{MPP} = \frac{2}{3} Voc \quad (1)$$

$$V_{MPP} = \frac{Voc\ R2}{R1+R2} \quad (2)$$

When the Vclk is 'LOW', the transistors MN1and MP1 is switched 'OFF', hence the buffer amplifier is disconnected from the capacitor C1 and the system enters in the hold mode. In this mode, the voltage of the capacitor (VSAH) is stored and will be used as a reference voltage for the next block, which is the comparator. This node VSAH is connected to the inverting input of the comparator. The operation in which the MP1 is switched 'on' and 'off' is further discussed on the Power Down System section in this chapter. The sample and hold circuit is important as it sets our system to not have a varying voltage when charging the storage capacitor.

Vclk represents the clock used to drive the switch. The clock is idealized and modeled as a voltage source employing a pulse behavior having a frequency of 100 kHz with approximately 67% duty cycle [1]. A rise time and fall time of 1ns is imposed to the clock in order to achieve a model close to non-ideal.

B. Comparator Block

The voltage comparator in Figure 7 on the next page assures that the storage capacitor does not charge unless maximum power point is reached. The input in the negative input is the reference voltage (VSAH) that is being held by the capacitor C1 in the sample and hold circuit. When the preceding control switch is operating, it charges the paralleled capacitor C2 of the comparator to the current value of VOC and the resistors will set the non-inverting input to 2/3 of the VOC which is the VMPP. During charging, the comparator continuously compares this voltage to the reference voltage VSAH. If the charged voltage is higher than the reference voltage sampled, the comparator turns on the proceeding control switch allowing the storage capacitor to charge to the current VMPP.

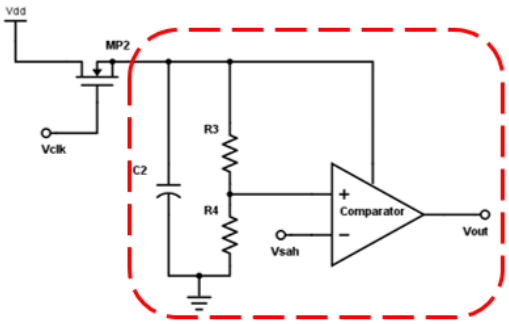

Figure 7: Comparator Block with Power Down

C. Power Down System Implementation

Power consumption of the circuit in low power systems is essential and will greatly affect the overall output. Therefore, any means in reducing the consumed power will improve the performance of the design, implying t that thus the designed power down system is essential. In the proposed MPPT system there is an idle time on the buffer amplifier U1 when transistor MN1 is 'OFF' and capacitor C1 in sampling circuit is not charging. Another idle time exist on the comparator when its preceding control switch MP2 is 'OFF' when the clock (Vclk) is 'HIGH'. The sampling circuit and the comparator blocks switches on and off alternately. At these states, since the buffer amplifier and comparator are not used, switching off its internal components will minimize the power consumption. To implement this, a Power Down (PD) System will be added to the MPPT circuit.

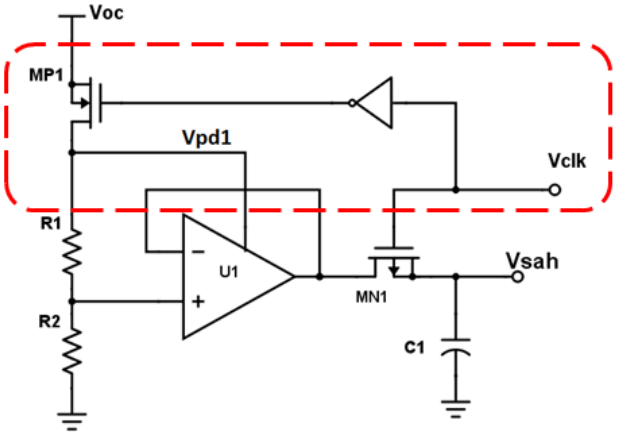

Figure 8: Power Down System for Sampling Block

For the sampling circuit, the system will only use a transistor MP1 and an inverter that will switch the idle blocks on and off. The circuit implementation is illustrated in Figure 8 above. The PMOS (MP1) will be used as a switch that will connect and disconnect the buffer from the Voc. Since the idle time of the sampling circuit exists when the clock output (Vclk) is 'LOW', an inverter circuit will be used to invert the clock output which activates the power down block and hence disconnecting the internal components of the Sampling block. The output from the inverter will control the MP1 connected between the buffer and the Voc and when Vclk is 'LOW' the buffer is disconnected from the Voc. Hence, the PD will lessen the power consumption by disconnecting the block at idle time.
On the other hand, the power down for the comparator block will only need a single transistor in driving the connection of the comparator to the source on and off. Figure 9 below depicts the application of a power down system to the comparator block. The concept is the same as the sample and hold block but with only alternate switching between these blocks following its operation.

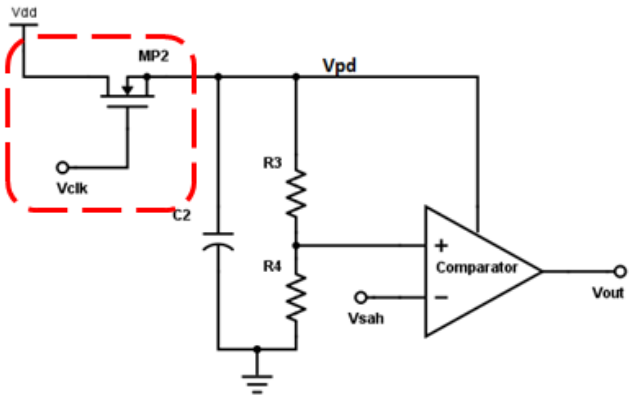

Figure 9: Power Down System for Comparator Block

The overall schematic of the designed MPPT circuit is shown in Figure 10 with all the interconnected blocks. The storage capacitor is labeled C4 in the figure.

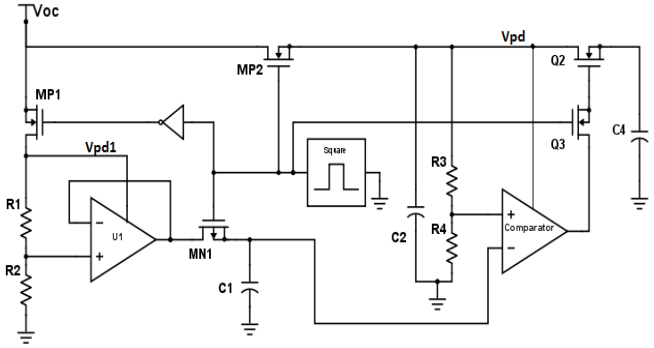

Figure 10: Overall MPPT Circuit with Power Down System

IV. Results and Discussions

This chapter illustrates the individual output response of the sampling block and the comparator block. Furthermore, the results of the implementation of power down system are discussed and also compared to the conventional MPPT circuit. The simulations include the output response and the power consumption of the overall MPPT circuits. The measurements and graphs are done using the Synopsis Custom Waveview tool.

A.Sampling Block Output Response

The function of this block is to copy the input at 'sample' mode and hold the voltage value at 'hold' mode. The simulation for the sampling block involves an oscillating input voltage with a frequency of 10 kHz (that ranges from about 730mV to 870mV). The output voltage of the sample and hold block is compared to the input as shown in Figure 11 below. The simulation showed that the circuit was able to copy and hold the voltage from the input with a maximum error of 2mV, which is close to the ideal output response.

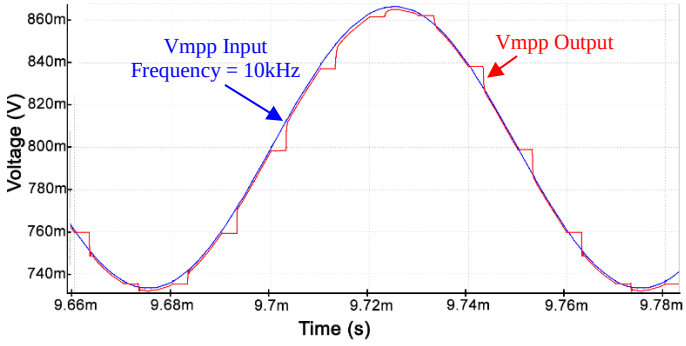

Figure 11: Output Response of the Sampling Circuit.

B. Comparator Block Output Response

The output response of the comparator block is shown in Figure 12. To illustrate the response, the non-inverting input used a sawtooth and the inverting input used a ramp voltage. The function of the comparator is to compare these two input voltages and produce a 'HIGH' or 'LOW' output based on which of the inputs have higher voltage value.

Based on the characteristics of the PV cell used that has a Voc of 1.2V, the maximum voltage, which is the 'HIGH' output voltage in this simulation is also 1.2V and the 'LOW' output is 0V. It can be seen from the figure above that the output is 'HIGH' when the non-inverting input (sawtooth) has greater voltage value than the inverting input (ramp) and

is 'LOW', if it is otherwise. Thus, the output response of the comparator block is in line with the ideal comparator.

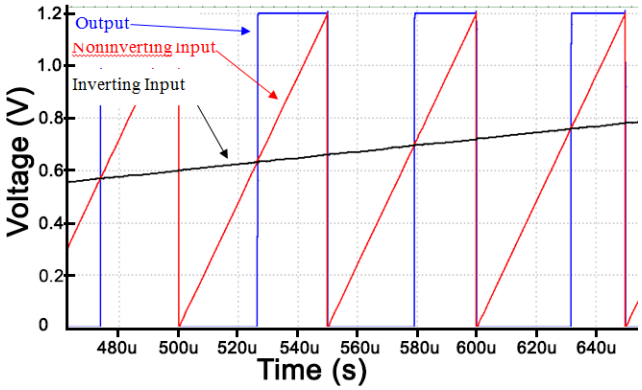

Figure 12: Output response of the comparator block

C. MPPT Output Response

The ideal Vmpp can be derived from Equation (1), which is 2/3 of the Voc. Given that the PV cell used in this study has a Voc of 1.2V, the ideal Vmpp is 800mV. The comparison of the output response between the reference MPPT and the MPPT with power down system is shown in Figure 13. It can be seen from the figure that oscillations are formed. This is due to the variation of the voltage input that accounts for the variations that happened in the surroundings of the PV cell. Though there are oscillations, the value of this oscillation is very small and still produces an average output near the ideal response.

Using the Synopsys Custom Waveview tool, the outputs are measured as shown in the figure below. The MPPT with PD system is represented by the color blue, while the conventional MPPT is represented by the color red in the graph. The MPPT with power down system showed an output of 806mV, while the one without power down showed an output of 811mV. Clearly, the output of the proposed MPPT is closer to the ideal output with an accuracy of 99.25% than the conventional one having an accuracy of 98.625%. In terms of settling time, the output of the proposed MPPT settled at 5.29ms, which is faster compared to the 6.32ms settling time of the reference MPPT output. Therefore, the output response of the MPPT with PD system is closer to the ideal output.

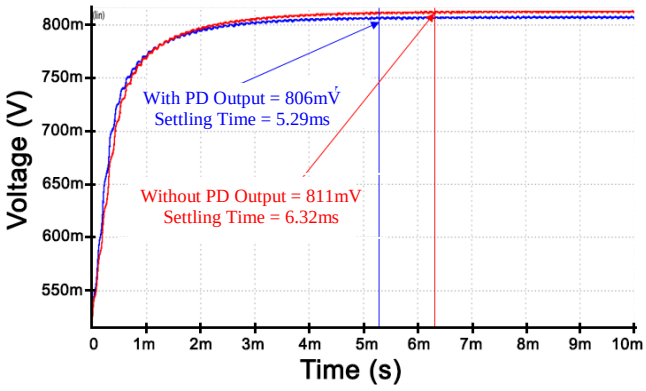

Figure 13: MPPT Output Response Comparison

D. MPPT Power Consumption

The average power consumption of the overall MPPT circuit is derived from the Equation (3) and Equation (4) below. The plot and the measurements are achieved using the Equation Builder tool in the Synopsis Custom Waveview. As indicated in Equation (4), the individual average power of each blocks (sample and hold, control switch, comparator, and PD switch) are added to achieve the overall power consumption. In order to get power consumption of the referenced circuit, it is simulated as well. To compare the power consumption, both designs were simulated using the same blocks found in the conventional MPPT, except for the additional power down system for the proposed circuit only.

$$P_{avg} = avg(i(t) * v(t)) \quad (3)$$

$$P_{avg} = avg(P_{sah} + P_{controlswitch} + P_{comparator} + P_{pdswitch}) \quad (4)$$

where: P_{avg} = Average power
i = Current
v = Voltage
P_{sah} = Power consumption of the sample and hold
$P_{controlswitch}$ = Power consumption of control switch
$P_{comparator}$ = Power consumption of the comparator
$P_{pdswitch}$ = Power consumption of the PD system

As shown in Figure 14, the MPPT with PD system consumed an average power of 255uW, while the reference MPPT consumed 324µW. Moreover, the proposed MPPT consumed 69µW lesser, which is 21.2% of the power consumption of the reference MPPT. Since both configurations use the same design blocks excluding the PD system, the results show that the MPPT with PD system has lower power consumption than the reference MPPT.

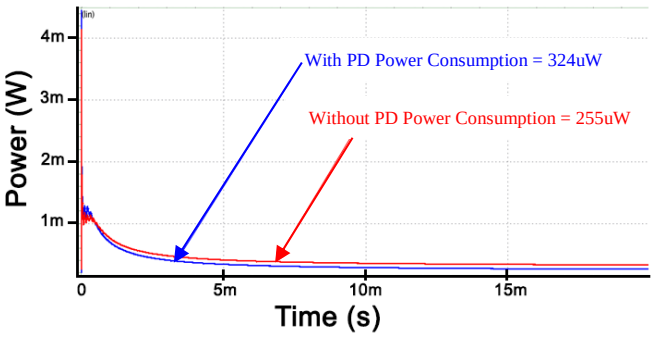

Figure 14: MPPT Power Consumption Comparison

The comparison results discussed in the sections above are summarized in Table 1. This shows that overall the MPPT with power down system has a more accurate Vmpp output and has lower power consumption than the reference MPPT without power down system.

Table 1
Comparison Summary

Parameters	[8]	This Work
Voc	1.2V	1.2V
Vmpp	811mV	806mV
Accuracy Percentage	98.625%	99.25%
Power Consumption	324µW	255µW
Power Saved	-	21.2%

V. CONCLUSION

A maximum power point tracking circuit has been designed by adding a power down system. The design takes the advantage of the different operation time of the major blocks, turning off the block that is not in use at a certain time. Furthermore, the maximum power point is achieved through the empirical data analysis that states that the maximum power is achieved when the voltage is at the k ratio of the open circuit voltage. The method stated beforehand is known to be the fractional open circuit voltage method and is one of the common methods in maximum power point tracking. In connection to this, the maximum power point voltage in this study is achieved with a slight variation to account the environmental changes and is close to the ideal output. Based on the results, the implemented design improved the conventional MPPT circuit by lowering its power consumption. This factor is significant in wireless sensor nodes, in low power light energy harvesting, particularly in indoors, and in other light harvesting applications that require low power design. Lastly, the power saving has been achieved with the implemented design using the SYNOPSYS Custom Designer with 65nm CMOS technology.

ACKNOWLEDGEMENT

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