The Effect of Gate-Induced Drain Leakage (GIDL) on Scaled MOSFETS of Low Power Consumptions

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***Abstract*—This project is aimed to study the impact of Gate-Induced Drain Leakage (GIDL) on scaled Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) for low power efficient application. The MOSFET is operated with low power consumption. Microchip industries are undergoing an evolution where the size of a device is getting smaller, but the performance is great. Thus, this project studies the leakage mechanism in terms of the GIDL current on MOSFET that operates for low power and its physical size had been reduced. The output of this project will determine on what is the implications of GIDL on the performance of MOSFET with various sizes that been supplied with low voltage power. The characteristic of GIDL was studied and from those characteristics, MOSFET design parameters were proposed by referring to the International Technology Roadmap for Semiconductors (ITRS), 2011 edition. DEVEDIT and Atlas application in Silvaco TCAD software was used in this project. Three MOSFET with different physical gate length and several other parameters were designed in DEVEDIT application, then being simulated for data extraction in Atlas application. From the data extracted, it shows that as the size of MOSFET physical gate length become smaller, the leakage current tends to be higher. Apart from GIDL current (IGIDL) value, the "ON" current (ION) value and threshold voltage (VTH) value also been extracted for all MOSFET designs.**

***Index Terms*—Gate-Induced Drain Leakage (GIDL); Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET); Scaling; Low Power Application.**

I. INTRODUCTION

Over four decades, semiconductor industry have undergoes various transformation in the improvement of its product. Moores' Law stated that processor speed or an overall processing power for computers will double for every two years. [1] It specifically states that the number of transistors of an affordable Central Processing Unit (CPU) would double for every two years. The early basic concept of the integrated circuit was to pack in multiple transistors, the devices that regulate current in a circuit, into a single, tiny chip, which would almost eliminate the distance between the circuits and therefore increase the speed with which electronic instructions flow through a computer.

As the improvement of Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) develops through times, the innovation of microchips had been evolved in many forms. [4] The size of the microchips is getting smaller. As it goes smaller, it would save more production cost which wills benefits the producer.

However, one of the problems that always occur when scaling of MOSFET being conducted is the Gate-Induced Drain Leakage (GIDL) current. GIDL is a crucial issue for scaling of the MOSFET. It is induced by the Band-to-Band Tunnelling (BTBT) effect in strong accumulation mode and generated in the gate-to-drain overlap region. The surface BTBT or GIDL increases exponentially due to the reduced gate oxide thickness. Thus, this project investigates the impact of GIDL on scaled MOSFETs for low power application. The result indicates that GIDL is significantly higher when the size of MOSFET physical gate length is being reduced.

II. DEVICE SIMULATION PROCESS

Development of this project is divided into two phase. The first phase is regarding the information gathering, analyzing and research on scaled MOSFET for low power application. The most important part this research phase being conducted is to familiarize the characteristics and impact of Gate-Induced Drain Leakage (GIDL) on MOSFET itself. All data and information collected is used when analysis for the impact of GIDL on all proposed design parameters were conducted.

Meanwhile, second phase is designing process of the MOSFET. These designs were constructed by using Silvaco TCAD software. The criterion of all three designs is based on the proposed suitable parameters.

The first stage in this process is by designing the MOSFET by using DEVEDIT application. All the dimension sizes were set according to the parameters that will be tested and some fixed parameters. Then, the base region and desired impurities was being doped into the structure.

After MOSFET being designed by using DEVEDIT application, it will then been tested and executed in Atlas application. In here, the desired graphs will be plotted by Tonyplot application. From graphs obtained, input voltage (VIN), gate-induced drain leakage current (IGIDL), and threshold voltage (VTH) had been extracted. Finally, analysis on the impact of GIDL for every design was carried out. The GIDL impact on all three design also been compared.

III. DEVICE DESIGN SIMULATION RESULTS

A. MOSFET Design with 24nm Physical Gate Length

Figure 1 shows the MOSFET design with 24nm gate length while Figure 2 shows the contour structure with junction depth for 24nm gate length MOSFET design. Figure 3 shows the Log Current (A) for Power Supplied to 24nm MOSFET Design.

Table 1
Overall MOSFET design parameters

Parameters	Physical Gate Length (nm)		
	24.0	16.0	9.8
Power Supply Voltage (V)	0.70	0.61	0.51
Channel Doping (Boron) (10^{18}/cm^3)	3.7	0.1	0.1
Silicon Dioxide (SiO_2) Thickness (nm)	0.9	0.8	0.7
Junction Depth (Xj) (nm)	9.0	6.0	3.7
Source/Drain Impurities (Arsenic) (10^{19}/cm^3)		1.0	
MOSFET Body Dimension (nm)		80 x 20	
Source/Drain Electrode Dimension (nm)		15 x 2	

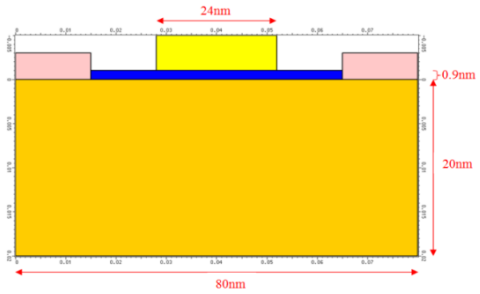

Figure 1**:** MOSFET design with 24nm gate length

B. MOSFET Design with 16nm Physical Gate Length

Figure 4 shows MOSFET design with 16nm gate length while Contour structure with junction depth for 16nm gate length MOSFET design. Figure 5 represent the contour structure with junction depth for 16nm gate length MOSFET design. Figure 6 shows the Overlay Graph of Gate Voltage (V) against Log Current (A) for Power Supplied to 16nm MOSFET Design.

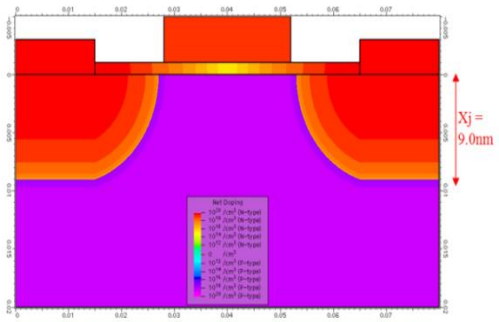

Figure 2**:** Contour structure with junction depth for 24nm gate length MOSFET design

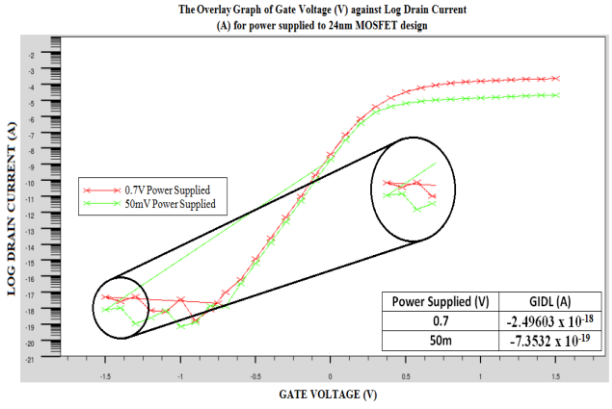

Figure 3: The Overlay Graph of Gate Voltage (V) against Log Current (A) for Power Supplied to 24nm MOSFET Design

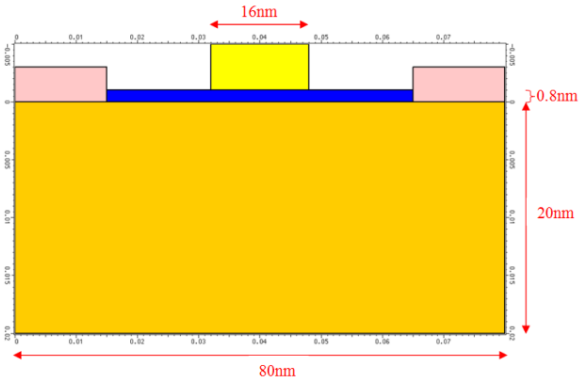

Figure 4: MOSFET design with 16nm gate length

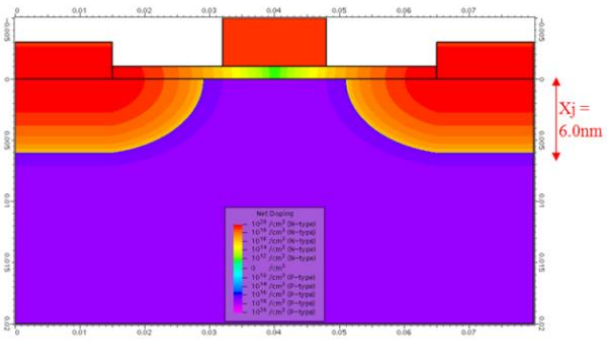

Figure 5: Contour structure with junction depth for 16nm gate length MOSFET design

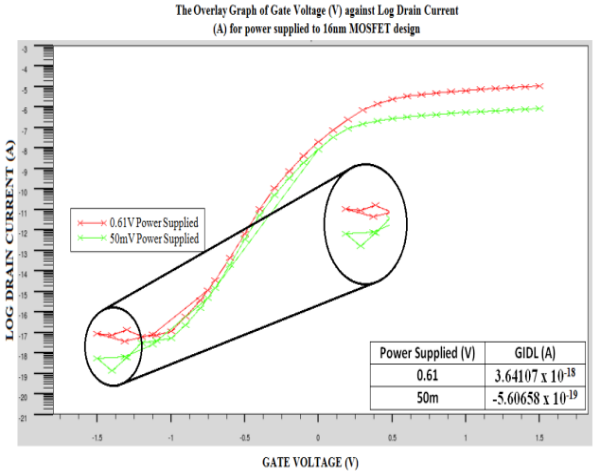

Figure 6: The Overlay Graph of Gate Voltage (V) against Log Current (A) for Power Supplied to 16nm MOSFET Design.

C. MOSFET Design with 9.8nm Physical Gate Length

Figure 7 represent the MOSFET design with 9.8nm gate length. Figure 8 shows the contour structure with junction depth for 9.8nm gate length MOSFET design. Figure 8 shows the contour structure with junction depth for 9.8nm gate length MOSFET design. Figure 9 represent the Overlay Graph of Gate Voltage (V) against Log Current (A) for Power Supplied to 9.8nm MOSFET Design.

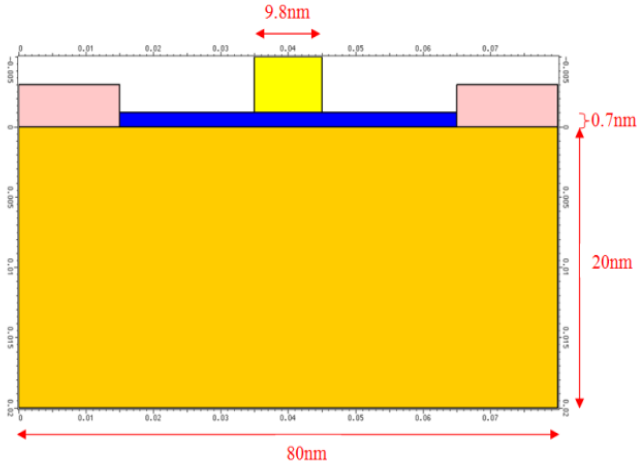

Figure 7: MOSFET design with 9.8nm gate length.

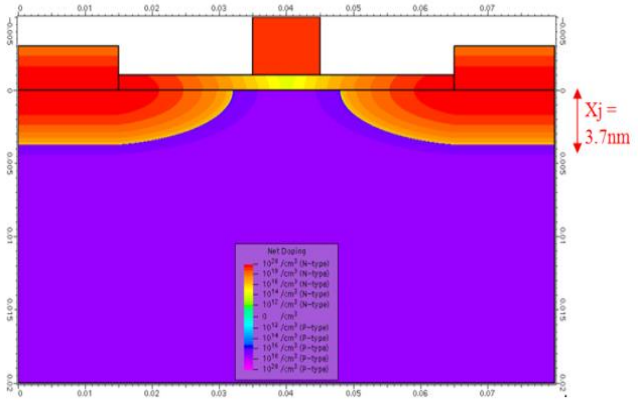

Figure 8: Contour structure with junction depth for 9.8nm gate length MOSFET design.

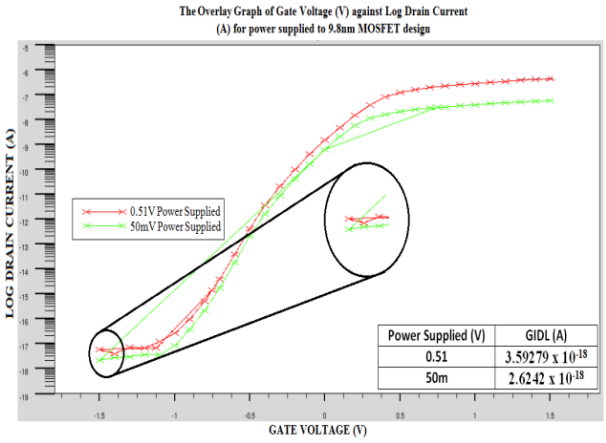

Figure 9: The Overlay Graph of Gate Voltage (V) against Log Current (A) for Power Supplied to 9.8nm MOSFET Design.

IV. Device Design Performance Analysis

Based on Table 2, it is obvious that there is difference between the extracted result readings on proposed power supplied if compared to 50mV power supplied into MOSFET structure designed. 50mV was supplied to observe the effect on MOSFET extracted data when it was supplied with fixed voltage value.

Table 2
The Overall Extracted Data

Gate Length (nm)	24		16		9.8	
Power Supply (V)	0.7	50 m	0.61	50m	0.51	50m
I_{ON} (A)	2.38 x 10^{-4}	2.17 x 10^{-5}	1.02 x 10^{-5}	8.07 x 10^{-7}	4.30 x 10^{-7}	5.80 x 10^{-8}
GIDL (A)	9.0 x 10^{-18}	8.7 x x 10^{-19}	8.5 x 10^{-18}	6.3 x 10^{-19}	6.0 x 10^{-18}	5.0 x 10^{-18}
V_{TH} (V)	0.315	0.2	0.2	0.1	0.125	0.05

For MOSFET designs with 24nm gate length, when it was supplied with 0.7V power, the "ON" current (I_{ON}) is 2.38 x 10^{-4} A, GIDL current (I_{GIDL}) is 9.0 x 10^{-18} A, threshold voltage (V_{TH}) is 0.315 V. Meanwhile, the extracted values when supplied with 50mV power shows the "ON" current (I_{ON}) is 2.17 x 10^{-5} A, GIDL current (I_{GIDL}) is 8.7 x 10^{-19} A, threshold voltage (V_{TH}) is 0.2 V. Comparing both the results, we can say that the "ON" current (I_{ON}) decreases when much lower power is supplied. GIDL current (I_{GIDL}) also results in decreasing value from 9.0 x 10^{-18} A to -8.7 x 10^{-19} A. Only threshold voltage (V_{TH}) shows increase value when the power supplied is decreases.

As for MOSFET design with 16nm gate length, the proposed supplied power is 0.61V. Result shows the "ON" current (I_{ON}) is 1.02 x 10^{-5} A, GIDL current (I_{GIDL}) is 8.5 x 10^{-18} A, threshold voltage (V_{TH}) is 0.2 V. When power supplied was change to 50mV, the "ON" current (I_{ON}) shows decrement to 8.07 x 10^{-7} A. GIDL current (I_{GIDL}) reading also showing decrement from 8.5 x 10^{-18} A to 6.3 x 10^{-19}. While threshold voltage (V_{TH}) decreases to 0.1 V.

On the other hand, MOSFET design with 9.8nm gate length was supplied with 0.51V power. The "ON" current (I_{ON}) is 4.30 x 10^{-7} A, eventually dropped to 5.80 x 10^{-8} A when power is supply is decreased to 50mV. Extracted GIDL current (I_{GIDL}) is 6.0 x 10^{-18} A increases to 5.0 x 10^{-18} A, when supplied with 50mV power. Decrement from 0.125 V to 0.05 V of threshold voltage (V_{TH}) also happens.

Analysing through the increment and decrement pattern of "ON" current (I_{ON}), GIDL current (I_{GIDL}) and threshold voltage (V_{TH}) on each MOSFET design when supplied power is changed, it can be said that the "ON" current (I_{ON}) and GIDL current (I_{GIDL}) decreases when lower power is exerted on it. On the other hand, threshold voltage (V_{TH}) increases.

However, by referring to the extracted result for the proposed power supplied to the MOSFET designs, the readings shows that for MOSFET with 24nm, 16nm and 9.8nm gate length, "ON" current (I_{ON}) and threshold voltage (V_{TH}) decreasing as the length of physical gate decreases, but the GIDL current (I_{GIDL}) increases as the length of MOSFET gate reduced.

Threshold voltage (V_{TH}) shifting is caused by an electrostatic field that is no longer resembles the planar capacitor as the effect of device scaling. Shifting of the threshold voltage value will cause lack in pinch off and definitely will increase the leakage current and output conductance. Gate capacitance will change upon device scaling.

Analysis for the leakage current shows that when the MOSFET physical gate length was being reduced, the GIDL current increases. It was found that the GIDL current increases by 5.56% when the physical gate length was reduced from 24nm to 16nm. Larger leakage value was get when physical gate length was reduced from 16nm to 9.8nm where the GIDL current increases by 29.41%.

The huge difference on GIDL current increment percentage especially on MOSFET physical gate length being reduced from 16nm to 9.8nm is due to the limitation constraints of the SILVACO TCAD software that had been use during the conduction of this project. Previous research stated that SILVACO TCAD software is not suitable to be used in simulating MOSFET with physical gate length which is lower than 15 to 12nm.[6] Other software such as Synopsys' Sentaurus TSUPREM4 or Ab Initio Quantum is said to be the one that is compatible to simulate MOSFET design with extremely short physical gate length.

V. CONCLUSION

This project was implemented to study and investigate on what is the impact of Gate-Induced Drain Leakage (GIDL) on low power consumptions Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) when we scaled down the size. When low voltage is applied to operate the MOSFET, the power consume by digital circuit is reduced. This means that power consumption is proportional to the square of voltage supplied. As for the leakage current, the leakage mechanism that overlaps from gate drain will cause GIDL when drain voltage is very high if compares to the gate voltage. All designed MOSFET was simulated with proposed supply voltage, 0.7V for 24nm gate length, 0.61V for 16nm gate length and 0.51V for 9.8nm gate length, and the constant simulation voltage which is 50mV for all designs. The constant 50mV was simulated to observe the data extraction difference with the proposed voltage supplied. As for the extraction result, the data pattern for "ON" current (ION) for both the proposed and constant voltage supplied shows that there is decrement in ION value as the physical gate length decreases. However, as for the GIDL current (IGIDL) and threshold voltage (VTH), the pattern for MOSFET with 9.8nm gate length shows slightly different result. This is due to some limitations that occur in this project. As this project was conducted by using SILVACO TCAD software, previous research state that MOSFET with physical gate length lower than 15 to 12nm is not really compatible to be simulated. By using SILVACO TCAD, the simulation still can be done, but the extracted data will be slightly different due to certain constrain errors.

REFERENCES

[1] S. T. M, 2006. Scaling of MOSFETs, in Indo German Winter Academy, Digha

[2] C., Ren-Ji, C.T., Sah, 1983. IEEE Transaction on Electron Devices

[3] J.R.,Brews. 1979. IEEE Trans. Electron Dev. ED-26(11):1696

[4] C. Fiegna, et al. 1994. Scaling The MOS Transistor below 0.1um, IEEE Transactions on Electron Devices, 41(6)

[5] T., Hiramoto, 2000. Low Power and Low Voltage MOSFET, Special issue on low power, high speed CMOS technology, 38(2):9

[6] S.A.,Parkle , 1992. Design for suppression of GIDL, IEEE Transaction on Electron Devices, 39(7):3

[7] J.L.A.Y.Y.K.,Fang , 2008. Investigation of Bulk Traps Enhanced Gate Induced Leakage Current in Hf-based MOSFETs, IEEE Electron Device Letter, 29(5): 509 - 511,

[8] B.C.A.L,Harrison., 2007. Zero-power MOSFETs reduces power consumption, in Advanced Linear Devices, Sydney

[9] Y. J.-H., Bum-Joon Kim, 2011. Characteristics of Low-powered Dual MOSFET, University of Seoul, Seoul,

[10] K., Jeon, 2012. Band-to-Band Tunnel Transistor Design and Modeling for Low Power Applications, University of California, Berkeley.