Implementation of Taguchi Method for Lower Drain Induced Barrier Lowering in Vertical Double Gate NMOS Device

K. E. Kaharudin, F. Salehuddin, A. S. M. Zain, M. N. I. A. Aziz
Centre for Telecommunication Research and Innovation, Faculty of Electronic and Computer Engineering, Universiti Teknikal Malaysia Melaka (UTeM), Hang Tuah Jaya, Durian Tunggal, 76100 Melaka.
khairilezwan@yahoo.com.my

***Abstract*—This paper presents a study in which an attempt has been made to reduce the drain induced barrier lowering (DIBL) in Vertical Double Gate NMOS device by optimizing multiple process parameter using L_{12} orthogonal array of Taguchi method. The device performance depended on the amount of DIBL effects that were successfully suppressed in the device. The Taguchi method comprised an orthogonal array (OA), main effects, signal-to-noise ratio (SNR) and analysis of variance (ANOVA) which were employed to analyze the effects of multiple process parameters on the DIBL of the device. Analysis of the experimental results revealed that the halo implant tilt angle was the most dominant process parameter which had a major influence on DIBL value with 62% of factor effect on SNR. Meanwhile, the lowest possible DIBL value retrieved after the optimization approach was observed to be 43.97 mV/V.**

***Index Terms*—ANOVA; DIBL; SNR; Taguchi Method.**

I. INTRODUCTION

In the devices with long channel lengths, the gate is totally responsible for depleting some part of the device. For the very short channel devices, part of depletion is completed by the source and drain bias [1]. As the drain voltage (V_D) is increased, more part of the device is depleted by the drain bias, hence decreasing the threshold voltage (V_{TH}) [2]. These effects normally occur in the lightly doped substrates. In the planar MOSFET device structure, a very short channel length will cause the depletion region from the drain reaches the source region, hence reduces the barrier of electron injection as illustrated in Figure 1. This phenomenon is known as punch through. Since less gate voltage (V_G) is required to deplete the region, the barrier for electron injection from source to drain decreases. This is known as drain induced barrier lowering (DIBL). This DIBL effect also occurs in Vertical Double Gate MOSFET architecture. Although, the issue of a small distance between the drain and the source region for a very short physical gate length (Lg) was resolved by applying vertical double gate structure, the DIBL was still the major problem to be addressed. The DIBL value is not only influenced by the device architecture, but also through the variation of multiple process parameters in the device structure. Salehuddin *et al.* have reported that the DIBL effect was successfully reduced in 32nm NMOS device by applying Taguchi method [3]. Besides that, the most significant process parameters that influence the DIBL value of 32nm NMOS device were successfully identified through ANOVA technique.

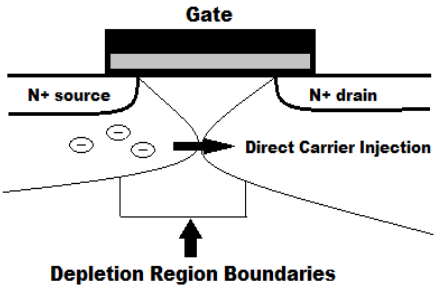

Figure 1: Direct carrier injection

This paper attempts to describe the optimization process of the multiple process parameters for the lowest possible DIBL value in the Vertical Double Gate NMOS device by utilizing L_{12} orthogonal array of Taguchi method. The main purpose was to find the optimal value of the involved process parameters producing the lowest DIBL value. Taguchi method was proven to be an effective statistical tool in MOSFET device's optimization [4-7]. Furthermore, Taguchi method was widely utilized to optimize the process parameters in mechanical and chemical engineering fields. For instance, Kamarudin *et al.* used Taguchi method to optimize the injection moulding parameters for manufacturing products [8]. The total shrinkage of an injection molding product was successfully enhanced by optimizing the injection molding parameters using Taguchi method. Asghar *et al.* utilized Taguchi method and central composite design (CCD) to optimize the Fenton oxidation process [9]. The final results showed that Taguchi method was better than CCD in optimizing Fenton oxidation process due to its efficiency and simplicity.

Taguchi method consists of a set of experiments that were used to investigate the dependency of multiple process parameters on the DIBL value. This method relies on the combination of different levels of multiple process parameters which were guided by a special set of orthogonal array (OA). OA was known as a matrix set which is arranged in column and row. The Taguchi method utilized signal-to-noise ratio (SNR) analysis to measure multiple process parameter

variations toward DIBL value. There are several SNR analysis depending on the type of characteristics which are known as lower-the-better, nominal-the-best and higher-the-better [10]. The importance of certain process parameter is determined by the percentage of factor effects on SNR, which are computed by using analysis of variance (ANOVA).

II. Materials And Methods

A. Virtual Fabrication

An Ultrathin Pillar Vertical Double Gate NMOS device was virtually fabricated by using a ATHENA module of SILVACO TCAD tools. Initially, a P-type silicon with <100> orientation was used as the main substrate for this experiment. Initial silicon was then being doped with 1 x 10^{14} atom/cm^3 of boron. The formation of BOX was done by depositing 16 nm oxide thickness (t_{BOX}). Next, an enhanced channel was developed on the top of the BOX formation by depositing polysilicon material with 8nm of thickness. Both formations were capable of suppressing short channel effects (SCEs) due to a reduction of the amount of charge carriers penetrating the depletion region. The mobility of charge carriers in the channel region will become more rapid, thus increasing the drive current (I_{ON}). The silicon was dry etched in order to form a pillar or ridge with a diameter of 12 nm (T_{SP}) that separates the two polysilicon gates. The height of the silicon pillar of 168 nm (Hsp) was chosen to provide the channel length (Lc) of 90 nm.

The aluminum layer was deposited on the top of the Intel-Metal Dielectric (IMD) and unwanted aluminum was etched to develop the contacts [11, 12]. The final vertical double gate NMOS device structure was completed by mirroring the right-hand side structure. The completed structure of Vertical Double Gate NMOS device is illustrated as in Figure 2.

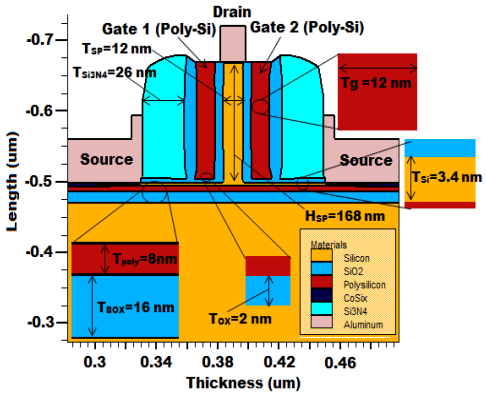

Figure 2: Vertical Double Gate NMOS Structure

B. Orthogonal Array of Taguchi Method

The L_{12} orthogonal array of Taguchi method has been selected to be an optimization tool to reduce the DIBL value in vertical double gate NMOS device. The process parameters that were involved for optimization purpose were substrate implant dose, V_{TH} implant dose, V_{TH} implant energy, halo implant dose, halo implant energy, halo implant tilt, S/D implant dose, S/D implant energy, S/D implant tilt, compensation implant dose and compensation implant energy. Each of them were represented by symbols: A, B, C, D, E, F, G, H, J, K and L. The values of the process parameters (control factors) and noise factors at different levels are listed in Table 1 and Table 2.

Table 1
Process parameters and their levels

Symbol	Process Parameters	Units	Levels	
			Low (1)	High (2)
A	Substrate Implant Dose	atom/cm^3	1x10^{14}	1.03x10^{14}
B	V_{TH} Implant Dose	atom/cm^3	9.81x10^{12}	9.84x10^{12}
C	V_{TH} Implant Energy	kev	20	21
D	Halo Implant Dose	atom/cm^3	2.61x10^{13}	2.64x10^{13}
E	Halo Implant Energy	kev	170	172
F	Halo Implant Tilt	degree	24	27
G	S/D Implant Dose	atom/cm^3	1.22x10^{18}	1.25x10^{18}
H	S/D Implant Energy	kev	43	45
J	S/D Implant Tilt	degree	80	83
K	Compensation Implant Dose	atom/cm^3	2.51x10^{12}	2.54x10^{12}
L	Compensation Implant Energy	kev	60	62

The noise factors are the important parameters to be included in the design of experiment (DoE). The noise factors should be used to form different testing conditions that allow the signal-to-noise ratio (SNR) accurately measures sensitivity to noise factors. In the MOSFET fabrication process, the temperature of certain process is the important noise factor that could contribute to the overall process variation. Normally, noise factors should not be mixed in with the control factors in an orthogonal array experiment. To save the experimental effort, control factors as well as the noise factors were assigned to the column of the orthogonal array experiment.

Table 2
Noise factors and their levels

Symbol	Noise factor	Units	Level 1	Level 2
U	Gate Oxidation Temperature	C^o	927	930
V	Polysilicon Oxidation Temperature	C^o	870	873

In the current study, the design of experiment (DoE) consists of 11 process parameters with two levels and two noise factors with two levels were used. The experiment only took 48 runs with Taguchi method. It greatly reduces the number of tests compared to conventional factorial design which took 324 (2^{11}x2^2) runs. An $L^{12}(2^{11})$ orthogonal array which comprised of 12 experiment was utilized. The experimental layout for the process parameters using the $L^{12}(2^{11})$ orthogonal array is shown in Table 3.

Table 3
L_{12} orthogonal array Taguchi method

Experiment No.	Process Parameter Level										
	A	B	C	D	E	F	G	H	J	K	L
1	1	1	1	1	1	1	1	1	1	1	1
2	1	1	1	1	1	2	2	2	2	2	2
3	1	1	2	2	2	1	1	1	2	2	2
4	1	2	1	2	2	1	2	2	1	1	2
5	1	2	2	1	2	2	1	2	1	2	1
6	1	2	2	2	1	2	2	1	2	1	1
7	2	1	2	2	1	1	2	2	1	2	1
8	2	1	2	1	2	2	2	1	1	1	2
9	2	1	1	2	2	2	1	2	2	1	1
10	2	2	2	1	1	1	1	2	2	1	2
11	2	2	1	2	1	2	1	1	1	2	2
12	2	2	1	1	2	1	2	1	2	2	1

III. Results And Discussion

The electrical characteristics of the device for the first set of experiment were simulated by utilizing ATHENA module of Silvaco International. Then, the results of DIBL value were obtained, analyzed and optimized by applying L_{12} orthogonal array of Taguchi method to get the optimum fabrication recipe. Figure 3 depicts the contour mode of vertical double gate NMOS device that shows the device's doping profile. The figure clearly visualizes the tabulation of silicon, silicon dioxide, polysilicon, silicon nitride, cobalt salicide and aluminum. A good doping concentration is desired in MOSFET fabrication as it ensures the device will work well with enhance gate control and lower leakage current [13].

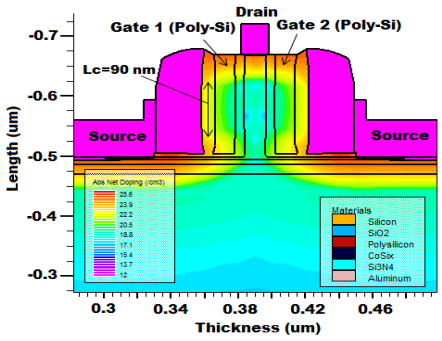

Figure 3: Contour mode of Vertical Double Gate NMOS device

A. *Characterization of Vertical Double Gate NMOS Device*

Figure 4 shows the graph of drain current (I_D) versus gate voltage (V_G) at drain voltage V_D = 0.05 V and voltage V_D = 1.0 V for p-channel vertical DG-MOSFET device. The initial threshold voltage (V_{TH}) value for this device is observed to be 0.401 V.

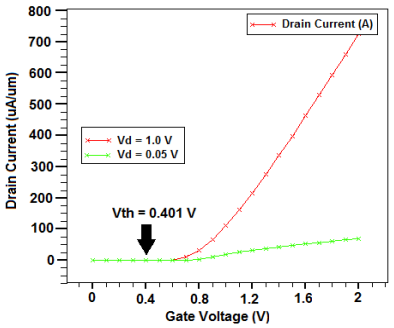

Figure 4: Graph of drain current (I_D) versus gate voltage (V_G)

Figure 5 depicts the graph of subthreshold drain current (I_D) versus gate voltage (V_G) at drain voltage V_D = 0.05 V and V_D = 1.0 V for vertical double gate NMOS device. The value of leakage current (I_{OFF}) and drive current (I_{ON}) was extracted from the graph.

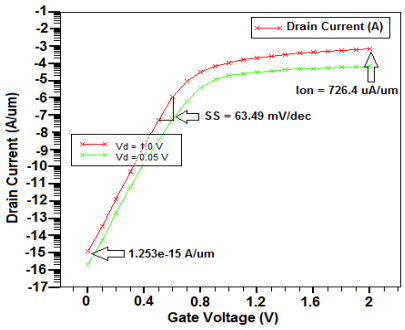

Figure 5: Graph of subthreshold drain current (I_D) vs. gate voltage (V_G)

Figure 6 shows the graph of drain current (I_D) versus ramp gate voltage (V_G) at drain voltage V_{D1} = 0.1 V and voltage V_{D2} = 3.0 V for n-channel device. This step is required to obtain two different values of threshold voltage which are V_{TH1} and V_{TH2}. Afterwards, the value of DIBL was computed by using the Equation (1) [3]:

$$DIBL = \frac{V_{TH1} - V_{TH2}}{V_{D2} - V_{D1}} \quad (1)$$

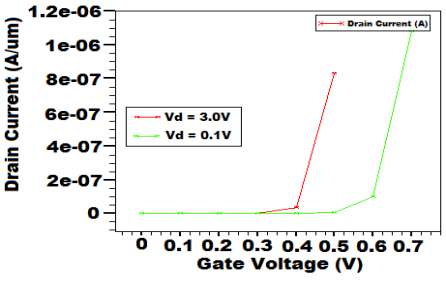

Figure 6: Graph I_D- Ramp V_G for Vertical Double Gate NMOS Device

After retrieving the simulation results, it was observed that the initial DIBL value was 66.21 mV/V. In the next section, L_{12} orthogonal array of Taguchi method was then implemented

in order to reduce the DIBL value as low as possible. Besides that, the process parameters that contributed the most significant impact on DIBL value were identified.

B. Signal-to-noise Ratio (SNR) Analysis

In Taguchi method, the signal-to-noise ratio (SNR) is used to measure how the device characteristic varies relative to the target value under different noise condition. Higher values of SNR will identify the process parameter level settings that minimize the effects of the noise factors. The experimental results of the DIBL value for vertical double gate NMOS device were obtained by using L_{12} orthogonal array with two noise factors as listed in Table 4.

There are three categories of performance characteristics which are known as lower-the-better, higher-the-better and nominal-the-best. However, the type of signal-to-noise (SNR) analysis that was assigned to analyze the DIBL values was the lower-the-better type. The SNR (Lower-the-better), η can be expressed as Equation (2) [12]:

$$\eta = -10Log_{10}\left[\frac{1}{n}\sum_{i=1}^{n} y_i^2\right] \quad (2)$$

where n is number of tests and y_i is the experimental values of DIBL. The SNR for each row of experiments were computed and recorded in Table V by using the formula given in Equation (2).

Table 4
DIBL values for Vertical Double Gate NMOS Device

Exp no.	Drain Induced Barrier Lowering , DIBL (mV/V)			
	$DIBL_1$ (U_1V_1)	$DIBL_2$ (U_1V_2)	$DIBL_3$ (U_2V_1)	$DIBL_4$ (U_2V_2)
1	66.21	65.78	66	65.29
2	47.72	64.48	56.33	61.77
3	65.34	64.3	64.86	63.17
4	65	63.66	64.3	62.23
5	43.97	47.05	51.14	56.83
6	48.07	63.19	58.5	65.25
7	65.96	65.38	65.58	64.59
8	46.9	50.96	56.32	62.38
9	52.32	58.27	64.44	63.91
10	66.37	65.97	66.3	65.68
11	54.42	62.67	65.79	65.34
12	65.78	65.16	65.53	64.41

Basically, the row that demonstrates the highest SNR will be regarded as the best performance characteristics. Based on Table 5, the experiment row no. 5 has the highest SNR value for DIBL which is -33.98dB. This result indicated that experiment row no. 5 had the best insensitivity for DIBL value. Since the design of experiment (DoE) was orthogonal, the SNR of each process parameters can be separated out. The SNR (Lower-the-better) was summarized in Table 6. Based on Table 6, the graph of factor effect for SNR (Lower-the-better) was plotted as illustrated in Figure 7. The dashed horizontal lines in both graphs represent the overall mean of SNR (Lower-the-better) which is -35.71dB.

Table 5
Mean Sum of SQ and SNR for DIBL values

Exp no.	Mean Sum of SQ	SNR (Lower-the-better) (dB)
1	4.30E+03	-36.37
2	3.40E+03	-35.26
3	4.20E+03	-36.18
4	4.10E+03	-36.1
5	2.50E+03	-33.98
6	3.50E+03	-35.44
7	4.30E+03	-36.31
8	3.00E+03	-34.72
9	3.60E+03	-35.55
10	4.40E+03	-36.4
11	3.90E+03	-35.88
12	4.30E+03	-36.29

Based on Figure 7, factor: A1, B2, C2, D1, E2, F2, G2, H2, J1, K2 and L1 were selected as the optimum value for the lowest DIBL due to their highest SNR. Factor: A, B, C, D, E, F, G, H, J, K and L represent Substrate Implant Dose, V_{TH} Implant Dose, V_{TH} Implant Energy, Halo Implant dose, Halo Implant Energy, Halo Implant Tilt, S/D Implant Dose, S/D Implant Energy, S/D Implant Tilt, Compensation Implant Dose and Compensation Implant Energy respectively.

Table 6
SNR of process parameters in Vertical Double Gate NMOS

Symbol	Process Parameter	SNR (Lower-the-better)		Overall mean SNR
		Level 1	Level 2	
A	Substrate Implant Dose	-35.55	-35.86	-35.71
B	V_{TH} Implant Dose	-35.73	-35.68	
C	V_{TH} Implant Energy	-35.91	-35.5	
D	Halo Implant Dose	-35.5	-35.91	
E	Halo Implant Energy	-35.94	-35.47	
F	Halo Implant Tilt	-36.27	-35.14	
G	S/D Implant Dose	-35.73	-35.68	
H	S/D Implant Energy	-35.81	-35.6	
J	S/D Implant Tilt	-35.56	-35.85	
K	Compensation Implant Dose	-35.76	-35.65	
L	Compensation Implant Energy	-35.65	-35.76	

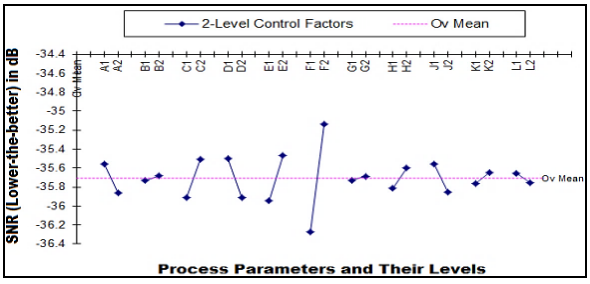

Figure 7: Factor effects graph for SNR (Lower-the-better)

C. Signal-to-noise Ratio (SNR) Analysis

Analysis of variance (ANOVA) is a table of information that displays the relative influence of factor or interaction

assigned to the column of orthogonal array. ANOVA measures parameters such as the sum of squares (SSQ), degree of freedom (DF), variance or mean square (MS), F-value and percentage of the effect of each factor (process parameter). The results of ANOVA for DIBL values are listed in Table 7. Generally, a larger F-value for certain process parameter indicates that the variation of process parameter contributes a significant change on the device performance.

According to Table 7, factor F (halo implantation tilt) was identified to be the most dominant factor (process parameter) contributing the most impact on DIBL value for the device. The percentage of factor effect on SNR indicates the priority of a factor (process parameter) to reduce variation. For a factor with a high percentage of contribution and a small variance (mean square) will have a great influence on the device's performance. The percentages of factor effect on SNR of all process parameters are shown in Figure 8.

Table 7
Results of ANOVA for DIBL in Vertical Double Gate NMOS

Process Parameter	DF	SSQ	MS	F-value	Factor effect on SNR	Dominant/ Significant/ Neutral
A	1	0	0	447	4	Neutral
B	1	0	0	13	0	Neutral
C	1	0	0	776	8	Significant
D	1	0	0	791	8	Significant
E	1	1	1	1064	11	Significant
F	1	4	4	6160	62	Dominant
G	1	0	0	8	0	Neutral
H	1	0	0	215	2	Neutral
J	1	0	0	415	4	Neutral
K	1	0	0	62	1	Neutral
L	1	0	0	49	0.49	Neutral

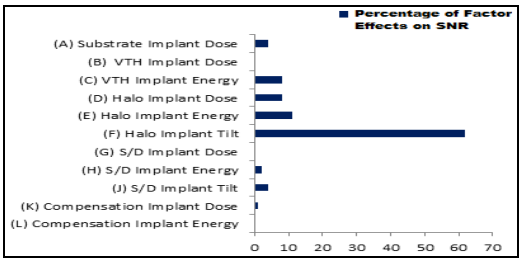

Figure 8: Pareto plot of Percentage of Factor Effects on SNR for DIBL

Based on Pareto plot in Figure 8, factor F (halo implant tilt) has the highest percentage of factor effect on SNR which is 62%. Therefore, halo implant tilt was regarded as a dominant factor and its level cannot be altered. Meanwhile, the percentage of factor effect on SNR of factor C (V_{TH} implant energy), factor D (halo implant dose) and factor E (halo implant energy) were observed to be 8%, 8% and 11% respectively. These factors were considered as significant factors as their levels were also not suggested to be altered. The remaining factors are regarded as neutral (pooled) as they contribute to almost zero percentage of factor effects on SNR. Hence, the neutral factors can be set at any level. The full recommendation for this optimization is A1, B2, C2, D1, E2, F2, G2, H2, J2, K2 and L1.

IV. CONFIRMATION TEST

Confirmation test is the final step in the design of experiment (DoE) process. The main purpose of the confirmation test is to validate the results retrieved during analysis phase [15]. Since the most optimum combination level of process parameters; A1B2C2D1E2F2G2H2J2K2L1 is different from any of the experiments in Table IV, the confirmation test has to be implemented. The best level setting of the process parameters for the device suggested by Taguchi method is shown in Table 8.

Table 8
Overall Best Level Setting of Process Parameters

Symbol	Process Parameter	Units	Best Value
A	Substrate Implant Dose	atom/cm^3	1x10^{14}
B	V_{TH} Implant Dose	atom/cm^3	9.84x10^{12}
C	V_{TH} Implant Energy	kev	21
D	Halo Implant Dose	atom/cm^3	2.61x10^{13}
E	Halo Implant Energy	kev	172
F	Halo Implant Tilt	degree	27
G	S/D Implant Dose	atom/cm^3	1.25x10^{18}
H	S/D Implant Energy	kev	45
J	S/D Implant Tilt	degree	83
K	Compensation Implant Dose	atom/cm^3	2.54x10^{12}
L	Compensation Implant Energy	kev	60

The final step is to verify the reduction of DIBL value by simulating the device once again using the best level setting of process parameters. The final simulation results of the device are shown in Table 9. The SNR for vertical double gate NMOS device after the optimization approach was -34.20 dB. The value was well within the predicted SNR range of -33.72 to -34.67 dB. The lowest possible DIBL value was observed to be 43.97 mV/V with both noise factors were set to the lowest level. The halo implant tilt angle was identified to be the most influenced process parameter towards the DIBL value in vertical double gate NMOS device.

Table 9
Results of the Confirmation Test for DIBL

Drain Induced Barrier Lowering, DIBL (mV/V)				SNR (Lower-the-better) in dB
$DIBL_1$ (U_1V_1)	$DIBL_2$ (U_1V_2)	$DIBL_3$ (U_2V_1)	$DIBL_4$ (U_2V_2)	
43.97	47.05	51.14	56.83	-34.2

The final results were compared to the results of the previous researchers as depicted in Table 10. The DIBL value of the current work was successfully suppressed using Taguchi Method. There was an improvement of 33.59% in the DIBL value after the optimization approach. These results

indicated that the L_{12} orthogonal array of the Taguchi method was capable of predicting the best process recipe of the device with the lowest DIBL value.

Table 10
Comparison of the Optimal DIBL Value with the Previous Researches

Research Works	Method of Study	DIBL (mV/V)
Saad & Razali. (2008) [16].	Simulation by using SILVACO TCAD	94
Rahul et al. (2014)[17].	Simulation by using SILVACO TCAD	44.29
Current research work (Before optimization).	Simulation by using SILVACO TCAD	66.21
Current research work (After Optimization).	Simulation by using SILVACO TCAD and Optimization by using Taguchi Method	43.97

V. CONCLUSION

The optimum solution in obtaining the lowest possible value of DIBL value was successfully predicted by L_{12} orthogonal array of Taguchi method. DIBL value is the main response that has been investigated in this project as it is regarded as the main factor in reducing the short channel effects (SCEs) of the device. The level of significance of process parameters on DIBL is determined by using analysis of variance (ANOVA). Based on ANOVA method, the process parameter which was a major contributor to affect DIBL value was identified as halo implantation tilt angle with 62% factor effects on SNR. The lowest DIBL value obtained using the optimized combination level of 11 process parameters predicted by Taguchi method was observed to 43.97 mV/V.

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