Modelling of 14NM Gate Length La_2O_3-based n-Type Mosfet

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***Abstract*—Gate length shrinkage is still the widely used method in transistor downsizing. In view of this, the downsizing of Equivalent Oxide Thickness (EOT) is also of high importance as it is the main focus in the process. Therefore, various studies on Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) fabricated from high-k dielectric and metal gate have been reported till today. In this paper, a 14nm silicon based n-type MOSFET was virtually fabricated using Lanthanum Oxide (La2O3) on Titanium Silicide (TiSi2). ATHENA and ATLAS modules from SILVACO were used for process and device simulation respectively. The results from this work show that the threshold voltage, VTH, on-current, ION and off-current, IOFF are 0.208397 V, 4.80048 x 10-5 A/μm and 1.00402 x 10-7 A/μm respectively. Furthermore, it is demonstrated that the development of high-k/metal gate MOSFET is a promising prospect for high performance nanoscale transistors.**

***Index Terms*—14nm n-transistor; High-k Dielectric; Metal Gate; ATHENA; ATLAS.**

I. INTRODUCTION

Information Technology has vastly changed the way we live ever since the beginning of industrial production of CMOS (Complementary Metal Oxide Semiconductor) in the 1960s. The need for increased speed and computing power of silicon microprocessors has led to the minimization of transistors in order to achieve higher transistor count and reduced chip size. The continuous improvement and downsizing of MOSFETS has encountered many technological challenges. As the size decreases, its efficiency drops as more heat dissipation occurs and leakage current of smaller transistors increases rapidly. The usage of silicon dioxide (SiO_2) gate oxide as the key material has been the main focus in the downscaling of the devices [1]. Continuous miniaturization of MOSFET over the decades has resulted in hitting the limitation of the physical thickness of SiO_2 with layers thinner than 2 nm having leakage current that is higher than the acceptable level. Reducing the tunneling effect and subthreshold leakage are vital as they are the major source of power consumption in high-performance processors. SiO_2 gate oxide thickness reduction is getting more difficult as SiO_2 has lesser atoms for further downscaling. Therefore, current research effort has been concentrated on new materials, new device structures and nanofabrication techniques [2].

Alternative materials with permittivity and physical thickness higher than those of SiO_2 are interesting options for researchers. The alternative gate dielectric materials must have high dielectric constant, large band gap, high band offset to silicon, thermodynamic stability, good interface quality and process compatibility. High-k material is a good candidate to act as a gate insulator because of its large gate capacitance and gate leakage current suppression characteristics. However, the combination of high-k and polysilicon has high threshold voltage, thus various metal gates have been investigated to set the proper threshold voltage. In view of this, it is crucial for research to focus on new material which could potentially replace silicon technology with a matching metal gate in in the near future of CMOS technology [3, 4].

A. Gate Dielectric Scaling

The transistor scaling principles described by Dennard [5] stated that a reduction of length, width and gate oxide thickness dimensions, doping concentration and voltage by a constant k produces transistors that are k^2 times smaller, k times faster and dissipates k^2 less power. Due to continuous downscaling, conventional MOSFETs face the challenges of having high off-current (I_{OFF}) due to short channel effects (SCEs) [6, 7]. Thinner gate oxide is used to suppress the SCEs. However, the trade-off of using thinner gate oxide is the increase in gate leakage current and tunneling effect [8, 9] which dampens transistor performance. Therefore, alternative materials for gate oxide have been investigated with the goal of finding a material that could increase the physical thickness without increasing the electrical oxide thickness. The term equivalent oxide thickness (EOT) indicates the SiO_2 physical thickness needed in order to have the same electrical characteristic as high-k material. The EOT is defined as:

$$t_{OX} = EOT = \left(\frac{3.9}{k}\right) t_{high-k} \quad (1)$$

The relationship between gate capacitance, C and oxide thickness is:

$$C = \frac{\varepsilon_0 kA}{t_{OX}} \quad (2)$$

where ε_0 is the permittivity of free space, k is the relative dielectric constant, A is the area, t_{OX} is the SiO_2 oxide thickness and t_{high-k} is the physical thickness of high-k material. SiO_2 has a static dielectric constant of 3.9 [10]. From the equation, it can be deduced that high-k dielectric materials meet the gate oxide requirement. High-k dielectric materials allow the increase capacitance with reduced leakage current as the thicker layer is able to hold off gate voltages and has the required EOT. This enables the reduction in size of the transistors without sacrificing performance.

B. *La2O3 as gate dielectric*

Lathanum oxide (La_2O_3) has been considered as one of the possible solutions for gate dielectric to reduce leakage current as it can achieve smaller EOT compare to using SiO_2. In addition, La_2O_3 has a high k value (about 27), relatively large band gap (5.8eV). The conduction band offset (2.3eV) on silicon is also higher than HfO_2 (1.4eV), the most-used high-k material in silicon-based electronics. Furthermore, La_2O_3 has a good thermal stability with silicon. In this research, La_2O_3 is chosen as the high-k dielectric while Titanium Silicide ($TiSi_2$) as gate material to prevent the existence of polysilicon depletion effect. $TiSi_2$ also has lower sheet resistance than polysilicon, ability to be self-aligned and is thermodynamically stable, which makes it a very interesting dielectric material for metal gate.

II. Design and Simulation

A planar 14nm n-type MOSFET was virtually fabricated using ATHENA module from SILVACO. The fabrication was performed on n-type phosphorus-doped silicon substrate with orientation of <100>. The silicon was exposed to dry oxygen to form SiO_2 thin oxide. Ion implantation was then performed using Boron at a dose of 3.75 x 10^{12} cm^{-2} to form p-well. After implantation, the substrate was annealed at 900°C in nitrogen and then dry oxygen to assure an even distribution of boron atoms. Next was the process of forming Shallow Trench Isolator (STI) for the purpose of isolating neighbouring MOSFET transistors [11]. The thickness of the STI was 130Å. Then, the wafer underwent oxidization at 900°C for 25 minutes. Low pressure chemical vapour deposition (LPCVD) of silicon nitride was performed on top of STI oxide layer, followed by 1.0 µm photoresist deposition and then annealed at 900°C for 15 minutes. A sacrificial oxide layer was deposited and etched to relieve induced stresses and defects [12]. The next step was to deposit the high-k material, La_2O_3 with a thickness of 1.5nm. The high-k material was etched to the required thickness and adjusted to produce a 14nm gate length [13]. Since the threshold voltage was the main parameter for the MOSFET, it was precisely controlled by the boron implantation on the N-well active area. The energy of implantation in this step was 5 keV at a dose of 8 x 10^{11} cm^{-2}. The next process was metal gate deposition, where $TiSi_2$ was deposited on top of La_2O_3 with thickness of 5nm [3,12]. Then, Halo implantation was performed with Indium with a dosage of 6.9 x 10^{13} cm^{-2} to control the Short-channel Effect (SCE) [12,14]. Next, sidewall spacers were formed to act as a mask for source-drain implantation. Both phosphorus and arsenic were used for the source-drain implantation. A dose of 1 x 10^{14} ions/cm^2 of arsenic followed by considerably less amount of phosphorus at a dose of 6.8 x 10^{11} ions/cm^2 were implanted to achieve the desired doping profile in the MOSFET. After that, a 0.3µm-thick Borophosphosilicate Glass (BPSG) was formed and referred to as pre metal dielectric (PMD) [15]. Then, annealing was done at 850°C for 20 minutes. It was followed by compensation implantation at a dose of 6.6 x 10^{13} ions/cm^2. Finally, metal interconnects for source and drain were formed. Aluminum was used as the metal contact in this final step. The completed n-type MOSFET was then characterized for its electrical properties using ATLAS to obtain the $V_{TH,}$ I_{ON} and I_{OFF}. These values were then compared with ITRS 2013 prediction.

III. Results and Discussion

The electrical characteristics of the 14nm n-type MOSFETs were verified using ATLAS. Figure 1 shows the cross-section of the NMOS design structure while Figure 2 presents the doping concentration profile where the source and drain are clearly defined.

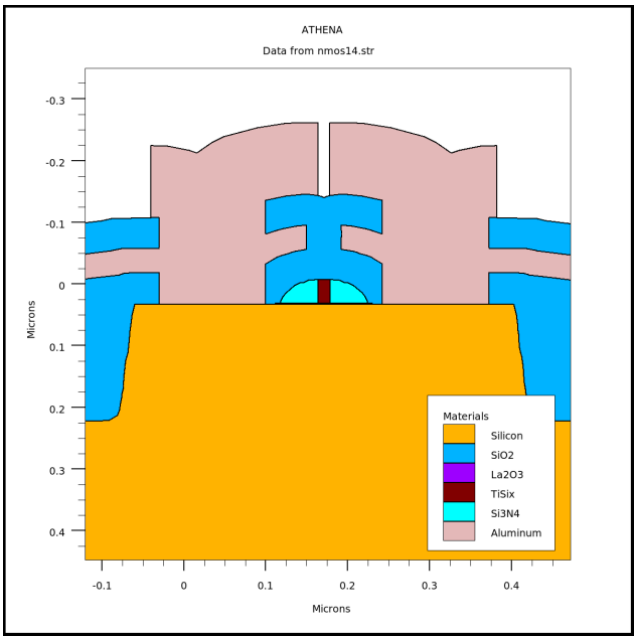

Figure 1. Cross-section of 14nm NMOS structure

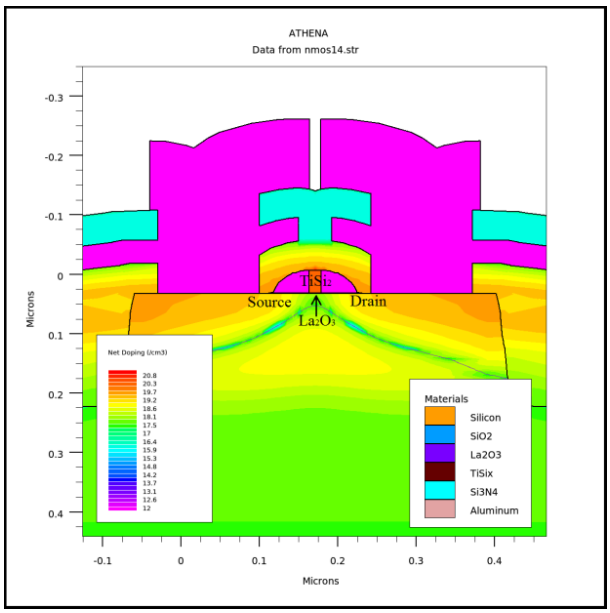

Figure 2. Profile of 14nm NMOS doping concentration

Figure 3 and Figure 4 show the electrical characteristic of the device simulated by ATLAS. Figure 3 presents the drain current, I_D versus gate voltage, V_G characteristics at drain voltage, V_D of 0.5V and 1.0V. Based on the graph, the V_{TH} is 0.208397 V. The V_{TH} value is found to be within the ITRS 2013 prediction. Figure 4 shows the sub-threshold I_D versus V_G at V_D of 0.5V and 1.0V. The NMOS has an I_{ON} of 4.80048 x 10^{-5} A/µm and I_{OFF} of 1.00402 x 10^{-7}A/µm. Although the I_{ON} value is beyond the ITRS target, the results indicated that further research and optimization is needed to obtain better functionality and performance of the device. The comparison between the simulation results and ITRS prediction is depicted in Table 1. The results reported in this research will be optimized in future work.

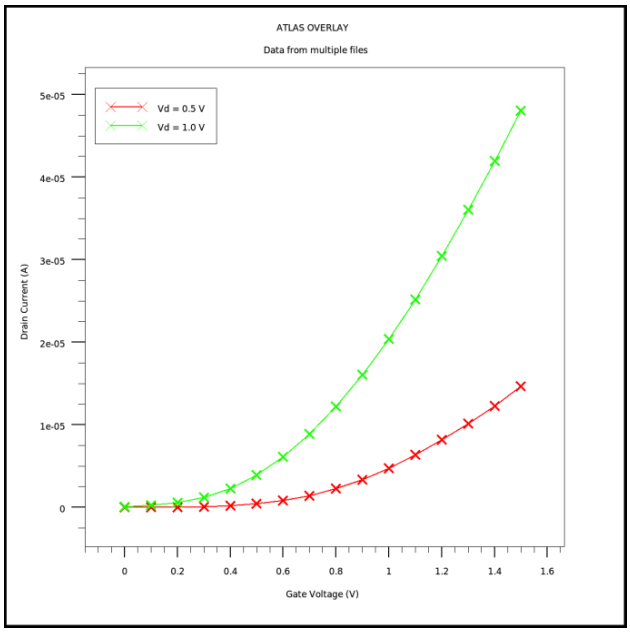

Figure 3. ID-VG curve

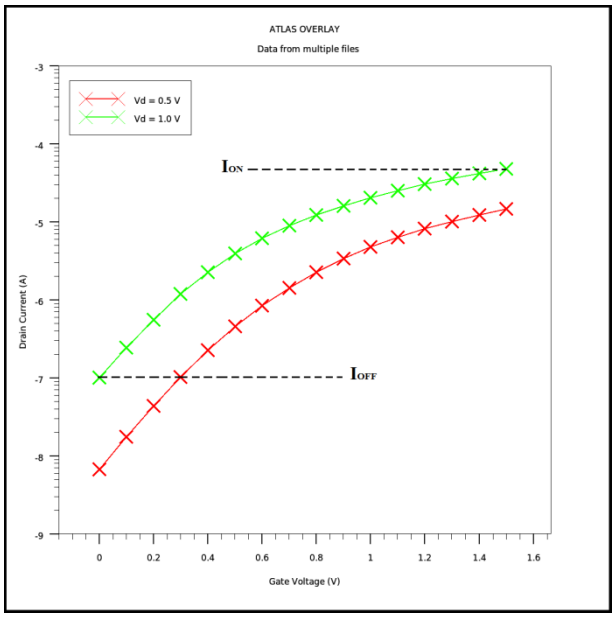

Figure 4. Subthreshold ID-VG curve

Table 1. V_{TH}, I_{ON} and I_{OFF} Results for n-Type Transistor

Parameter	Simulation Result	ITRS Prediction
V_{TH}	0.208397 V	0.20079 V - 0.25921 V
I_{ON}	4.80048 x 10^{-5} A/µm	1267 x 10^{-6}A/µm
I_{OFF}	1.00402 x 10^{-7} A/µm	100 x 10^{-9} A/µm

IV. CONCLUSION

The design of 14nm n-type MOSFET using La_2O_3 as high-k and $TiSi_2$ as gate material was achieved in this research. As the V_{TH}, I_{ON} and I_{OFF} values are within ITRS 2013 prediction, it can be deduced that the device meets the expected performance. Since both results from simulation and prediction are comparable, this research can pave way for future improvements in high-k and metal gate.

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